Investigations of selected influencing process factors for transient liquid phase soldering (TLPS) as a die-attach method for automotive power modules

Bettina Ottinger[1,2], Joshua Holverscheid[1], Sebastian König[1], Annette Brunner[1], Dr. Lars Müller[1], Dr. Christian Goth[1], Prof. Dr. Jörg Franke[2]
[1] *Vitesco Technologies Germany GmbH, Nuernberg, Germany*
[2] *Institute for Factory Automation and Production Systems Friedrich-Alexander University Erlangen – Nürnberg, Germany*

Abstract
Increasing the operating temperatures in power electronic applications cause a decreasing lifetime of the die-attach interconnection. Transient liquid phase soldering (TLPS) is able to create a reliable and high temperature resistant connection layer via diffusion processes in the form of intermetallic phases with melting points up to > 400°C. This study concentrates on a TLPS reflow-soldering process with a tin-copper-tin (Sn-Cu-Sn) layered preform. During the soldering process the influence of the selected process parameters for the Sn-Cu-Sn on the grown intermetallic phase interconnections between the preform and the components are investigated via the average void percentage and a process capability analysis (c_{pK}). The application of mechanical pressure decreases the average void percentage below 10%. Due to the lower average void percentage the influence of the holding time, peak temperature and heating gradient are examined under low pressure. The biggest impact shows the heating gradient. With a slow heating gradient, the thermomechanical stress decreases by increasing the solubility and the average void percentage could be reduced to less than 2.7 %. In combination of the optimized selected process factors it is possible to reach a process capability value of 1.

Key words
die-attach, TLPS, Sn-Cu-Sn, thin solder layers, reflow-soldering process, automotive power module

I. Introduction
Over the last decades the composition of solder alloys has changed constantly. In the past, the most common alloys where lead (Pb) and tin (Sn) based solder alloys. Through different proportionate compositions of the two metals, a huge number of applications could be covered [1]. Due to the fact that lead is clearly toxic and carcinogenic the European Union banned lead for the production of electronic assemblies [2]. Various alternatives are alloys with two or three ingredients with a major proportion of tin >90 % [3,4]. Alloys with more than three ingredients are rare but also used. One of the most common is “Innolot”. The added compounds are normally copper (Cu), silver (Ag), antimony (Sb) and sometimes nickel (Ni) with a proportion up to 10 % [3,4]. The melting point of these alloys is between 200°C and 250°C [3,4]. The big advantage of tin based solder alloys is the relatively low price and the good wetting characteristics on blank copper or silver substrates which leads to nearly void free joints and homogeneous thick solder layers, when used as preforms in vacuum solder processes. Some interface materials like copper and nickel promote the growth of intermetallic phase (IMC) during the soldering of common tin based solders. The growth of the IMC is also the prove of a successful soldering process, because of a firmly bonded interconnection [5]. The layer of intermetallic phase at the interface can have a negative impact on the thermo-mechanical properties of the solder joint because of its brittleness and hardness [1]. That is the reason why the layer should be as thin as possible. During the soldering process of common tin based solders, the soldering time and the peak temperature have the biggest impact on the thickness of the intermetallic layer [1]. Transient liquid phase soldering (TLPS) aims at the growth of intermetallic phase through the complete solder layer. The advantage of a complete intermetallic layer is the high remelting temperature after the soldering process and the firmly bonded interconnection. The commonly known intermetallic phase Cu_6Sn_5 has a melting point of 415 °C [6]. The second IMC phase Cu_3Sn

melts at 676 °C [6]. To generate TLPS interconnects different methods and material properties can be used. One possibility is to transform very thin tin layers into intermetallic phases. The tin layer is realized with a standard SnAgCu solder paste [6]. Alternative ways are solder pastes with copper balls inside or a copper paste with a solder deposit next to the chip [7]. Furthermore, very thin Sn-Cu preforms can be used [8].

This paper concentrates on TLPS-soldering on a preform based reflow-soldering process. The layered structure of the given preform has a copper core inside, coated with thin tin layers on the top and the bottom side. The idea to use preforms is not new and had been considered by Syed-Khaja (2018) [9,14]. The layered preform including a copper core with thin tin layers (Sn-Cu-Sn) has a lot of potential to achieve thin intermetallic phases with a good heat transfer at once. Previous investigations had a look on the assembly technique in general, because the application of solder paste with copper balls in it needs a special treatment and is complex to realize [7]. Other publications investigated the soldering parameters with particular attention on vacuum process steps and the pressure inside the soldering chamber with air pressure up to 240 kPa [8]. The solution with very thin solder paste layers without cooper balls inside showed that if the solder paste layer is too thick, the intermetallic phase will not grow through the complete layer [6]. To avoid this problem the tin layers in the Sn-Cu-Sn preforms show a low thickness. This is favorable to create intermetallic phases but makes it hard to solder void free. Usually solder layers for die-attach have thicknesses of 50µm or more in the industry. The first samples soldered with the layered Sn-Cu-Sn preforms showed very big voids and a bad interconnection of the die and the substrate due to warpage. That is the reason why mechanical pressure is required. To apply this pressure inside of soldering oven stamps are installed. The stamps move down during the soldering process and press on the dies. Different pressures are investigated. Further interactions between the important soldering parameters have been examined in C. Ehrhardt (2017) [11]. The holding time of the peak-temperature, the peak-temperature itself and the heating gradient have been changed and tried to be optimized. The overall goal is to identify the influence of the tested parameters and characterize the main process factors in dependence of the mechanical pressure from the stamp. Criteria for the quality of the solder joint is the average void percentage and the equal formation of the intermetallic phase.

II. Materials and Methods

A. Experimental Procedure

For sample preparation silicon dies with a metallization of nickel and silver are used. The dies are soldered onto direct copper bonded (DCB) substrates consisting of copper and a ceramic for the electrical insulation. The TLPS solder preform consists of a layered structure of tin (Sn) and copper (Cu) with an average thickness of 50 µm. The preform is placed between the silicon die and the DCB substrate (Fig. 1a).

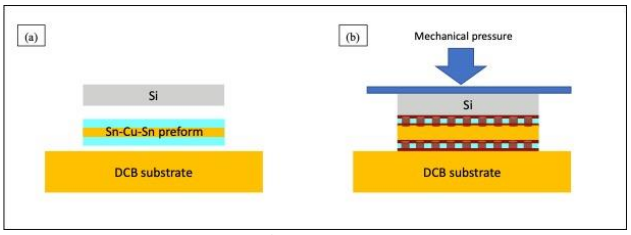

Fig. 1: Schematic drawing of the(a) sample set up and (b) the TLPS soldering process

The soldering process is very similar to standard soldering processes which are used in the industry. Usually, the major steps are pre-heating, soldering at peak temperature and cooling [5]. The standard TLPS soldering process is as follows. At the beginning the assembly is heated up with a standard soldering temperature profile in the reflow soldering oven to transform the tin layers into IMC. During the heating and soldering step different steps are included to remove contaminations and reduce voiding [6,8,9,14]. Additional changes in the holding time of the peak temperature, the peak-temperature and the heating gradient are made.

After the soldering step the samples are slowly cooled down to room temperature to keep the stress on the interconnection as low as possible while it gets solid again. In order to counteract the warpage of the structure, a stamp is used to apply mechanical pressure from the top during the soldering process shown in Fig. 1b.

B. Analysis of the TLPS die-attach interconnection

The main method for analyzing TLPS die-attach interconnections is “scanning acoustic microscopy” (SAM). This is an imaging and non-destructive analysis method which is using ultrasound with a frequency range between 1 MHz and 2 GHz. The ultrasound is transmitted by a piezoelectric sonic head called transducer. The transducer sends a very short ultrasonic pulse (T < 3ns) into the sample. This pulse gets absorbed, scattered, and reflected for example by inhomogeneities and inclusions. The reflected part of the pulse is now detected by the transducer which can function as a detector too. The main characteristics of the reflected signals are amplitude, phase, and duration of the signal. All the characteristics are enhanced by an electrical amplifier and get recorded with an external computer. The sample and the transducer operate in a water bath to minimize the absorption from other acoustic waves. To generate a lateral image the transducer moves with a mechanical scanning unit in x- and y direction above the

sample. The ultrasonic waves are reflected at the inner and outer boundaries. At these boundaries the contacting materials can be detected because the acoustic impedance is distinguishing [10]. This is important for the analysis of TLPS soldered samples, because it gives the opportunity to constitute the different layers precisely and non-destructivly. This is not possible with standard X-ray because of the copper core of the preform.
In this investigation the main quality criterion is the connecting surface on the DCB. This surface should be as void free as possible to have a proper connection between the die and the substrate.

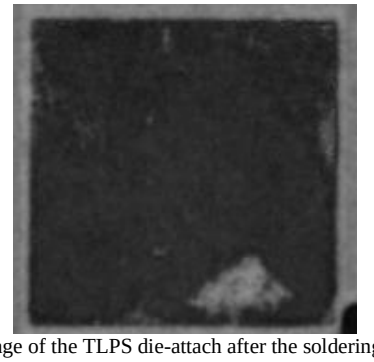

Fig. 2 SAM image of the TLPS die-attach after the soldering process

In Fig. 2, the connecting surfaces are good to see in dark grey and nearly consistent. Only one bigger void is visible under a die (light grey). To measure the amount of the surface connection under the dies an image processing program (ImageJ) is used. The measurement can be done by standard processes. Therefore, a threshold gets set and separates the dark from the bright areas in the pictures. To analyze the areas properly the picture needs to be binarized. The dark areas are colored white while the bright areas are colored black. The white connecting surface must be cut out separately and can be analyzed by ImageJ itself. The program counts the black pixels in the chosen area and recognizes if the pixels are linked. Amount, size, and proportion of voids can be measured very quickly in this way. To generate a plausible range of values it is necessary to set the right scale before the measurement starts.

III. Results

A. Analysis of the voiding after diffusion soldering with standard parameters

After the soldering process of the preform based Sn-Cu-Sn die-attach with standard parameters and no mechanical pressure the percentage of the void is measured to be more than 15 %. With paste-based Sn-Cu transient liquid phase diffusion soldering materials void percentages of 10-15% could be achieved in Syed-Khaja (2018) [14]. The high percentage of voids for the standard parameters could be explained by the different thermal expansion coefficients of the dies and the DCB substrate which results in warpage. During the soldering the warpage of the components is formed in different ways which generates a gap. This gap cannot be balanced by the thin liquid tin layers. As a result, the connected and unconnected die-attach areas occur. The connected areas are partially wetted with solder and the IMC starts growing during soldering process. The unconnected areas could be detected as voids after the soldering process. To counteract the warpage of the components mechanical pressure is applied on the die via a stamp.

B. Analysis of the voiding after diffusion soldering with standard parameters and mechanical pressure

In order to counteract the warpage of the assembly, a stamp is used to apply mechanical pressure from the top. The stamps footprint is doubled between the two sets and is defined as low to high pressure. First the location and the distribution of the biggest void is analyzed via contour diagrams in Fig. 3. It is used to check whether there is an accumulation of large area of voids in the center of the die due to the warpage. However, no specific accumulation of voids in the center can be determined by low and high pressure, which indicates that the pressure is sufficient to counteract the warpage of the components and to enable an even die-attach connection. All voids are between 5-10%, evenly distributed and located at the edges for both settings.

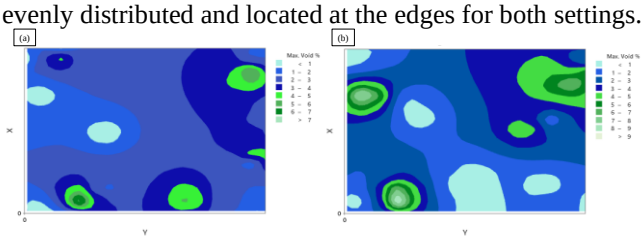

Fig. 3. Contour diagrams with low pressure (a) and high pressure (b)

The influence of the high and low stamp print on the void percentage is illustrated in Fig. 4.

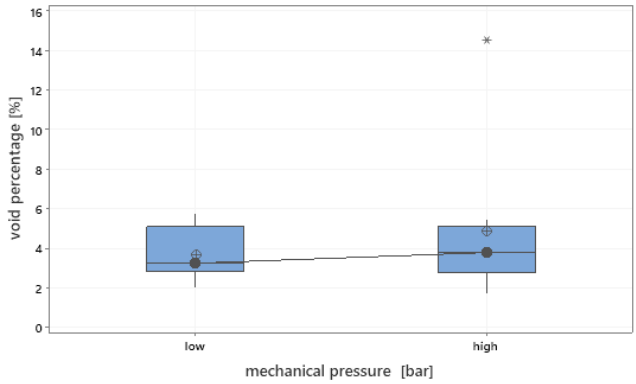

Fig. 4. Boxplot influence of the mechanical pressure on the void percentage

With low pressure an average void percentage of 3.7 % and a value of c_{pK}= 0.86 could be achieved. A doubled stamp

print (high pressure) shows an average void percentage of 4.9% and a lower c_{pK}= 0.32. Increasing the pressure increases the average void percentage and the scrap rate increases from 0.01 % to more than 13%. Therefore, only low pressure is used for further investigations. In addition, the homogenous growth of the IMC at the die-attach with low pressure is shown in Fig. 5.

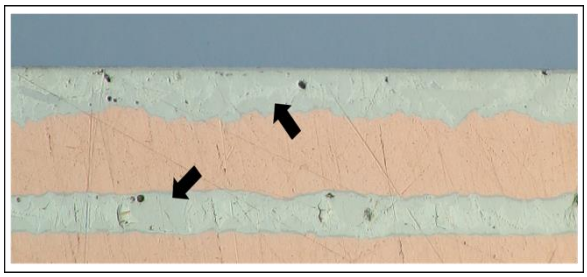

Fig. 5. Grown intermetallic phases during the soldering process.

The layered structure of the die-attach layer is clearly visible. In both tin layers the intermetallic compound phase (IMC) Cu_6Sn_5 are grown over the entire layer via columns. Between the columns phases with a high amount of tin are determined.

C. Influence of selected process parameters on the void percentage

Due to the lower average void percentage the following investigation on the heating gradient, peak temperature and peak holding time are examined under low pressure.

Fig. 6. shows the influence of the void percentage on the maximum peak temperature. The increase of the maximum peak temperature by 6% increases the average void percentage from 3.5 % to 3.8 %. The process capability (c_{pk}) increases from 0.85 (low) to 0.87 (high) and thereby lowers the scrap rate due to the reduced standard deviation (Tab.1). The concentration of the solved copper in tin is temperature and time dependent. By constant holding time the higher peak temperature increases the solubility of copper in tin and the wetting behavior of the liquid tin on the interface materials, which has a positive impact on the equal intermetallic phase growth during the soldering process [7,11].

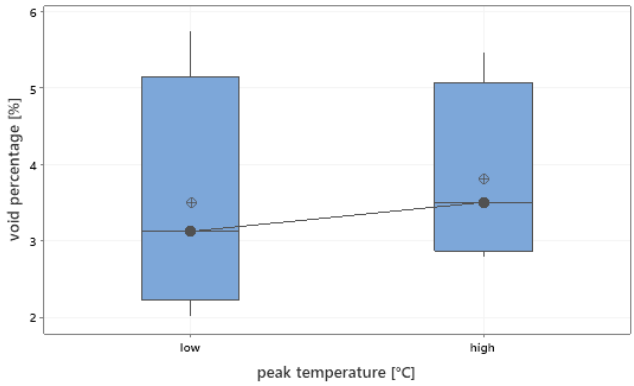

Fig. 6. Boxplot influence of the peak temperature on the void percentage

By doubling the peak holding time the average void percentage decreases from 3.7 % (c_{pK}=0.78) to 3.5 % (c_{pK}=0.84) as shown in (Fig. 7). Due to the longer peak holding time the tin phase is well saturated, when the even growth of the intermetallic compounds starts with isothermal solidification [7,11].

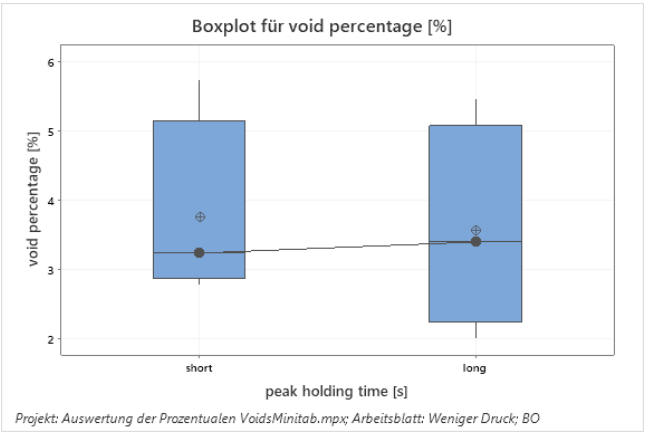

Fig. 7. Boxplot influence of the peak holding time on the void percentage

The influence of the heating gradient on the void percentage is shown in Fig. 8. The reduction of the heat gradient causes a decrease of the average void percentage from 4.6 % (with a c_{pK}=0.76) to 2.7 % (with a c_{pK}=1.1). The slow heating induces less thermo-mechanical stress in the assembly and less warpage. In addition, the wetting of the liquid tin at the interfaces is equal and the copper can be solved steady, which indicates in the low average void percentage of 2.7 % and the high c_{pK} value of 1.1 [7,11].

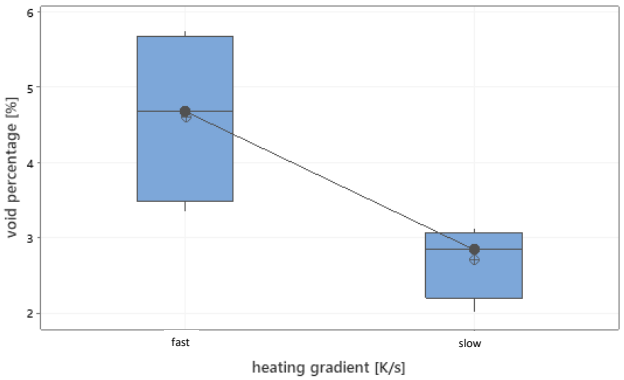

Fig. 8. Boxplot influence of the heating gradient on the void percentage

Table 1: Results of the selected process factors under low mechanical pressure for the average void percentage, the standard deviation and the c_{pK} value.

		Average void percentag	standard deviation	c_{pK}
peak temperature [°C]	low	3.5	1.6	0.85
	high	3.8	1.2	0.78
peak holding time [s]	short	3.7	1.4	0.78
	long	3.5	1.5	0.84
heat gradient [K/s]	fast	4.6	1.1	0.76
	slow	2.7	0.5	1

The investigations on the influence of selected TLPS process parameters for the minimum void percentage with low mechanical pressure shows that the lowest average void percentage could be achieved with 2.7 % by the slow heat gradient. The highest average void percentage under low pressure is achieved by the high heating gradient with 4.6 %. Using the process capability value c_{pK} the measured values of the average void percentages of the selected process parameters could be set in relation to the expected scrap rate. The average void percentage of a high heating gradient, a short holding time and a low peak temperature determines the lowest c_{pK}=0.7. The combination of a slow heating gradient, long holding time and high peak temperature improve c_{pK} value to 1 by having a low average void percentage.

IV. Conclusions

For the transient liquid phase solder material Sn-Cu-Sn selected process parameters are investigated via the average void percentage. To improve the wettability and to counteract the warpage a mechanical pressure is applied with a stamp. The application of a mechanical pressure lowers the void percentage of the die-attach layer below 10%. Two different pressures are applied on the samples and the results indicate lower average void percentages for lower pressure. The applied low pressure is sufficient to counteract the warpage of the components thereby improves wetting of the interface surfaces, so that the value of the average void percentage drops below the 10 % limit. In the next step the influence of the selected process factors on the void percentage are examined under low pressure. Due to higher peak temperature and longer holding time the solubility of copper in tin increases equally and shows a lower void percentage. The heating gradient has the most significant impact on the void percentage. With a slower heating gradient, the thermomechanical stress decreases by increasing the solubility and the average void percentage can be reduced by more than 50%. The investigation hints at the possibility that while using a combination of the best process parameters process capability values of 5 could be reachable indicating very low scrap rates. Further investigations are focused on widening of the statistic bases, process development and analysis of the grown microstructure.

References

[1] R. J. Klein Wassink, Weichlöten in der Elektronik. Saulgau/Württ. 1991, pp. 24-256
[2] EuropäischesParlamentundRat, RICHTLINIE 2011/65/EU, Brüssel: EUR-Lex, 2011.
[3] Heraeus, Alloy Properties Table https://www.heraeus.com/media/media/het/doc_het/products_and_solutions_het_documents/solder_materials_docs/Alloy_Composition_Table.pdf
[4] V.-R. Manikam, K.Y. Cheong, Die Attach Materials for High Temperature Applications: A Review, IEEE Transactions on Components, Packaging and Manufacturing Technology, Vol. 1 No.4, April 2014
[5] H. Bell, Reflowlöten. Bad Saulgau. 2005, pp. 13-186.
[6] A. Syed Khaja, C. Kaestle, A. Reinhardt, J. Franke, "Optimized Thin–Film Diffusion Soldering for Power–Electronics Production". 2014
[7] C. Ehrhardt,M. Hutter, H. Oppermann, "K.-D. Lang, A Lead Free Joining Technology for High Temperature Interconnects Using Transient Liquid Phase Soldering". 2014
[8] A. Syed-Khaja, A. Klemm, T. Zerna, J. Franke "Characterization and Optimization of Sn-Cu TLPS Interconnects for High Temperature Power Electronics through In-Situ-X-Ray Investigations". 2016
[9] A. Syed-Khaja, J. Franke, Investigation on Advanced Soldering Mechanisms for Transient Liquid Phase Soldering (TLPS) in Power Electronics, IEEE 2014
[10] J. Bauch und R. Rosenkranz, Physikalische Werkstoffdiagnostik. Dresden. 2016, pp. 95-100
[11] C. Ehrhadt, Transient Liquid Phase Soldering als Verbindungstechnik leistungselektronischer Halbleiter für Hochtemperaturanwendungen, PhD. Dissertation, Fakultät IV – Elektrotechnik und Informatik der Technischen Universität Berlin 2017
[12] J.-M. Wang, K-J. Wang, J.-G. Duh, Cu Substrates with Different Grain Sizes, J. Electron. Mater., vol.40, no.7, pp. 1549-1555, 2011
[13] W. Choi and H. Lee, Efect of soldering and aging time on industrial microstructure and growth of intermetallic compounds between Sn-3.5 Ag solder alloy and Cu substrate, J. Electron. Mater., pp. 1207-1213, 2000
[14] A. Syed-Khaja, Diffusion Soldering for High-temperature Packaging or Power Electronics. FAU Studien aus dem Maschinenbau Band 315. Erlangen