

Impact of FCBGA substrate stack-up on BLR performance

Jaimal Williamson¹, Yutaka Suzuki¹, and Ron Eller²
Texas Instruments, Inc.
12500 TI Boulevard
Dallas, Texas, 75243, U.S.A.

¹Worldwide Semiconductor Packaging
²Worldwide Quality and Reliability Engineering
Email: jaimal@ti.com

Abstract

Board level reliability (BLR) temperature cycling is a metric for FCBGA field performance, where it is imperative to understand process variation holistically covering both substrate and / or assembly manufacturing process and its impact to product margin. This study focuses on technical reasoning a common FCBGA design manufactured with an identical substrate material set (i.e. core, dielectric, solder mask), assembly bill-of-materials (i.e. underfill, lid, etc.) and assembly site demonstrated different cycles to first failure during BLR testing. Although results far exceeded JESD22-A104 condition G requirements, BLR performance based on identical substrate designs (manufactured at different points in time) proved TV1 (test vehicle 1) performed ~2x better than its TV2 (test vehicle 2) counterpart. To elucidate the primary factor of the disparity in BLR performance, supplier feedback as well as a detailed package construction analysis ensued to compare build-up substrate layer thickness dimensions between TV1 and TV2. Discovery demonstrated a slightly larger volume of a specific layer in the build-up stack within TV2 that generated a higher degree of out-of-plane displacement as compared to TV1. Reproducing the cycles to first failure with the superior TV1 device via the TV1a and impact of substrate warpage was investigated as a factor in the BLR findings driving root cause.

Key words

Board level reliability (BLR), dielectric thickness, Flip chip ball grid array (FCBGA), substrate, warpage

I. Introduction

Flip chip ball grid array (FCBGA) packaging has revolutionized the semiconductor industry because of its inherent high-performance attributes of improved electrical integrity due to shorter interconnects and efficient heat dissipation as the entire backside of the silicon is available for thermal management. As such, FCBGA packages have proliferated into high volume manufacturing (HVM) for a myriad application including automotive, wireless, industrial, aerospace and defense to name a few. Specific to automotive applications, OEMs require semiconductor components to achieve a survival life span upwards to 15 to 18 years [1], [2]. As a result, it is pivotal to establish a robust HVM supply chain to ensure continuity of supply with robust quality and reliability meeting or exceeding the AEC-Q100 automotive standard [3]. Establishing continuity of supply across multiple suppliers requires a fundamental understanding of the packaging material set in terms of its

dynamic material properties over a temperature range and its impact on chip-to-package interaction (CPI). Since FCBGA devices consist of mainly an organic composite material set (e.g. core material, build-up dielectric material, and solder mask) having a keen understanding of the time-dependent viscoelastic material properties as a function of temperature is a key aspect to establishing confidence in the CPI performance during board and component level reliability. Previous work highlighted how BLR performance can be impacted by changes in substrate coefficient of thermal expansion and is expanded further in this study [4].

This paper presents a scenario where BLR results were compared from a FCBGA device having an *identical* package structure and design (e.g. build-up stack, copper density between layers), packaging material set (i.e. both substrate and assembly bill-of-materials), and common assembly site. The aforementioned similarities were common between the two test vehicles evaluated during BLR with the lone difference being substrate supplier. Throughout

this paper the two test vehicles forming the basis on this study are referred to as TV1 and TV2 and is detailed in section II. Despite FCBGA substrate designs being common, TV1 performed $\sim 2\times$ better than its TV2 counterpart at cycles to first failure.

To identify root cause of the BLR disparity, additional BLR temperature cycling testing was repeated with a specially designed test vehicle referred to as TV1a. TV1a has the same substrate supplier as TV1. TV1a was manufactured closely matching the build-up stack of the aforementioned TV2 part with inferior BLR results. The JESD22-A104 condition G BLR testing was repeated with TV1a parts, where empirical results demonstrated similar cycles to first failure as TV2 affirming the substrate supplier manufacturing contribution. Stress modeling was supplemented to understand inelastic strain energy density contributions to the failure mode as a function of the TV1 and TV2 substrate build-up layer differences measured. Modeling simulation results and Weibull analysis further aided the elucidation of the primary factor driving disparity in BLR performance and detailed in the results and discussion section.

II. Description of BLR test vehicle and test conditions

The form factor investigated in the study is a lidded FCBGA as depicted in figure 1. Its package attributes are as followed:

- 24mm x 24mm body size at 0.8mm pitch
- 400 μm core thickness and 3/2/3 build-up stack
- Substrate bill-of-materials (i.e. core, dielectric, and solder mask) consistent with FCBGA HVM material set

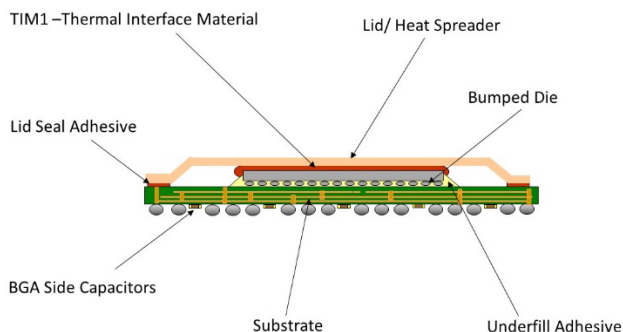


Figure 1: Example of lidded FCBGA device

All test vehicles stated in this paper are daisy-chained and designed to facilitate *in-situ* BLR monitoring isolating both 1st and 2nd level interconnect failures as well in any in package / substrate failure. BLR testing was based on JESD22-A104 condition G, soak mode 4 conditions. The

FCBGA test vehicles were mounted to an 8-layer BLR test board with thickness of 1.57mm. SMT process and conditions were consistent with common industry practices. Failure criteria was enabled using an event detector, where failure was defined by first interruption for a specified period of nanoseconds and increase in daisy chain resistance to a specified ohmic value and followed by nine or more interruptions within a specified percentage of the cycles to first failure. BLR testing was carried out to obtain BGA solder joint characteristic life at 63.2% fails, but differences in first cycles to failure is focus of this paper.

III. Results and Discussion

A. Initial BLR findings

The following test vehicle details, as showcased in figure 2, compare differences between TV1 and TV2. As listed in the figure 2 the lone difference is the substrate supplier with all other variables fixed. BLR was run simultaneously across TV1 and TV2 where results proved the 1,000 cycles requirement as specified per JESD22-A104 condition G, soak mode 4 was far exceeded. However, the focus of this study is to understand what caused a wide variation in first cycles to failure between TV1 and TV2, which manifested itself during BLR testing. Refer to figure 3 for an illustration of the differences in first cycles to failure.

Device	Substrate supplier	Substrate / Assembly BoM	Substrate design	Build up stack tolerances
TV1	A	same	same	same
TV2	B	same	same	same

Figure 2: Comparison between TV1 and TV2

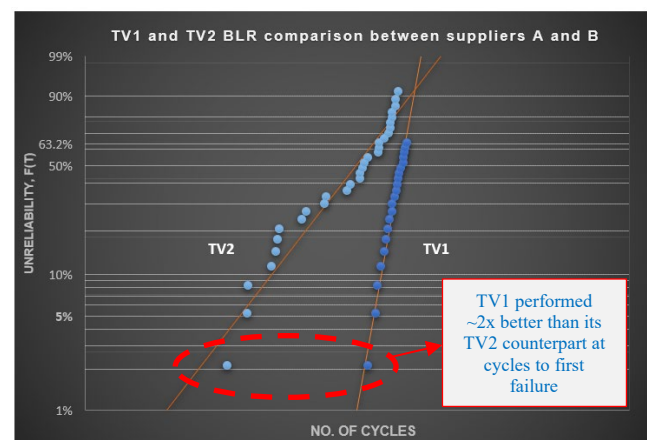


Figure 3: BLR comparison between TV1 and TV2

Figure 3 shows Weibull information is redacted for publication purposes but indicate TV1 parts nearly

producing a 2x improvement in first cycles to failure *in package* as compared to TV2 based on *in situ* BLR monitoring. The failure mode was an in-package failure driven by out-of-plane displacement during the temperature cycling. The fact that a non-2nd level interconnect failure transpired, which did not fit the norm, launched a series of investigations.

B. Initial shadow moiré comparison

The BLR performance between TV1 and TV2 initiated a series of development actions to elucidate what factors contributed to differences in first cycles to failure. The first course of action was to measure bare substrate warpage at both the C4 die area and substrate unit level as received from the substrate supplier. Shadow moiré was performed on the bare substrate in the dead bug configuration ramping from a temperature range of 25°C to 245°C simulating a typical Pb free reflow profile. Figure 4 presents data comparing die area warpage between TV1 and TV2, where results show a statistical difference as measured at 245°C (i.e. simulating peak reflow temperature). TV2 parts clearly show warpage values encompassing a wider spread signifying a higher degree of variation. Likewise, warpage at the substrate unit level was compared as illustrated in figure 5. A similar trend was measured in that wider spread of warpage values was evident with TV2 parts having more sporadic results. Warpage results as measured in both C4 die area and substrate unit level exhibited a concave shape or negative warpage.

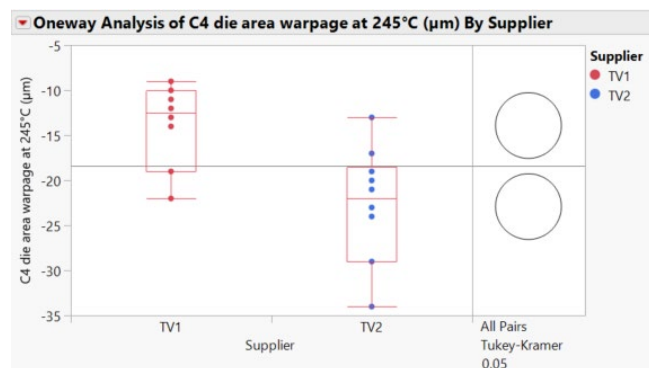


Figure 4: Die area warpage at 245°C comparison between TV1 and TV2

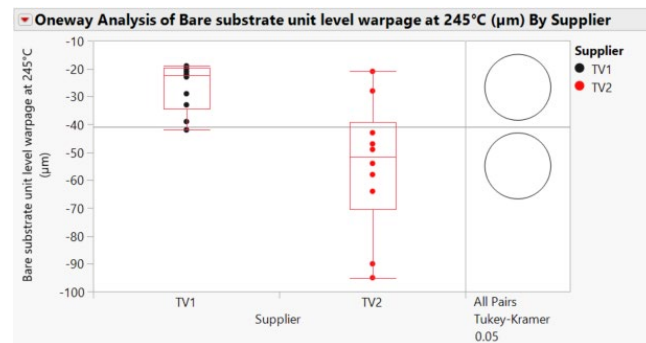


Figure 5: Bare substrate unit level warpage at 245°C comparison between TV1 and TV2

C. A review of package construction analysis

The next course of action was to perform package construction analysis between TV1 and TV2 to better understand any variation of the tolerances in the individual substrate layers that contributed to the warpage differences. The aforementioned concavity of warpage in both the die area and substrate unit provided a clue in terms of what material to focus in the FCBGA build-up stack. For example, based on the fundamentals of polymer chemistry, polymers like epoxies used for dielectric materials within the FCBGA substrate undergo shrinkage during cure [5]. Shrinkage is compounded upon cooling as CTE mismatch generates warpage. In this particular case, the package construction analysis revealed an asymmetry of dielectric thicknesses above and below the substrate core. As the dielectric material shrinks, the side of the core with a higher volume of material bended preferentially towards that side of the substrate. Figure 6 presents a normalized view of the asymmetry in the dielectric thickness within the TV2 FCBGA substrate:

Substrate layer	Dielectric thickness
Layer 1	1
Layer 2	0.91
Layer 3	1
Layer 4	N/A core layers
Layer 5	N/A core layers
Layer 6	0.91
Layer 7	0.91
Layer 8	0.91

Figure 6 presents a normalized view of the asymmetry in the dielectric thickness within the TV2 FCBGA substrate

To prove asymmetry of the substrate dielectric layers caused the concave warpage shape and early first cycles to failure in TV2, adjustments were made in the substrate supplier B manufacturing process to counterbalance the asymmetric layers above and below the substrate core. Figure 7 represents the adjustments made during substrate supplier B manufacturing to counter the warpage with the more balanced (symmetrical) substrate layers.

Substrate layer	Dielectric thickness
Layer 1	1
Layer 2	0.91
Layer 3	0.91
Layer 4	N/A core layers
Layer 5	N/A core layers
Layer 6	1
Layer 7	0.91
Layer 8	0.91

Figure 7 presents a normalized view of the dielectric thickness within the more balanced FCBGA substrate

To validate the theory of improving symmetry / balancing above and below the core, empirical data obtained via shadow moiré was repeated at bare substrate level to compare warpage and any hysteresis effect between the balanced substrate and TV2 from 25°C to 260°C. This was analyzed to understand any reduction in concavity ratio of the substrate. Results are compared in figure 8, which compares the deviation in warpage at 25°C after heating and before heating.

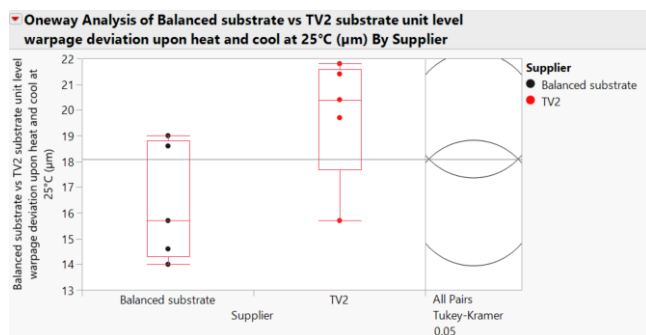


Figure 8: Warpage deviation at 25°C before and after heating

Results indicated no statistical difference in warpage, but

the ratio of parts exhibiting concavity reduced ~ 10%. The trend for lower degree of hysteresis infers a lesser degree of package displacement during BLR testing.

D. Confirmation BLR testing comparing TV1a head-to-head with TV2 and validation of root cause

To corroborate this theory, BLR testing was repeated through JESD22-A104 condition G specification with TV1a parts specially manufactured with dielectric thickness values with similar asymmetry above and below core similar to TV2. The goal was to study if first cycles to failure would be similar to TV2 results as depicted in figure 3. The basis of the design of TV1a test vehicle, was to elucidate root cause of the BLR disparity at first cycles to failure between TV1 and TV2.

Examining the BLR results in figure 9, TV1a was found to be within 1% of first cycles to failure to TV2 reinforcing the importance of controlling the symmetry of the dielectric volume above and below the core.

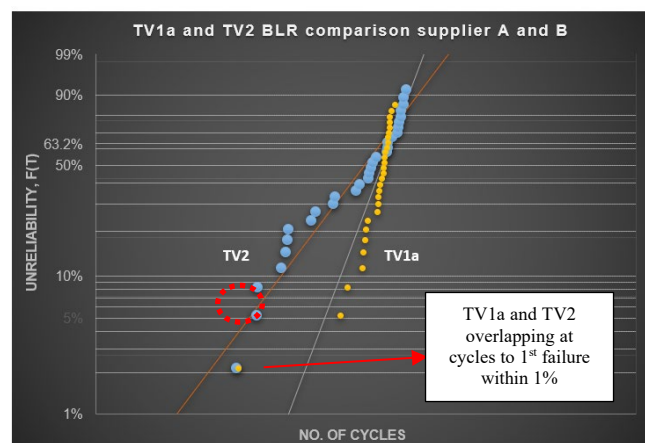


Figure 9: BLR comparison between TV1a and TV2

E. Stress modeling simulation

To build on the empirical findings, thermo-mechanical simulation was carried out using Finite-Element-Method (FEM) models with ANSYS to build on the materials science understanding of the BLR output. Fig. 10 shows the example of mechanical modeling.

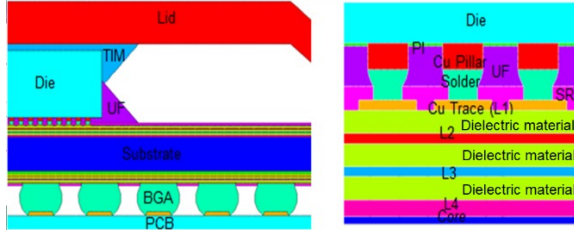


Figure 10: Example of thermo-mechanical simulation

To capture the rate-dependent plasticity of solder material, L. Anand [6] proposed the rate-dependent plasticity based on the improvement of Garofalo model. This model is called Anand's viscoplastic constitutive model. This model has been widely used in the semiconductor industry to evaluate solder crack risk under reliability tests. Material constraints of Anand's viscoplastic constitutive model can be fitted to the strain rate and steady-state stress tests based on equations (1) and (2), and related strain hardening material parameters can be fitted based on (3) and (4) data based on stated equations. The associated constraints are listed in figure 11.

$$\frac{d\epsilon^p}{dt} = A \exp\left(-\frac{Q}{RT}\right) \left[\sinh\left(\frac{\zeta\sigma}{s}\right) \right]^{1/m} \quad (1)$$

$$\sigma^* = \frac{s}{\zeta} \left\{ \frac{1}{A} \frac{d\epsilon^p}{dt} \exp\left(\frac{Q}{RT}\right) \right\}^m \sinh^{-1} \left[\left\{ \frac{1}{A} \frac{d\epsilon^p}{dt} \exp\left(\frac{Q}{RT}\right) \right\}^n \right] \quad (2)$$

$$\frac{d\sigma}{d\epsilon^p} = ch_0 \left(1 - \frac{\sigma}{\sigma^*}\right)^a, \quad \sigma = c s, \quad \sigma^* = c s^* \quad (3)$$

$$c \equiv \frac{1}{\zeta} \sinh^{-1} \left[\left\{ \frac{1}{A} \frac{d\epsilon^p}{dt} \exp\left(\frac{Q}{RT}\right) \right\}^m \right] \quad (4)$$

Pre-exponential factor	A (s ⁻¹)	717.26
Activation energy/Boltzmann's constant	Q/R (/K)	6067
Multiplier of stress	ζ	2
Strain rate sensitivity of stress	m	0.13
Coefficient for deformation resistance saturation value	$\bar{s}$ (MPa)	29
Strain rate sensitivity of saturation value	n	0.0436
Hardening constant	h0 (Mpa)	14560
Strain rate sensitivity of hardening	a	2.22
Initial value of deformation resistance	s ₁ (MPa)	2.45

Figure 11: Material constants of Anand's viscoplastic constitutive model

In addition, the thermomechanical properties of thermosetting epoxy-based mold compounds (for example) are sensitive to temperature and strain rate. Dielectric material was considered to be thermo-rheological simple viscoelastic materials. The generalized Maxwell model-based viscoelastic behavior was used to input parameters for dielectric material to capture the rate-dependent elastic behavior. The viscoelastic behavior of the kth element of the

generalized Maxwell model can be obtained, and total stress is given by summing the solutions of (6) up to $k=n$. The parameters in the equation above are calculated from the dynamic viscoelastic experiment. The experiment is the dynamic response, dynamic-mechanical-analysis (DMA) with frequency / temperature sweep was conducted to estimate the rate-dependent elastic properties with the Prony series, thus a strain is given,

$$\frac{d\epsilon_k}{dt} = \frac{1}{G_k} \frac{d\sigma_k}{dt} + \frac{\sigma_k}{\eta_k} \quad (5)$$

$$\sigma = \epsilon_0 G(t) = \epsilon_0 G_\infty + \epsilon_0 \sum_{k=1}^n G_k \exp(-t / \tau_k) \quad (6)$$

$$\epsilon = \epsilon_0 e^{i\omega t} \quad (7)$$

After substituting the Eq. (7) into Eq. (6), the evolution equation for $\sigma(t)$ can be written as:

$$\sigma(t) = \left\{ G_\infty \epsilon_0 + \sum_{k=1}^n G_k \epsilon_0 \frac{i\omega \tau_k}{1 + i\omega \tau_k} \right\} \exp(i\omega t) \quad (8)$$

$$G'(\omega) = G_\infty + \sum_{k=1}^n G_k \frac{\omega^2 \tau_k^2}{1 + \omega^2 \tau_k^2} \quad (9)$$

$$G''(\omega) = \sum_{k=1}^n G_k \frac{\omega \tau_k}{1 + \omega^2 \tau_k^2} \quad (10)$$

where $G'(\omega)$ is dynamic storage elastic modulus, and $G''(\omega)$ is dynamic loss elastic modulus. Frequency dispersion of specific temperatures is given by using the time-temperature-superposition (TTS) to create the rate-dependent properties at the frequency or time domain from the experimental results of G_∞ , G_k , and τ_k by using the least square method. In ANSYS, G_∞ was automatically calculated from another input parameters. Figure 12 lists the viscoelastic parameters for the dielectric material with the 20 Prony series based on the DMA test result.

	k=1	k=2	k=3	k=4	k=5	k=6	k=7	k=8	k=9	k=10
G_k	1.77E-02	1.64E-02	1.61E-02	1.74E-02	1.81E-02	2.05E-02	2.22E-02	3.57E-02	9.13E-02	1.46E-01
τ_k	4.27E-02	5.51E-01	7.10E+00	9.16E+01	1.18E+03	1.52E+04	1.97E+05	2.54E+06	3.27E+07	4.22E+08
	k=11	k=12	k=13	k=14	k=15	k=16	k=17	k=18	k=19	k=20
G_k	1.62E-01	1.55E-01	9.28E-02	4.87E-02	3.79E-02	2.37E-02	1.75E-02	1.34E-02	7.14E-03	7.14E-03
τ_k	5.45E+09	7.02E+10	9.06E+11	1.17E+13	1.51E+14	1.94E+15	2.51E+16	3.24E+17	4.17E+18	5.38E+19

Figure 12: Viscoelastic parameters with 20 Prony series for dielectric material

The FEM models calculate the inelastic strain energy density called the plastic work density (PWD) in ANSYS as

a failure-sensitive parameter (FSP) to evaluate in package failure associated with a copper material (i.e. non 2nd level interconnect) risk under the BLR temperature cycling test loading. Copper material is regarded as a ductile material that shows plastic behaviors under the higher stress field, and this accumulated plastic work leads to an anomaly with a copper material in package. Equation 10 is the definition of PWD to represent copper damage under the reliability test. PWD is given,

$$PWD = \frac{\sum_{k=1}^n (\sigma_{ij}(k) \delta \epsilon_{ij}(k)) - \sigma_{ij}^2(n) / 2E_{ij}(n)}{V} \quad (10)$$

Figure 13 lists the plastic mechanical properties for the in-package copper material. Figure 14 shows the contour plot of PWD under the BLR TC loading, and figure 15 is the comparison between TV1 and TV2 for the in-package copper failure under the BLR temperature cycling loading. The thermo-mechanical simulation expects that TV1 would show the better BLR temperature cycling performance as compared to TV2.

TEMP (degC)	YIELD_STRENGTH (Pa)	TANGENT_MODULUS (Pa)
-65	9.80E+07	1.83E+10
260	4.70E+07	1.83E+10

Fig 13: Plastic material properties for the in-package copper material

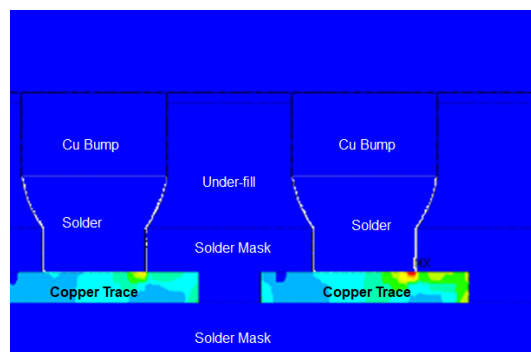


Fig 14: Contour plot of inelastic strain energy density under the BLR TC loading

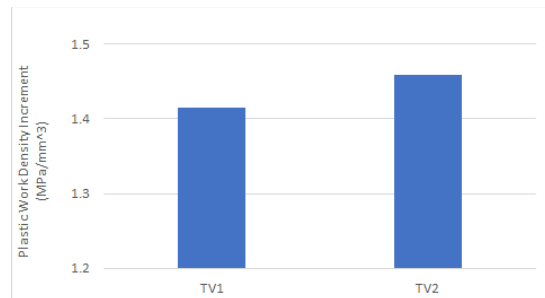


Fig 15: Comparison the in-package copper anomaly risk between TV1 and TV2

IV. Conclusion

This investigation revealed the sensitivity in dielectric thickness variation between TV1 and TV2 on BLR performance at first cycles to failure. TV2 exhibiting an asymmetry in dielectric thickness above the core material versus below the core caused warpage in a concave shape. This variation was found to be a deleterious effect on BLR performance as compared to TV1. The concavity initiated a failure of a copper material in-package. TV1 with its superior BLR performance was specially manufactured as TV1a to mimic the asymmetry of TV2 and reproduce the in-package BLR failure. Based on the modulating the dielectric thickness in TV1a, BLR results proved TV1a can match TV2 at first cycles to failure. Stress modeling simulation validated higher plastic work density in TV2 enabling a correlation with the empirical BLR results.

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