Glass Substrate for Co-Packaged Optics

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Abstract
Co-packaged optics leads to significant power reduction by placing the electronic and photonic chiplets in a single package. An integrated electro-optical substrate made of glass with optical waveguides, through vias and electrical redistribution layers inside a single-sided cavity enables fine-line electrical routing and low-cost assembly. Existing glass and thin film technologies were evaluated and combined into a single process stream including photonic assembly. Photonic chips with silicon nitride waveguides were optically coupled to integrated low-loss (<0.1 dB/cm) glass waveguides with minimum loss of 0.65 dB achieved by fiducial alignment and pick-and-place assembly.

Key words
Evanescent Coupling, Flip Chip Assembly, Integrated Waveguides, Laser Singulation, Through Glass Via

I. Introduction
A decade ago, co-packaged optics based on multimode optical links were deployed for high-performance computing (HPC) applications [1]. Multimode optical engines with discrete components were demonstrated using glass carriers assembled on a common organic packaging substrate [2]. With advanced silicon photonic transceiver technology [3] the motivation continues to minimize the length of the electrical link for significant power reduction and increased bandwidth. In addition to HPC, the main drivers are datacenter networks, artificial intelligence, and machine learning. The heterogenous integration of electronic integrated circuits (IC) and photonic integrated circuit (PIC) transceivers onto a common package substrate reduces the electrical interconnect loss by decreasing the required reach. This trend is supported by the chiplet technology [4] and the creation of an interconnection standard for connecting different chiplets together [5]. The use of photonic interposers for 2D or 3D integration for driving electronic ICs with PICs will further improve power efficiency, particularly for high channel count cases. However, there are significant electrical, thermal, and mechanical packaging challenges, particularly resulting from large multi-chip substrate sizes hosting many chiplets. New materials and assembly approaches are needed for: low loss and power efficient high-speed electrical interconnects; thermal management of high-power consumption electrical ICs on the same substrate as temperature sensitive PICs; low substrate warpage, and high electrical reliability of chip-to-package substrate bumps/pillars and substrate-to-board ball grid array (BGA). Glass has a unique combination of properties that makes it well-positioned to overcome these co-packaging challenges with the additional capability to integrate optical interfaces for pick-and-place assembly of PICs. The approach in this work consists of using a single glass substrate where the top redistribution layers (RDLs) connect high-speed electrical lines between the electronic IC and the PICs along with through glass vias (TGV) to provide power and ground. The single layer provides simpler fabrication and assembly compared to a 2.5D silicon interposer on an organic substrate or an embedded multi-die interconnect bridge configuration [6] and as such, has the potential for lower overall packaging cost. Ion-exchanged (IOX) optical waveguides with propagation losses of less than 0.1 dB/cm are located underneath the top surface of the glass. The RDL and electrical bumps are inside the cavity to minimize the distance between PIC evanescent couplers and IOX waveguides. The cavity was made by etching 50 µm into the glass to allow enough clearance underneath for the RDL and the electrical bumps. TGVs were formed in glass to connect the top surface inside the cavity with the bottom surface of the glass substrate. TGVs were etched to an

entrance opening of 100 µm and placed with 250 µm spacing inside the cavity. A schematic cross-section view of different steps in the process flow is shown in Fig. 1, starting with IOX waveguide fabrication, cavity and TGV formation, metallization, PIC and connector (MPO-16 guide pin) assembly.

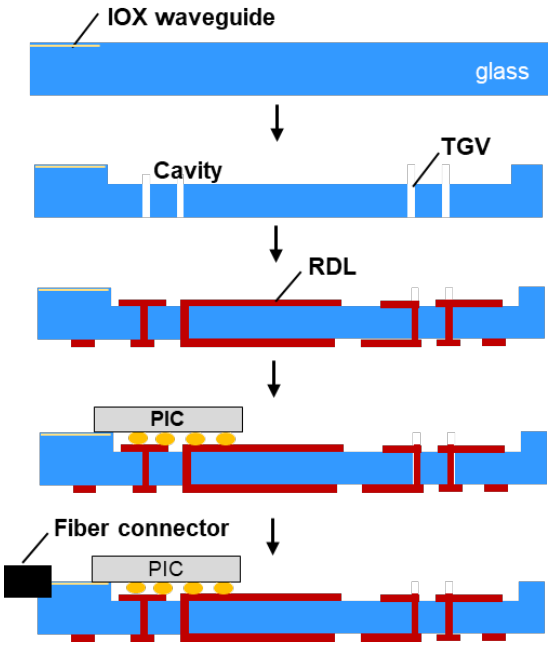

Fig. 1. Process flow of glass substrate fabrication.

II. Ion-exchanged Waveguides in Glass

Integration of planar waveguides below the glass surface was achieved by a two-step thermal ion-exchange process sequence. The waveguides were designed to match the mode field of a Corning® SMF-28® Ultra Optical Fiber at 1310 nm. The propagation loss was demonstrated to be <0.1dB/cm at wavelength of 1310 nm [6]. For this work, the ion-exchanged waveguides fabricated a core refractive index approximately 5×10^{-3} higher than the surrounding glass cladding. Single-mode fiber coupling loss to the IOX waveguides depends on the top layer index and is calculated to be 0.3 (0.6) dB for air and 0.1 (0.2) dB for index-matched adhesive top cladding at 1310 (1550) nm wavelength. The waveguide positions and alignment marks are defined lithographically in the same process step to enable the accurate alignment of PICs. Different sizes of IOX waveguide samples can be made. Figure 2 shows the size of 75 mm × 75 mm packaging substrate with integrated waveguides, while Fig. 3 depicts a sample of 3.8 mm × 10 mm in size with lithographically defined fiducials for direct chip assembly.

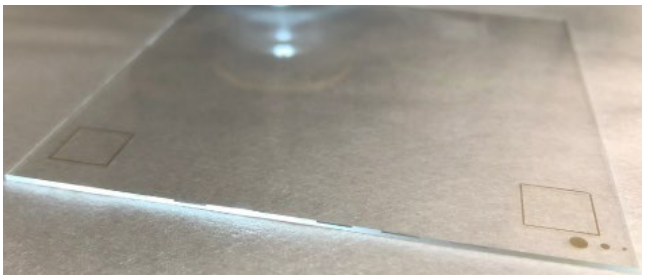

Fig 2. 75 mm × 75 mm × 0.7 mm glass waveguide sample.

Fig 3. Top view image for 3.8 mm × 10 mm × 0.7 mm glass sample with fiducials and an array of 12 waveguides.

III. Cavity and Through Glass Via Integration

For interfacing the photonic chip with the IOX waveguides at the glass surface, the RDL needs to be embedded below the surface of the glass where the IOX waveguides will connect optically with the PIC. This can be achieved by etching a cavity with a depth that is the same as the total thickness of the RDL and the height of the electrical bumps or pillars after bonding. The cavity was defined to be 50 µm for this experiment. After integration of the IOX waveguides, the position of the TGVs and the cavity was aligned to the lithographically defined fiducials from the IOX process. A mask was applied to the surface of the glass to protect the IOX waveguides during the TGV and cavity chemical etching process. Figure 4 and Fig. 5 show glass test samples of 75 mm × 75 mm and 25 mm × 24 mm, respectively. The TGV opening width is measured to be ~ 100 µm on both sides.

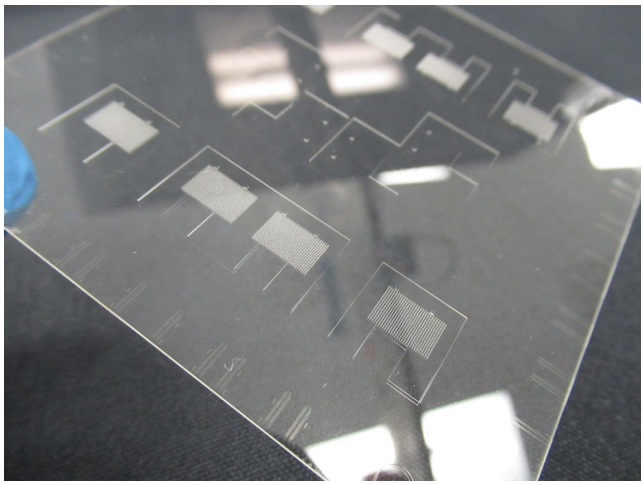

Fig 4. 75 mm × 75 mm glass substrate with IOX waveguides, 10.5 mm × 11 mm U-shaped cavities, and TGV arrays with 250 µm pitch.

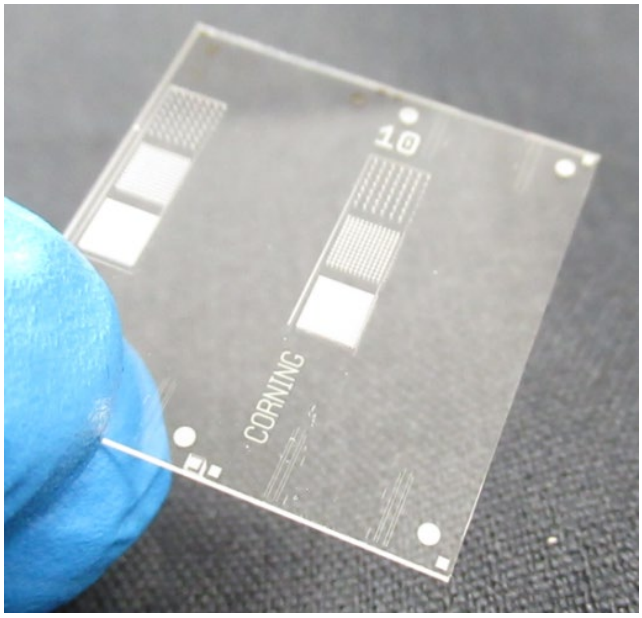

Fig 5. 25 mm × 24 mm glass substrate with IOX waveguides, 11.3 mm × 3.3 mm cavities and TGV arrays with 150 µm, 250 µm, and 500 µm pitch.

The 25 mm × 24 mm sample had TGVs with different pitches of 150 µm, 250 µm, and 500 µm as shown in Fig 6. No cracks or defects were observed between the TGVs. The surface roughness at the floor of the cavity was measured for five different wafers with maximum R_a of 1 nm and R_{max} of 13.9 nm.

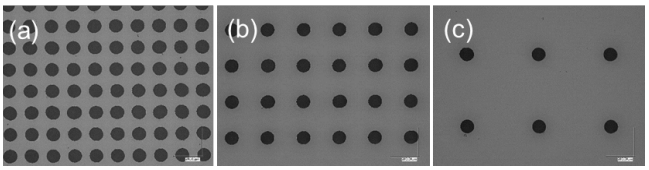

Fig. 6. Top-view optical micrographs of TGVs with (a) 150 µm, (b) 250 µm, and (c) 500 µm pitch formed inside the 50 µm deep cavity.

IV. Electrical Redistribution Layer

Metallization of up to three surface layers in combination with conformal metallized TGVs has previously been demonstrated for glass substrates [8]. However, the fabrication of a RDL inside a cavity needs to be explored by thin film processing. Chrome as adhesion promoter was sputtered before the gold layer deposition. Instead of a spin-coating photoresist, a spray coating resist was selected to apply a uniform film across the 3D surface of the 150 mm wafer with 50 µm deep cavities. A positive acting MicroSpray™ photoresist was applied and mask contact litography performed with gap of 50 µm between the glass surface and floor of the etched cavities. The test pattern consisted of an array of square pads with 100 µm edge length located inside the U-shaped cavities of 10.5 mm × 11 mm in size. The pitch of the pads was 225 µm. The bond pad size after etching and resist removal was measured to be 90 µm due to the large gap resulting in a non-contact lithograph of the positive resist leading to an offset of 5 µm on each side. The process was applied to a glass wafer with integrated IOX waveguides to demonstrate the co-integration of optical waveguides and electrical bonding pads. A top-view of the waveguide array integrated next to the surface of the glass outside the cavity and bonding pads at the floor inside the cavity is shown in Fig. 7. The experiment demonstrates the limitations of contact lithography for accurate transfer of the layout which significantly limits fine-line electrical circuit fabrication inside the cavity. This could be overcome by a high-resolution laser direct imaging system.

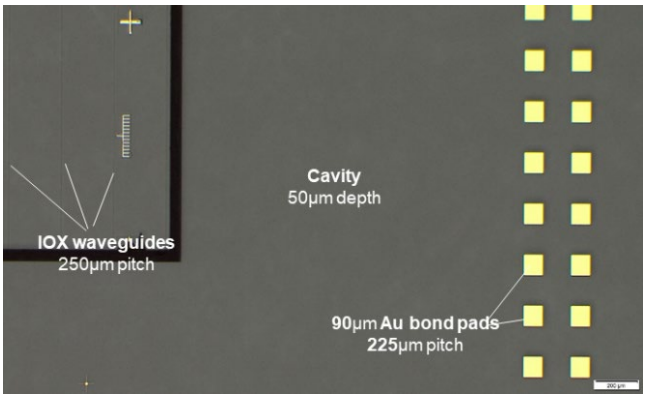

Fig 7. Electrical integration by thin film deposition, spin coating, and contact lithography.

V. Photonic Chip Coupling

Edge and grating couplers are two common methods of interfacing between fiber and on-chip waveguide modes. Evanescent coupling methods to connect fiber modes to on-chip waveguide modes have been demonstrated [9]. Such an approach is scalable to high optical port counts and can be automated by pick-and-place machines. For evaluation of the optical interface and demonstration of low-loss optical coupling between IOX waveguides and PICs, the optical coupling is separated from the electrical interface momentary. Optical layouts were composed of U-shaped waveguide loopbacks with 250 µm pitch for both Si and SiN chips and turns designed to minimize any radiative loss due to bends in the loopbacks. Si chips of size 10 mm × 10 mm were fabricated by AMO GmbH in Aachen, Germany using electron-beam lithography. SiN chips of size 5 mm × 5 mm were fabricated by Ligentec using deep ultraviolet lithography. The optical couplers on both chips were based on linear tapers with different sections to couple both TE and TM modes. At the end of the first short taper section, both TE and TM modes were still well confined in the waveguides with reduced width. Adiabatic linear tapers are used in a ~2-2.5 mm long second section presents fewer parameters and is less sensitive to provide coupling that is robust to variations in the design that accounts for both mode polarizations and over a range of wavelengths, simplifying the initial coupler fabrication process considered in this work. Taper shape optimization, such as that utilized in [6], can be applied to reduce the length of the second stage to 1.0-1.5 mm in the final design.

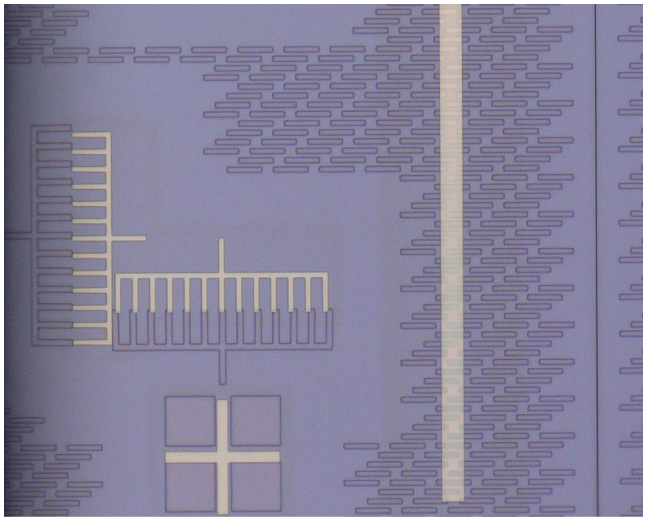

Fig. 9. An optical micrograph of a glass waveguide substrate mounted on top of a SiN chip. The alignment was done by using Vernier fiducials for horizontal and vertical direction. The cross-fiducial is on the IOX glass waveguide sample and the squares are on the SiN chip.

The IOX glass waveguide samples with an array of 12 waveguides with 250 µm pitch were fabricated with fiducials for visual alignment as shown in Fig 9. The samples were aligned to the Si and SiN tapers by a set of fiducials and placed by a FINEPLACER® lambda die bonder. IOX glass waveguide sample and Si or SiN chip have cross and Vernier fiducials for lateral alignment by a split optic. Once both components were aligned, the components were bonded with an adhesive. The vision-based alignment enabled a coupling of all waveguides in a single assembly step and is independent of the number of waveguides. In the present case, all 12 waveguides were aligned in one step. After assembly, the lateral misalignment was measured by an optical microscope to be 3 µm or less. Figure 10 shows a top-view optical micrograph of a SiN chip after assembly.

Fig. 10. Top-view optical micrograph of an assembled IOX glass waveguide substrate on a SiN chip. The width of the smaller IOX sample is 3.8 mm.

In order to measure the bond-line thickness, the protruding IOX glass was laser cut, and the assembly was end-face polished. The adhesive bond-line thickness was measured by optical microscope to be 1 µm or less between the glass surface and the top surface of the Si and SiN chip buried oxide (BOX) layer. Measurements of the assemblies were made using an external cavity tunable laser connected to the odd channels of a 12-channel fiber array unit (FAU) by an optical switch. After aligning the FAU to the assembly, index matching fluid was used to minimize the optical coupling losses. Optical power from the loopback waveguides was measured using an InGaAs photodetector connected to the even ports of the FAU by a separate optical switch. The maximum and minimum loss values of the loopback waveguides were recorded from 1515 nm to 1590 nm as the polarization state was varied across the Poincaré sphere. Losses due to the switches and connectors were calibrated out by separate measurements.

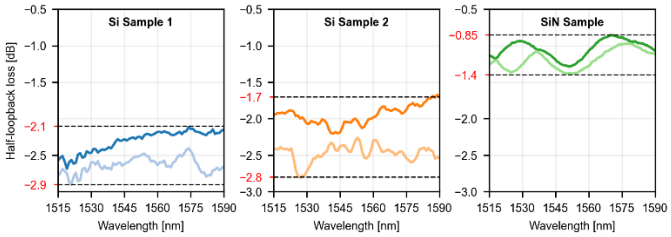

Fig. 11. Half-loopback insertion loss (FAU to IOX glass edge coupling (0.2 dB) + IOX glass to PIC evanescent coupling) measurements across different samples. Lowest and highest loss curves are plotted in dark and light colors, respectively.

Figure 11 which shows measurements across different Si and SiN based assemblies. Variations in adhesive thickness along the evanescent coupling region, misalignments between glass and the PIC, and Si or SiN device layer thickness variations on the PIC are primary reasons for fluctuations in loss values. Additionally, a ~0.2 dB change in insertion loss was observed as the sample temperature was varied between 10-60°C for Si based assemblies. Minimum insertion loss due to evanescent coupling from Si to IOX glass waveguide was measured to be -1.5 dB on "Si Sample 2," after removing 0.2 dB fiber to IOX waveguide edge coupling loss (see Ion-exchanged Waveguides in Glass section for edge coupling loss estimates). Among Si-waveguide-based samples, a minimum roll-off value of 0.8 dB is measured for "Si Sample 1." For the SiN-waveguide-based samples, a minimum insertion loss of 0.65 dB (after removing the IOX waveguide to fiber edge coupling loss) and a roll-off value and 0.55 dB were measured (see "SiN Sample" in Fig. 11).

VI. Optical Fiber Coupling

The successful commercial deployment of glass substrates for co-packaged optics will require wafer- or panel-scale volume production of circuits that will need to be singulated, followed by the low-loss fiber-to-chip coupling. Edge coupling offers broadband, high-coupling efficiency without polarization dependency and was chosen for the present work. However, to minimize coupling losses, edge coupling places the requirement for vertical and optical-quality end-facets which is traditionally achieved by expensive and time-consuming post-processes such as mechanical polishing. Here, a high-speed, non-contact, near-zero kerf-width laser singulation method (Corning® nanoPerforation) was employed to directly singulate glass wafers with optical-quality end-facets [10]. The method employs a quasi-non diffracting beam to create an elongated focal region to selectively modify the entire thickness of the glass substrate (except in the regions around the optical waveguides by gating the laser and/or controlling the laser focal position) in a single pass. When the laser defined contour is separated by a mechanical or thermal stress the unmodified zones give way to mirror-like regions that provide the equivalent low-loss edge coupling when compared to optically polished end-facets. Figure 12 shows a Scanning Electron Microscope (SEM) end-view picture of the separated glass edge with a surface roughness (Ra) of ~1 µm for direct butt-coupling of optical fibers.

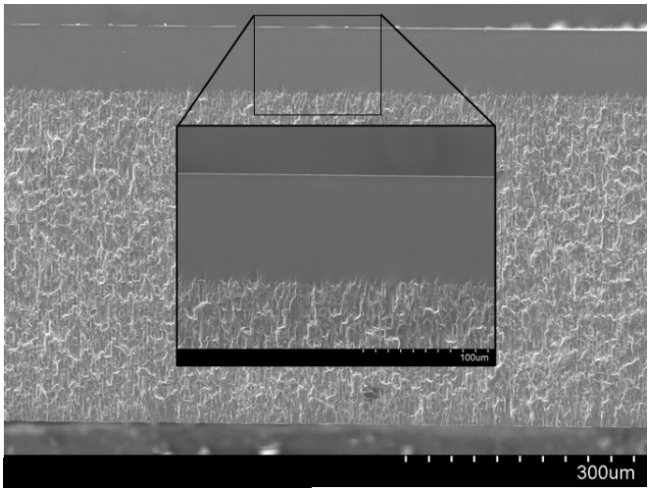

Fig. 12. SEM image and a higher resolution inset of an optical facet (end-view) of laser singulated glass substrate with an optical-quality region for ion-exchange waveguides near the top surface.

For mating with standard MPO-16 connector ferrules, guide pins with 550 µm in diameter were placed inside laser ablated trenches separated by 5.3 mm. The pins were passively aligned in the trench and permanently bonded to the glass together with a glass lid by an adhesive which required a dual cure. First, UV light secures the position of the pins inside the trench which is followed by a thermal cure to increase the thermal stability of the adhesive. Figure 13 shows an example of a 75 mm × 75 mm glass substrate with total of 16 assembled pairs of MPO-16 guide pins. The lowest average connector loss was measured to be 0.5 dB for physical contact [11].

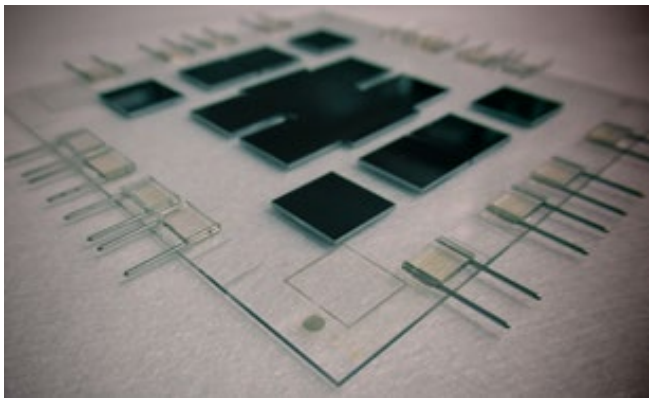

Fig. 13. 75 mm × 75 mm substrate with 16 assembled MPO-16 guide pin interfaces for fiber to glass waveguide butt-coupling at the edges of the glass substrate.

VII. Conclusion

A process for fabricating a glass substrate with ion-exchange optical waveguides, TGVs and electrical interconnects inside a single-sided cavity was discussed for co-integration of electronic and photonic chiplets in a single package. TGV arrays were fabricated with a minimum pitch of 150 µm and opening widths of less than 100 µm in 0.6 mm glass thickness. Thin film metallization inside a 50 µm deep cavity was studied with resolution limitations for contact lithography. Additional work is required to develop a robust spray coating and laser direct imaging technology for a multi-layer RDL in the cavity. Low-loss single-mode optical waveguides were integrated in glass by silver-ion exchange with <0.1 dB/cm propagation loss. Evanescent couplers were designed with lowest loss demonstrated for SiN couplers (0.65 dB) for glass waveguide to chip coupling. The assembly process for PICs is scalable to more than 12 channels and evanescent optical couplers in combination with electrical interface in a robust single assembly step present a promising approach.

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