

A high-uniformity, high-purity copper pillar ECP process with limited acid concentration

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Abstract

The requirements for wafer-level packaging (WLP) are becoming more and more stringent both from a sustainability perspective and process performance. For instance, there is a demand for continuous process improvement for within die uniformity (WID) and operating in a low acid environment for copper pillar plating. Antagonistic these requests are; however, we must devise novel ECP techniques and additive designs to meet such ambitious targets. The additives consist of an accelerator, suppressor, and leveler. The systematic use of Linear Sweep Voltammetry (LSV) aided the study of the electrochemical response to screen the additives and determine the Wagner number (Wa) in the current density region of interest. In addition, the rigorous use of the Design of Experiment (DOE) enabled us to determine the concentrations for combining this new leveler and suppressor with the accelerator. Owing to designing the right leveler and suppressor, we controlled the free acid concentration at 10% (100 g/L) while maintaining the WID below 2.5% and controlling the within-feature (WIF) less than 1 μ m (~2.0%), using a deposition rate of approximately 2.0 μ m/min, to various wafer patterns with various aspect ratios and layouts. Lastly, the resulting film properties are as crucial as ECP performance. SIMS studies support a deficient level of inclusion in the copper film with a total impurity of 3.1 ppm, including C, O, N, S, and Cl. Therefore, when studied with a solder cap, the Kirkendall void performance was outstanding based on minimal voids post 10X reflow cycles and high-temperature storage. The shear stress test measuring the bonding between the copper and its pad on the wafer is 18.4 gf/mil².

Keyword

High uniformity, high-purity Cu pillar; environmentally sustainable, low acid, reliability, WID, WIF, IMC, shear stress, DOE.

I. Introduction

2.5D and 3D packaging schemes advances necessitate higher I/O counts, finer feature size, and tighter pitch requirements [1]. This requirement puts more dependence on the performance and reliability of interconnect materials, such as an electroplated copper pillar. With the demand for this ever-improving uniformity in copper pillar electrochemical plating (ECP), there is a need to develop new additives and techniques to meet those ambitious targets. In addition, health and environmental regulation has imposed another restriction on acid concentration in the plating bath. The specific requirement is acid concentration must not be higher than 10% (weight concentration) to avoid the process safety management registration [2]. While driving toward stronger additive systems for improving pillar height uniformity, bump shape and purity must be kept in check and stay within

health and environmental guidelines. This work describes a newly developed environmentally sustainable acid copper ECP additive system with a little acid concentration of 10% (100g/L). We can apply this high purity, excellent uniformity pillar ECP process with good bump shape control to various wafer patterns with various aspect ratios and layouts. It can achieve < 2.5% within-die coplanarity (WID), < 3.8% within-wafer coplanarity (WIW), and < 1.0 μ m (~2.0%) within-feature bump shape (WIF).

II. Material and methods

A. Plating Chemical, apparatus, and pillar characterization

The basic make-up solution consists of 0.79 M copper sulfate, 1.02 M sulfuric acid (100g/L), and 1.37 mM hydrochloride for chloride ions. We fixed the sulfuric acid concentration as 1.02 M in this study to meet the

requirements of health, environmental and regulatory restrictions. The plating bath includes make-up solutions and organic additives with an accelerator, suppressor, and leveler. In addition, we performed coupon level testing using a mini-cell and the temperature-controlled by a water bath. The anode is an insoluble Titanium anode. We applied a VSP Biologic Potentiostat to perform coupon plating and electrochemical studies and utilized a Nokota tool for whole wafer plating and a Keyence surface profilometer for pillar characterization.

B. Electrochemical study

We utilized linear sweep voltammetry (LSV) to determine the polarization behavior and polarization strength of the additives in the plating bath. The working electrode is a Pt rotating disk electrode (RDE). A Cu plate is the counter electrode, and Hg/Hg₂SO₄ electrode is the reference electrode. The scan rate is 2.0 mv/s, and we scanned the voltage from open-circuit potential (OCP) to -0.9 V (vs. Hg/Hg₂SO₄).

C. Testing wafer layout

We tested the pillar performance on various wafer patterns with different sizes, aspect ratios, and layouts. The critical dimension (CD) of the pillar varies from 30 μm to 60 μm , and the pillar height range is from 15 μm to 40 μm . The open area of the wafer varies from 15% to 4%. The data presented in this paper covers pillars of 60 μm in width, 40 μm in height, and 10.3% open area for the overall substrate.

D. Reliability study

We performed the reflow on a stack with Sn-Ag plated on the top of the Cu pillar. Standard Sn-Ag reflow conditions as 240 °C and 15 sec are applied. High-temperature storage is 150 °C at ambient pressure. We used a dual beam focus ion beam (FIB, Zeiss, Auriga) to analyze the interfacial microstructure of the UBM and the copper pillar, followed by its subsequent interaction with the solder bump. We also used XYZ TEC Condor Sigma to measure the shear stress between the Cu pillar and its pad on the wafer. The shear height is 7 μm . The shear rate is 100 $\mu\text{m}/\text{min}$ with a shear distance of 150 μm , and the pressure is 0.25 kgf.

III. Results and discussion

A. Electrochemical study

Acid copper baths for electrodeposition of pillars generally consist of make-up solution and a trio of organic additives: accelerator, suppressor, and leveler. The primary drivers of pillar height uniformity among these bath components are the acid and the additives. High acid concentration is

typically good for pillar height uniformity due to the increase in electrolyte conductivity and pillar surface polarization. However, on the other hand, some countries ban high acid concentrations of the ECP process for new product manufacturing due to health and environmental regulations. Therefore, in this study, we limited the acid concentration to 10% (100 g/L, 1.02 M sulfuric acid) and focused on additive development to achieve high uniformity and maintain high purity.

Fig.1 compares linear sweep voltammetry (LSV) of the current ECP process and a former process. Overall strong polarization strength of the current process indicates a flat copper pillar with better shape control. In addition, the greater slope (Wagner number, Wa) at the 9-11 A/dm² (ASD) current density region indicates improved uniformity across the whole die [3]. Equation (1) is the expression of Wa ,

$$Wa = \frac{d\eta}{dj} \frac{k}{l} \quad (1)$$

where $d\eta/dj$ is the slope of the cathodic activation overpotential over current density, k is the conductivity of the solution, and l is a characteristic length. More extensive Wa means more even current distribution and more even pillar height deposition.

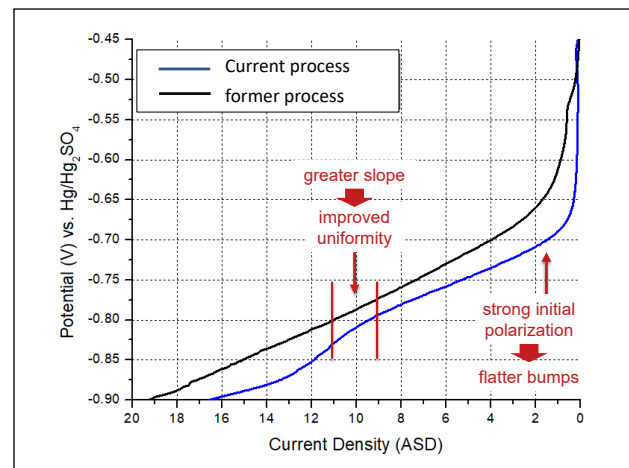


Fig. 1 Comparison of Linea seep voltammetry (LSV) of current and old process

The leveler component controls the within die (WID) uniformity in terms of the function of additives. The leveler component is typically a polymer with a cationic charge that helps shield and slow plating in areas with higher negative charge density [4]. For this work, we developed a new leveler with a higher molecular weight, higher charge density, and strong polarization, as shown in Fig. 1. We also developed a more potent suppressor to match this strong leveler.

B. Design of experiment (DOE) - coupon level testing

We utilized the response surface design to understand better and optimize the additive concentration after we finalized the selection of accelerator (A), suppressor (S), and leveler (L) by LSV screening and factorial DOE coupon plating. We fixed the plating speed at about 2.0 $\mu\text{m}/\text{min}$, plating temperature at 30 $^{\circ}\text{C}$, and agitation at 150 rpm. Fig. 2(a) shows the main effects plot for WID, and Fig. 2(b) shows the contour plots of WID vs. additive concentration. Fig. 2 indicates that accelerator concentration has minimal effect on WID; medium to high suppressor concentration is best for WID, and leveler is the main drive for WID. When we combine a higher leveler concentration with a medium suppressor, it results in the best WID. Fig 3(a) shows the main effects plot for WIF, and Fig. 3(b) shows the contour plots of WIF vs. additive concentration. For WIF, all three additives possess the same trend for WIF control. The lower the additives, the better the WIF is. However, a low accelerator is vulnerable to defect formation. Therefore, to minimize both WID and WIF with a defect-free process, we set the optimal additive concentration as high leveler (5 ml/l), medium accelerator (5 ml/l), and medium suppressor (5 ml/L).

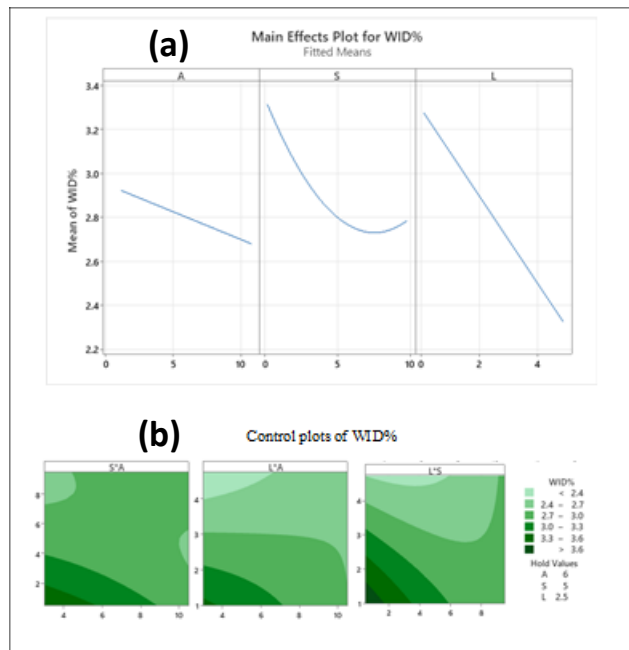


Fig. 2 (a) Main effect for WID (%), (b) contour plot of WID (%) vs. additive concentration

C. Tool level testing

We applied the recommendation of additive concentration to run whole wafer testing on the Nokota tool. Fig. 4 shows the locations of 13 chosen dies on the wafer to measure the

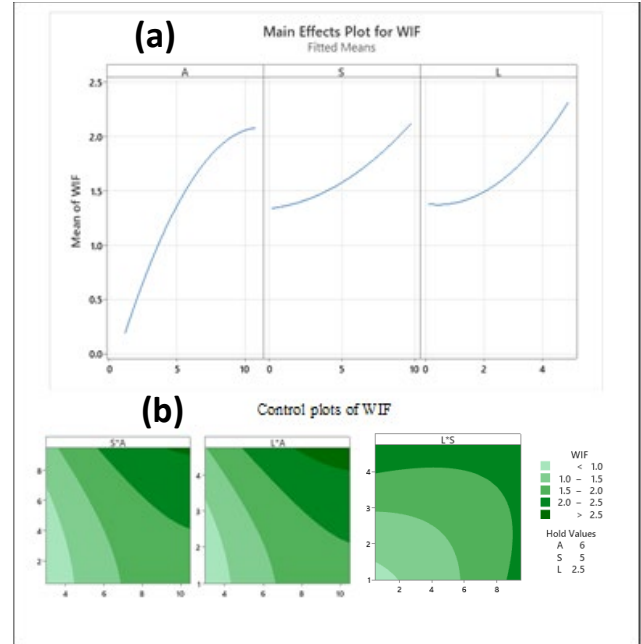


Fig. 3 (a) Main effect for WIF (%), (b) contour plot of WIF (%) vs. additive concentration

Within-wafer (WIW) performance. The die locations cover the wafer's top, bottom, left, right, center, and edge and represent the pillar performance. Like coupon level testing, we use eight pillars from different pitches and locations on each die to measure the WID and WIF performance, as shown in Fig. 5. The WID of all 13 dies is less than 2.5%. All the pillars are flat, and the WIF is less than 1.0 μm with a pillar height of 40 μm . The tool-level testing results agree well with mini-cell testing, and we achieved a WIW of less than 3.8%. Fig 6 shows the microscopy images of one section of a die, one image of the pillar, and the profile of a pillar. The microscopy image is a shiny, clean, flat, and defect-free pillar.

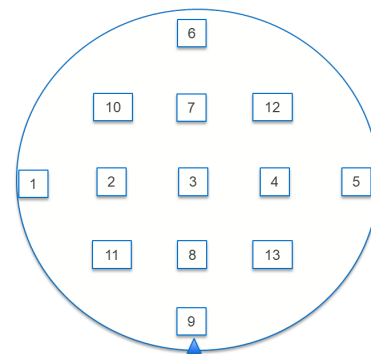


Fig. 4 Thirteen dies location used for within wafer performance measurement

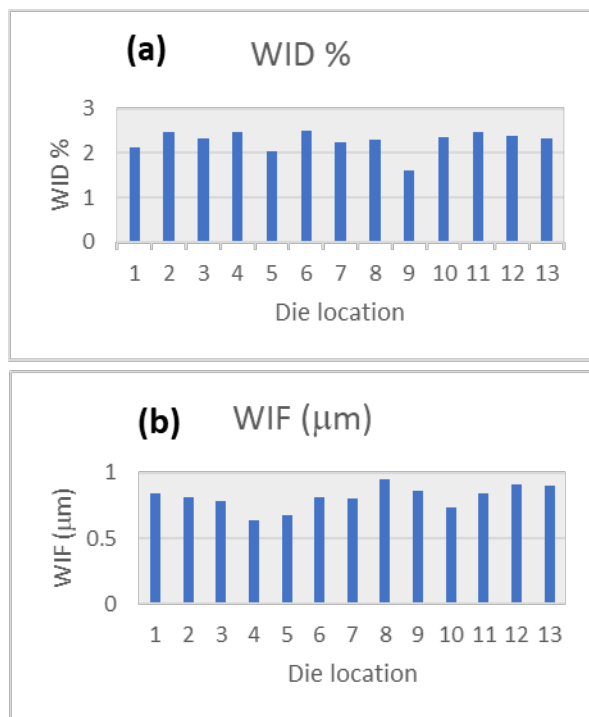


Fig. 5 Within die (WID - %) and within feature (WIF - μm) performance on the tool

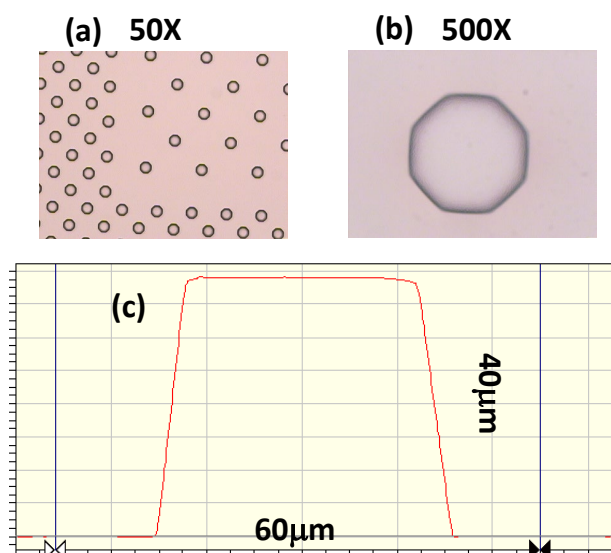


Fig. 7 (a) microscopy image of one section of die, (b) microscopy images of one pillar, (c) profile of the pillar

D. Reliability

Ensuring superior package reliability entails minimizing inclusions in the film, i.e., understanding its purity. A common problem with high-strength levelers is high

impurity. Stronger adsorption of such levelers to the surface of the copper cathode might result in higher inclusions, which in turn contribute to the formation of Kirkendall voids in the intermetallic compound (IMC) layer between the copper and tin-based solder plated on top of it. Kirkendall voids produce due to the imbalance of diffusion of Cu into Sn by forming the IMC layer of Cu_6Sn_5 and Cu_3Sn [5,6]. Organic impurities embedded in the Cu film might introduce vacancy and cause additional voids; therefore, we should strive to minimize the level of voids in the copper film. Our study compared the Cu pillar impurities plated with various current densities (2, 4, and 9 ASD) and utilized secondary ion mass spectrometry (SIMS) to detect and assess impurity levels, including C, O, N, S, and Cl. Fig. 6 shows the total organic inclusion vs. current density. The total impurity level of the pillar is less than 4.0 ppm when plated under 2 ASD, the inclusion increases slightly to close to 5.0 ppm when plated with 4 ASD, and the inclusion is about 9.0 ppm when plated with 9 ASD. Overall, under the current density tested, the impurity is very low even with this strong leveler. However, we can still minimize the impurities near the top of the copper pillar with a cap plated at a lower current density, such as 2 ASD, resulting in relatively low impurities (3.1 ppm on the top 1-2 μm) and minimum voids in between the Cu pillar and solder bump. Fig. 7 shows the cross-section of solder bump with 1x reflow following the 500 hours high temperature (150 °C) storage and 10X reflow. This high pure Cu pillar exhibits satisfactory voiding performance post solder bumping, reflow, and high-temperature storage (HTS) testing.

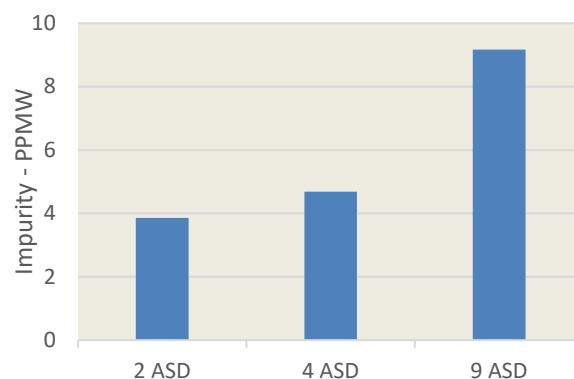


Fig. 7 Total organic inclusion (C, O, S, Cl and N) vs. current density

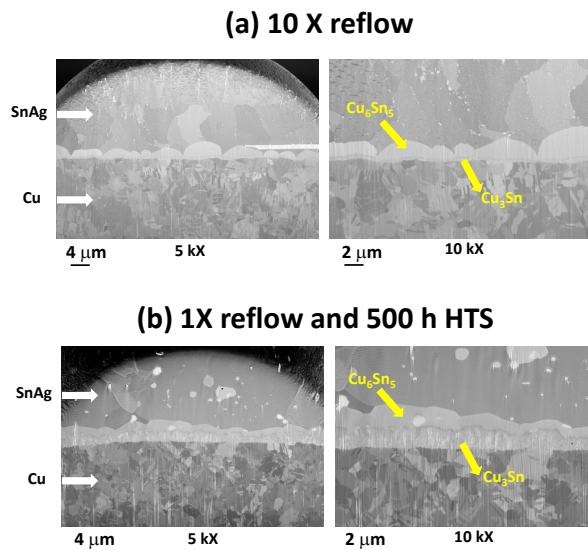


Fig. 8 FIB cross-sectional images of solder bump stacked on the top of Cu pillar: (a) 10X reflow; (b) 1X reflow following 500 hours 150 °C storage

Testing the mechanical integrity of the Cu pillar for interconnect is another essential criterion for reliable packaging. We used the shear stress test to measure the bonding between the copper and its pad on the wafer. We tested five pillars, and the average shear stress is 18.4 gf/mil², which is well above the standard criteria of 2.5 gf/mil².

	Pillar 1	Pillar 2	Pillar 3	Pillar 4	Pillar 5
Microscopy images					
Shear stress	17	17.44	18.75	19.40	19.62

Fig. 9 Microscopy images of sheared surface

III. Conclusion

We demonstrate the development of high uniformity, excellent pillar shape, and high purity of Cu pillar ECP process with limited acid concentration, 10% (100 g/L). This ECP process will complement aggressive device scaling initiatives at the advanced wafer-level packaging solutions providers while fulfilling the tighter environmental and health requirement and regulations. We apply this process to wafer patterns with various aspect ratios and layouts. As a result, the WID is below 2.5%, and WIF is less than 1.0 μm (~2.0%). Furthermore, this high pure Cu pillar exhibits satisfactory voiding performance post solder bumping reflow and high-temperature storage (HTS) testing and has high shear stress of 18.4 gf/mil².

Acknowledgment

The authors thank Dr. Cai Wang for his assistance with SEM/FIB work and Dr. Tao-Chi Liu and Sonia Huang for the reliability testing.

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