A novel hybrid method to integrate delicate MEMS components into a FOWLP

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Abstract

A steep increase in IoT- and smart devices fuels the need for ever more miniaturized and highly integrated microelectronic packages. Fan-Out technology is well suited for this task, as it allows for heterogeneous (co-)integration of sensor elements and corresponding circuitry. Following a Chip-First approach in Fan-Out Wafer-Level Packaging (FOWLP), protection of delicate sensor areas during compression molding and formation of redistribution layers (RDL) becomes a key part of the manufacturing process chain. Such areas include thin membranes, antireflective coatings, air bridges or media access for gas sensors.

We demonstrate a novel packaging method for a MEMS pressure sensor with corresponding ASIC (application-specific integrated circuit). We integrate vertical interconnect elements (VIE), instead of employing laser drilling for via formation and thereby avoid debris and reduce the overall package thickness. The hybrid approach, at heart, relies on a structured adhesive layer, onto which components are placed prior to compression molding. Due to its thermal and mechanical stability, the patterned thin film adhesive serves as a (first) dielectric layer. Process development includes warpage management to allow for laser debonding from temporary glass carriers and RDL processing compatible with delicate MEMS surfaces.

Summarizing, we present a novel process variant to avoid common issues related to sensor surface integrity using Fan Out technology and thus allow for highly miniaturized System in Package (SiP) concepts with sensor integration by mold embedding.

Key words

FOWLP, MEMS, pressure sensor, SiP, structured adhesive layer

I. Introduction

Large scale technology trends, such as autonomous driving, ever more complex consumer electronics, smart manufacturing and, most prominently, smart devices equipped with a variety of sensors as part of the Internet of Things (IoT) are key drivers for highly miniaturized, scalable packaging solutions at low cost.

Fan-Out Wafer-Level Packaging (FOWLP) with its intrinsic possibility for heterogeneous integration with multiple components and passives, as well as at excellent electrical and thermal system performance, offers a scalable platform which enables manufacturing of highly integrated System in Package (SiP) solutions for sensor applications at low cost [1,2].

The increasing demand for sensor integration requires solutions allowing for Fan-Out Packaging whilst protecting delicate components, such as MEMS microphones and pressure sensors, gas sensors and applications which require antireflective (AR) coatings, media access or other no-touch areas (also referred to as Keep Out Zones, KOZ) [3].

For the integration of a MEMS pressure sensor, which is considered in the following, either a Mold first – face down approach or an RDL-first flow can be applied, as are depicted in Fig. 1. Challenges regarding membrane cracking and
breaking arise during wafer reconstitution, namely during molding and especially carrier release. RDL formation with its typical process steps such as sputtering, photolithographic processes, etching and electroplating, can lead to similar failures of the delicate membrane structure.

Ensuring integrity of delicate surfaces on MEMS components, previous work focused on manufacturing subassemblies by glass on Si wafer bonding. These subassemblies for capacitive MEMS pressure sensor dice then form the starting point for the eWLB process [4]. A different approach is reported in [5], where the last steps of the MEMS fabrication process, final cavity etch and membrane release, are performed only after wafer reconstitution and RDL processing. This eliminates the need for dedicated measures to maintain membrane integrity of the packaged MEMS microphone. Yet, this requires interrupting the bulk Si DRIE etching process in the wafer fab.

In [6], the approach to establish Keep-Out-Zones (KOZ) on the RDL is pursued. Essentially, the delicate zones, such as sensor membranes and areas for media access or optical paths, are closed before RDL processing and opened afterwards, without damaging the underlying structure. Here, this is achieved using two dielectric layers, where the first one masks the KOZ and the second acts as a mask for subsequent ashing of the 1st dielectric layer by means of O₂ plasma. This offers an elegant solution and is compatible with established manufacturing flows. However, it does require direct deposition of the dielectric layer onto the structure, which is to be protected. This step alone might lead to damage in cases of highly sensitive structures, as is shown in the next chapter.

Approaches to avoid planar technologies for RDL processing altogether, such as metal sputtering, photolithographic patterning, and electroplating, were explored by using additive manufacturing technologies (AM) instead. Work focuses on inkjet, aerosol-jetting and related processes, as is reported in [7] and [8]. However, such approaches circumvent the need for protective measures during processing. Compared to fully parallel RDL processing, such serial approaches lack processing speed and scalability to higher volumes and to lower cost.

II. Packaging Process Development

Herein, we aim to develop a highly miniaturized SiP with a MEMS pressure sensor and corresponding ASIC with through mold vias (TMV) for signal routing to the package backside, as is sketched in Fig. 2.

Fig. 3a shows the used MEMS pressure sensor component, designed and fabricated by VTT. It features a 1x1 mm² footprint with 400 µm chip height with most of the die area consisting of hexagonal polysilicon membranes of ~1 µm thickness (compare Fig. 3b), which are connected in parallel. A typical membrane failure is depicted in Fig. 3c, which here originates from carrier release after overmolding.

The corresponding ASIC, depicted in Fig. 4 and developed by MAS, is 1.97x1.97 mm² large with a die thickness of 180 µm.
A. Structured adhesive layer

To solve membrane cracking issues due to mechanical load during P&P and release from the carrier wafer, several thin film polymer materials were evaluated regarding their suitability as temporary adhesives, having membrane integrity in mind. However, no available material allowed for a process to reliably obtain intact MEMS components after compression molding.

Hence, we develop a more complex, hybrid approach, which introduces elements typically found in RDL 1st flows (compare Fig. 1). The core of the hybrid Fan-Out flow is to adapt the eWLB-type “mold first – face down” such that the thermal release tape, onto which components are placed, is replaced by a structured adhesive layer.

For this, a polymer layer is developed and tailored to the specific requirements, such as:

- Mechanical decoupling of the sensitive membrane to avoid cracking.
- Strong enough adhesion to keep components in place during compression molding whilst most of the area under the die being recessed to protect the membrane, essentially leaving the die are towards the edges for adhesion.
- Non-sticky at room temperature, enabling easy handling and extensive storage of prepared glass carriers.
- The fully cured adhesive layer is stable enough to be used as a (first) dielectric layer.

The polymer is applied in a spin coating process, hence layer thickness can be adapted to package and component requirements. The polymer is structured by a resist and subsequent dry etching process. Finally, the polymer is non-sticky at room temperature and can thus be stored without timely restrictions. It needs to be heated up to ~100 °C for component assembly. Curing of the polymer takes place at 200 °C.

Two design variants are depicted in Fig. 5, with openings for all pads in the first row (a)-(d). Variant (e)-(h) features only two pad openings, used for MEMS alignment during pick and place [P&P]. Remaining pads can be opened later in the process via laser or dry etching. Both variants do not show membrane damage throughout the molding process.

The ASIC with a 1.97x1.97 mm² footprint is significantly larger than the MEMS component. The adhesive layer was chosen with a layer thickness of 2 µm to handle the topography of the ASIC and MEMS components. To limit the flow of adhesive into the contact pads cavities, dummy recess structures were introduced, as shown in Fig. 6. The more detailed ‘buffer-pads’ around the actual pad openings are shown throughout P&P, adhesive curing and compression molding in Fig. 7.

Note the clearly visible buffer pads in Fig. 7b, of which most are filled with adhesive after thermal curing (Fig. 7c).

Figure 5: Details recess for MEMS placement; a) initial; b) after ASIC P&P; c) after adhesive curing, d) after compression molding.

Figure 6: Design variants of structured adhesive layer: (a) alignment structures and basic dummy recesses; (b) advanced dummy recesses for improved shape of pad opening after component P&P.
Employing a structured adhesive layer in such a fashion allows to effectively mitigate the issue regarding handling of fragile areas on dies during wafer reconstitution. Furthermore, after (laser) release, the adhesive layer serves as the first dielectric layer.

B. Through Mold Vias - Vertical Interconnect Elements

Z-axis interconnects routing signals to the package backside are typically realized by combining laser drilling and subsequent electroplating. Here, we avoid laser drilling and thereby eliminate the following cleaning step as well. We manufacture Vertical Interconnect Elements (VIEs), mold-embedded Cu traces, which are diced and assembled onto the structured adhesive layer with MEMS and ASICs. The fabrication process, Fig. 8a, is straightforward: Blank Epoxy Molding Compound [EMC] wafer molding (Ø200 mm), Cu plating in a subtractive fashion, overmolding (Ø190 mm) and singulation by blade dicing. A 90° rotation around the short edge is done during assembly. Fig. 8b and c show the final dimensions of 400x500x700 µm³. Cu is 35 µm high, as well as ~40 µm and 70 µm wide, respectively, as is shown in Fig. 9b.

Previously manufactured VIE proved to be an easy to manufacture z-axis interconnection, which fits well into the proposed process flow, as after overmolding alongside with MEMS and ASIC, opening of Cu on the package bottom side is done by grinding. This is especially useful as it can be done without releasing the reconfigured molded wafer from the temporary glass carrier, hence membrane protection is ensured.

VIEs are treated as components during assembly and by employing VIEs, we eliminate laser drilling through EMC entirely from the proposed process flow. Also, the chance to test VIEs before assembly allow to adapt the ‘Known Good Die’ to these elements, which therefore contributes to increase production yield.

C. Developed Hybrid Fan-Out process flow

Summarizing, we combine the initial process flow (Fig. 1, left, ‘Mold first - face down’) with the patterned adhesive layer, as laid out in A, and VIE elements, as discussed in B. Essentially, the resulting ‘Hybrid Fan-Out’ process flow replaces commonly used thermal release tape with a patterned adhesive layer from typical RDL 1st process flows. It keeps the dice and components in place, even though only a small portion of the die surface actually comes into contact with the adhesive. Proper adhesion is achieved due to carefully optimized substrate temperature, bonding force and bonding time. Here, we balance sufficient adhesion and sealing of the recess underneath components with
flowing/squeezing of the adhesive layer itself. After curing, it also serves as the first dielectric layer. Integrating previously manufactured VIE elements simplifies the process flow, as they are treated as components during die assembly. Also, they eliminate the need for laser drilling to create z-axis interconnects, as back grinding opens the backside contacts and allows for backside RDL processing. After this, laser release of the reconfigured wafer from the glass carrier is performed. Figure 10 shows the adapted process sequence.

III. Results
In the previous section, we introduce the integration concept for delicate components into miniaturized SiP solutions for Fan-Out Wafer Level Packaging. We demonstrate this with the pressure sensor MEMS and corresponding ASIC on 200 mm wafer format. The final package features a footprint of 3x4.5 mm², compare Fig. 11, with a thickness remaining EMC thickness of 300 µm after back grinding. Here, patterned areas, as described above, are turquoise, top metal layer is depicted in green, whereas the bottom metal is blue. Orange denotes pads of ASIC, MEMS and VIE elements. Fig. 12a shows an isometric photograph of all components after pick and place onto the glass carrier before overmolding. Fig. 12b shows the VIE placed atop the patterned opening, which also served as an alignment/target structure during VIE assembly. The intermediate top view after back grinding is shown in Fig. 13a, where VIE Cu traces are opened. Also grinding removed bulk Si from the MEMS backside. The 180 µm thick ASIC, however, is still fully embedded in EMC. The bottom side is shown in Fig. 13b, whereas the top side with the active sensor area can be seen in Fig. 13c.

Only one out of nine tested MEMS exhibited membrane damage.
IV. Conclusion
We demonstrate a ‘Hybrid Fan-Out’ package, which contains a MEMS pressure sensor with fragile membrane. The innovative concept overcomes some disadvantages of the eWLB process and avoids contact between sensor areas and the (typically temporary) adhesive layer by employing (etched) recesses in the otherwise continuous layer. Fine-tuned patterning of the adhesive layer together with careful control of the P&P process allows us to achieve good adhesion of components with only a small part of each sensor die being actually in contact with the adhesive layer. The developed patterned adhesive layer avoids the demand for a thermal release tape (TRT), which is commonly used, and enables using a glass carrier, also during backside RDL processing. By using the adhesive layer as first dielectric layer it has high potential for lower cost instead, as no TRT is needed. The realization of through mold vias (TMV) by the developed vertical interconnect elements (VIEs) show an excellent integration into the Fan-Out process with a high potential also for packages with increased I/O demands. The packaging process was demonstrated on 200 mm substrates.

The developed integration concept can be extended to a larger variety of components with delicate surfaces, such as optical components, gas sensors, microphones or RF-chips with air-gaps and will thus further contribute to FOWLP gaining even more traction and penetrating further market segments.

Next steps will be the extension of the technology to multiple, high density, routing layers. Further investigations should be performed to bring this concept closer to production. The material for the adhesive shows potential for further optimization to higher resolution and mechanical stability. Handling and processing of thinned mold substrates after release from the glass carrier needs to be improved for automated production. A further future aspect to consider is the mismatch in thermal expansion between Si (~2.6 ppm/K) and EMC (~8 ppm/K), as well as shrinkage of the EMC (due to the poly-addition of the epoxy-matrix during curing). They lead to warpage, making handling more challenging in wafer-level, but also introduce compressive residual stress into the MEMS sensor. As this possibly affects performance, stress buffer layers (i.e. a soft polymer layer with a low Young’s modulus, i.e. <2 GPa) could be considered.

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References


