

# Inspection Solution for 2 $\mu$ m RDL from Wafer-Level to Panel-Level Fan-out Process

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## Abstract

In the advanced packaging industry, both fan-out wafer-level packaging (FOWLP) and fan-out panel-level packaging (FOPLP) have grown quickly in recent years since they are compatible with largescale, low-cost manufacturing and are key enablers for ultra-thin and high-density packages. However, the commercialization of the fan-out process continues to face technical challenges with the rapid adoption of finer pitch and width of the Cu redistribution layer (RDL) in die-first or die-last integration approaches. AOI has been widely used in the advanced packaging industry as a major tool for defect inspection during various process steps. The conventional bright field and dark field imaging techniques suffer from a high nuisance rate for RDL inspection; in many cases, the RDL metal grain size could be larger than the defect of interest, and the interferences from underneath the pattern, such as bottom RDL layers or molding compounds, can increase the difficulties of defect detection. In this paper, we present Onto Innovation's innovative fluorescence technology to enhance contrasts between organic material, such as polyimide, or photoresists and metals that enable fine-pitch RDL inspection with increased accuracy by eliminating nuisance defects. By using powerful fluorescence technology, in conjunction with higher resolution, high-definition inspection (HDI) technology, fine-pitch RDL defect inspections on both wafer-level and panel-level packaging were studied and shown to enable accelerated development cycles in the R&D stage, as well enable rapid yield enhancements in the HVM environment.

## Key words

AOI, Fan-out, FOWLP, FOPLP, HVM, RDL

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Fan-out packaging is becoming mainstream for high-end device applications [1], especially for system-in-package (SIP) and heterogenous integration for both active and passive devices with a high density of interconnect, excellent performance in electrical performance and power consumption. Today, fan-out packages are used in high-volume applications for a wide variety of mobile, HPC and 5G products, including PMICs, RF packages, baseband processors and high-end networking systems.

Fan-out packaging is a steadily growing market, with 15.9% CAGR forecasted between 2019 and 2025. The market value should reach \$3 billion (U.S.) at the end of that period [2]. First-generation "core" fan-out packages were geared toward mobile applications, with redistribution layers (RDLs) typically in the scale of 15 $\mu$ m/15 $\mu$ m (line/space). RDLs are copper metal lines that connect part of the package

to another and are defined by line/space. High-density fan-out (HDFO) packaging typically requires a smaller dimensional RDL with less than 10 $\mu$ m L/S; HDFO has demonstrated remarkable growth in recent years following successful adoption by key players. The advanced third-generation, ultra-high-density fan-out (UHDFO) processes [3-4] were developed to integrate multiple chips in a single package through multilevel RDL lines at smaller width and tighter pitch. These RDL lines were scaled down to 2 $\mu$ m L/S, with further shrinking a potential trend (Fig. 1). Continuous scaling does lead to increased process complexity as well, with more process monitoring challenges in order to maintain high yields.

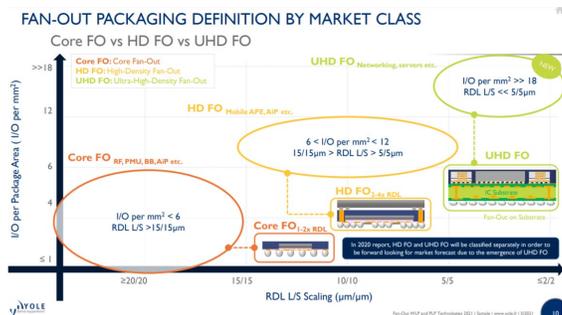


Figure 1. Fan-out package definition from Yole 2021

The detection of open and bridge defects in RDL without finding nuisance defects has become critical as the cost of each known good die (KGD) is extremely high in the back-end. An AOI inspection system to detect open/short defects and confirm final yield result also requires innovations in several areas. The first is to enable higher resolution detection capability in response to rigorous process control as the design rule scales. Traditional macro AOI inspection may reach boundary resolution in considerations of the WPH and DOF with 10x. Second, the thin wafers or substrates used in HDFO processes can be highly warped across several different process stages; the warpage of 2mm or more is commonly a result of mismatched thermal expansion coefficients between the molding compound and die. The AOI system must be able to support the handling of highly warped substrates. Thirdly, the enhancement on robust site alignment to ensure positioning accuracy on repeating RDL structures is critical to deal with the inspection of larger dies on product wafers.

In this paper, we will discuss higher-resolution RDL detection capability by high-definition inspection (HDI), an extended camera solution with double-pixel resolution from 1µm to 0.5µm that pushes detection capability down to 0.7µm. In addition, the industry is studying panel-level HDFO packaging in conjunction with patterning approaches for cost-reduction and yield-enhancement solutions. HDI, as a fine-pitch RDL solution that overcomes the process challenges of extending capability from the wafer-level to panel-level, will be presented in this paper.

**Inspection Methodology**

Conventional macro inspection is equipped with bright field (BF) and dark field (DF) illuminations from different angles. To overcome nuisance defects caused by high Cu graininess from the plating process, both BF and DF struggle to detect true defects while filtering out the huge nuisance defects from the rough RDL surface. The innovative solution to increase defect detectability under such conditions is to add fluorescence illumination (Fig. 2).

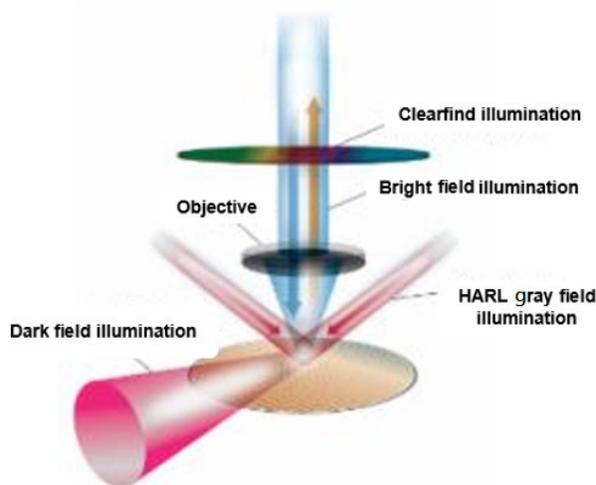
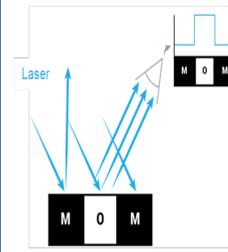
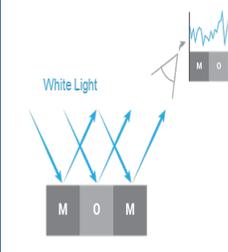


Figure 2. Illumination light path of Clearfind

Clearfind® (CF) technology is a fluorescence illumination method. CF uses a constant laser wavelength to excite fluorescence on organic material. Fluorescence is the emission of light by a substance that has absorbed light or other electromagnetic radiation. It is a form of luminescence. In most cases, the emitted light has a longer wavelength and, therefore, a lower photon energy than the absorbed radiation (Fig.3).



- Clearfind® technology can distinguish organics from metals in one image because it uses a patented combination of *laser*, optics, and image analysis which produces high contrast between organics and metals.



- Other suppliers cannot distinguish organics from metals because they use *white light* which illuminates metal grains producing a noisy image with little contrast between organics and metals.

Figure 3. Enhanced organics/metal contracts by fluorescence

The contrast between organic material and metals is enhanced as a result of different fluorescence responses to illumination; Thus the signal-to-noise ratio is significantly improved for defect detection. Fluorescence technology has

become mainstream for RDL inspection application in recent years.

With RDL scaling down to  $2\mu\text{m}$  L/S or below in fan-out processes, the high definition inspection (HDI) mode is essential to offering the resolution required for defect detection in finer-pitch RDL (Fig.4). It is now designed to serve wider application spaces by enabling the higher resolution HDI mode using  $1 \times 1$  binning on top of a standard high-speed inspection (HSI) mode with  $2 \times 2$  binning. The binning feature has the advantage of increasing the scan speed with degraded resolution by averaging out and integrating the adjacent pixels. This feature is particularly useful when acquiring line images with lower resolution. With the binning feature, one can acquire lower resolution images without having to change optics or lighting settings. Our AOI system is designed with the flexibility to offer HDI and HSI inspections in the same platform for the best user experience while balancing performance and productivity options.

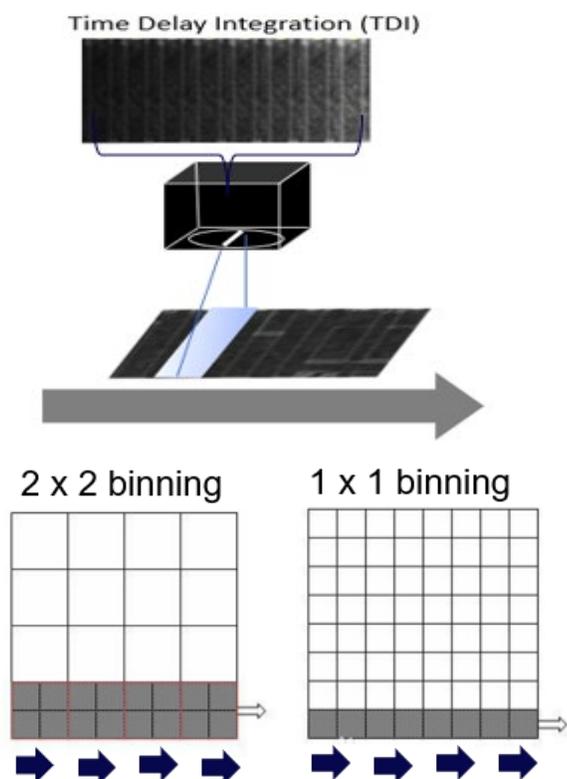


Figure 4. 9K TDI (time delay integration) camera enable  $1 \times 1$  binning from  $2 \times 2$  binning to release high definition

The new 9K TDI (time delay integration) camera enables faster scanning speed by enhanced integration efficiency at lower light illumination. TDI operation effectively averages out fluctuations in light intensity to represent a DC light

source. Gain control with analog gain typically is set from 1 to 4 while digital gain in is in the range of 1 to 8. (Table I).

Table I. Selected features for new 9K TDI camera

Generation	Last Generation	New Generation
Resolution (pixels)	4096	8912
Pixel size ( $\mu\text{m}$ )	14.0	7.0
Max line rate (kHz)	100	196
TDI stages	48	128
HDI function	No	Yes
Sensitivity	Medium	High

Image processing is another critical function in the inspection setup; it is typically applied to enhance features, contrast and sharpness or to filter out noises from the raw images. Optimized image processing settings, such as morphological transformation, spatial filter, etc., could greatly improve the image quality for RDL inspections.

An example of morphological transformation is illustrated in Fig.5. The goal is to analyze and process objects in images (e.g., skeleton, convexity, edge, feature, connectivity, etc.). Techniques of morphological filtering, thinning and pruning are typically involved to extract pixels from defects of interest. The raw scanned image (a) contains several defects including mouse bites, protrusion and open, (b) followed by two separate morphological transformations applied to yield the dilated image and (c) the eroded image. One can easily get enhanced features from DOI in a difference image (d) by subtracting these two images.

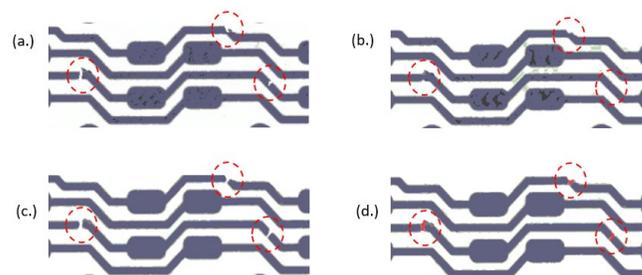


Figure 5. Morphology transformation case, (a.) Raw image. (b.) Post-dilation image. (c.) Post-erosion image. (d.) Difference image of (b - c) with enhanced DOI features.

Other examples of how RDL open/short defects get enhancement through image process strategies are illustrated in Table II and Table III. The image process strategy needs to be optimized according to key defect types, patterned layout and scheme.

Table II. RDL Open image process enhancement

Raw image	Enhancement edge feature first	Enhancement edge feature second	Smooth all image first	Morphology to filter nuisance on RDL area	Enhancement edge feature on RDL
RDL open feature is not clear, gray pixels will cause false escaped.	Convolve Laplacian 8 connected Edge Algorithm : Canny Smoothness 50	Convolve Sharpen all feature Algorithm : Canny Smoothness: 10	Gaussian Kernel Size : 9 Sigma Factor: 3	Close Kernel Size: 3 Iteration: 1	Convolve Sharpen all feature Algorithm : Canny Smoothness: 10

Table III. RDL Short image process enhancement

Raw image	Gaussian filter first	Enhancement edge feature	Enhancement edge feature again	Morphology to filter nuisance on RDL area
Non RDL line GSV between RDL to RDL is not bright and close nuisance.	Gaussian Kernel Size : 9 Sigma Factor: 1	Convolve Laplacian 4 connected Edge Algorithm : Canny Smoothness 50	Convolve Sharpen all feature Algorithm : Canny Smoothness: 50	Close Kernel Size: 3 Iteration: 1

**Inspection Experiment from Wafer Level**

There are great varieties of packaging forms in FOWLP that can be split into three categories accordingly to process sequence, namely chip-first (die face-down), chip-first (die face-up) and chip-last or RDL-first. In this study, we took an experimental inspection of RDL-first samples with RDL 2µm L/S. CF illumination was used instead of conventional BF or DF. Fig. 6 shows comparisons between BF, DF and CF on 2µm RDL.

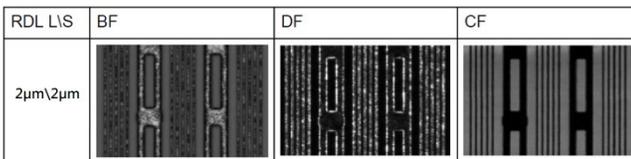


Figure 6. Image comparison under different light sources

CF offers enhanced image contrast, with metal graininess eliminated. The next question is how to deal with background gray scale value (GSV) deviations that could vary from die to die and wafer to wafer as a result of normal process variations from multi-underlying RDLs or fan-out compounds (Fig. 7). Such a high deviation of background GSV could lead to unstable inspection with huge nuisances.

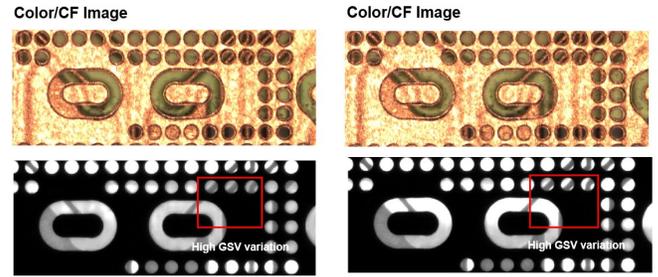


Figure 7. Background GSV can vary from die-to-die comparison

To overcome the challenge, HDI was used, instead of the standard mode, to increase pixel resolution to 0.5µm /pixel with 10X objective to gain ideal line-space separation (Fig. 8). The 20X objective was tested but not applied in this case since its spatial resolution (~0.4µm) is close to pixel resolution and does not offer much further enhancement but degrades the throughput performance dramatically.

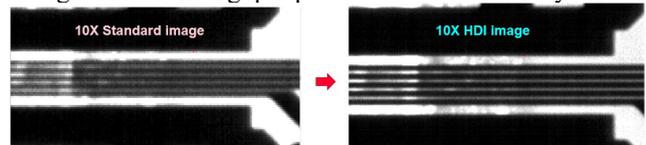


Figure 8. RDL 2/2 comparison between standard and HDI mode

The next step is to optimize 10X raw image by image process strategies to enhance RDL image contrast. See Fig. 9 for image comparison.

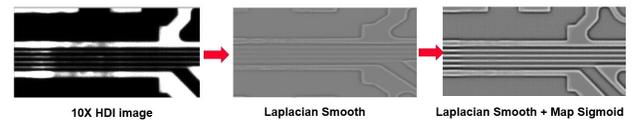


Figure 9. RDL 2µm line/space contrast enhancement by steps of image process.

The defect maps comparison, with and without image process strategies, is demonstrated in Fig. 10 with defect counts analysis in Table IV. The true killer defects remained the same, indicating no degradation of sensitivity, while nuisances were significantly suppressed by 1,000X through image process strategies.

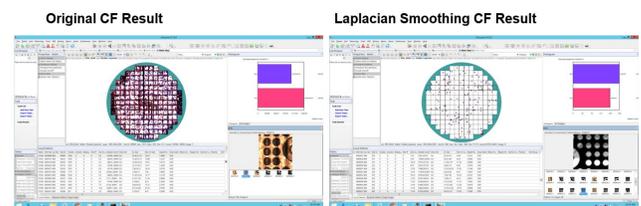


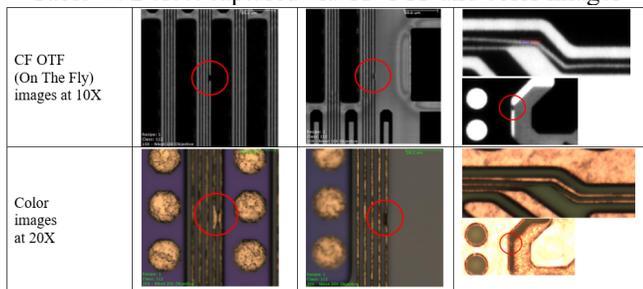
Figure 10. Inspection result comparison after applying image process

Table IV. Inspection result for defect counts

	Original	CF + image process
Real killer	132	132
Nuisance	106,118	63

The following are reference images for selected killer defects captured by CF on-the-fly (OTF) inspection (Table V):

Table V. Defect captured via CF OTF and color images



**Inspection Experiment from Panel Level**

Cost is one of the driving forces pushing panel-level fan-out packaging. The industry has gradually narrowed panel dimensions into two sizes, 510mm x 515mm or 600mm x 600mm, in preparation for commercialization. Unlike the wafer-level fan-out process that is relative mature, the panel level fan-out process has more unique challenges, such as larger panel warpage, die shifting and less aggressive RDL at the 5µm L/S, while R&D is pushing down to 2µm L/S. In this section, we'll introduce how we overcame the inspection challenges on R&D design of experiments (DOE) shuttle panel and improved proven inspection sensitivity to 2µm RDL and below.

A DOE shuttle panel with programmed RDL open and short defects from 1µm to 3µm on specific 2µm RDL areas was prepared for this study. The programmed DOE defects varied from 1µm to 1.5µm, 2µm, 2.5µm and 3µm for both open and short defect types for schematic plot on 510mm x 515mm panel and designed for open/short defects (Fig 11). In each RDL layout, two directions of horizontal and vertical were designed on the upper and bottom areas.

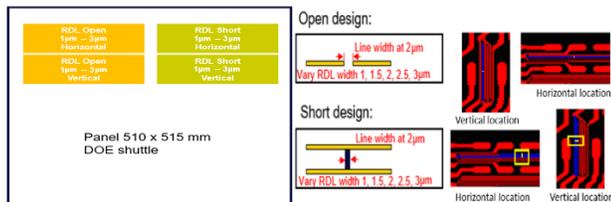


Figure 11. 2 RDL Panel, DOE shuttle

The initial trial inspection result by CF with HDI 10X was listed in Fig. 12. The detection capability was limited to 3µm for RDL open defects and 2.5µm for RDL short defects for

the first trial. The reason for missing smaller programmed defects was the influences from underlying layers, pattern variations and other nuisances (Fig.13).



Figure 12. Initial trial inspection result on DOE panel.

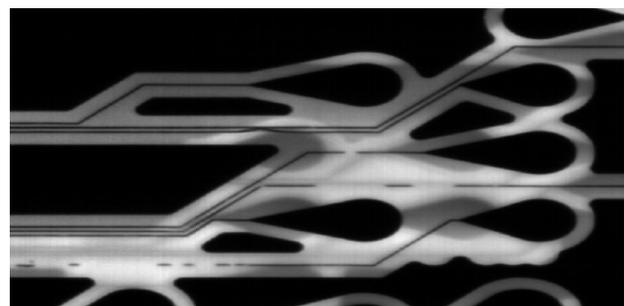


Figure 13. Inspection result occurring under layer pattern and nuisance

By studying similar approaches of nuisance reduction on wafer forms, image process strategies were applied to increase the raw image contrast and effectively filter out the nuisance (Fig. 14). The separate image process strategies were optimized for RDL open defects and RDL short defects to ensure best sensitivity on DOIs.

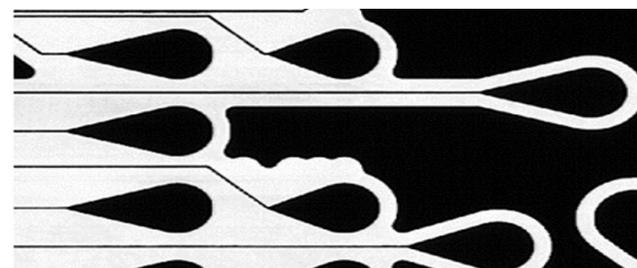


Figure 14. Image process strategies were applied to suppress background noise

After applying several steps of image processes for RDL line and space separately, CF inspection capability was successfully pushed down to 1µm RDL for open defects and 1µm RDL for short defects on programmed defects; see Fig. 15 for the result. Furthermore, defect detection rates for three types of inspection strategies were compared: one pass, two passes and two passes + image process (Table VI). All programmed defects can be captured 100% using the optimized strategy of two passes + image process.

[5] Yole Development, "Fan-out packaging: what will be the next killer applications?", *Yole Development*, June 2021.

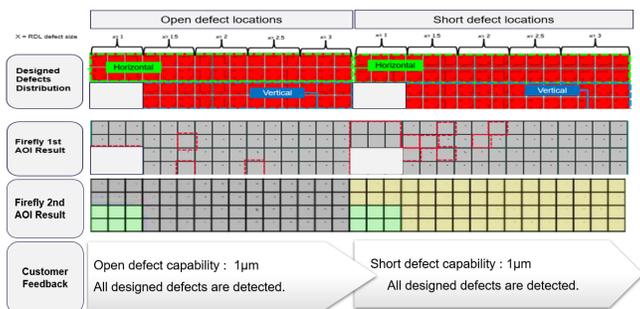


Figure 15. Optimized inspection scheme to capture all programmed defects

Table VI. Improved detection rate with enhanced inspection scheme

Tool + Image Processing	Real defects	Defect detection rate
One pass for open and short	112	30%
Two passes for open and short	54 + 58	85.80% (average)
Two passes + image processing	54 + 58	100%

### III. Conclusion

This paper examined fine-pitch RDL inspection requirements and challenges in the fan-out process from wafer to panel form. Automated defect inspection systems must offer the capability to inspect RDL down to 2µm L/S with 1µm defect detection sensitivity.

Fluorescence illumination was greatly adopted as a key enabler to overcome grainy RDL for defect inspection. Additional image process strategies were proven to greatly enhance image contrasts and suppress the influence of underlying layers. As a combination of both, the defect inspection accuracy significantly improved with nuisance elimination. Unlike the traditional BF or DF that requires complex segmentations on ROIs but still has several gaps on fine-pitch RDL inspection, Onto Innovation’s Clearfind® and image process techniques offer a powerful method for killer defect detection that enables true RDL process monitoring in R&D and HVM phases.

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### References

- [1] Buisson, T. & Kumar, S., "What is driving advanced packaging platforms development?", *Chip Scale Review*, pp. 32-36, May-June 2016.
- [2] Lau, J., "Recent advances and trends in advanced packaging," *Chip Scale Review*, pp. 46-54, May-June 2017.
- [3] Lau, J., "Recent advances and trends in fan-out wafer/panel-level Packaging," *J. Electron Package*, Dec 2019.
- [4] Yess, Kim, "Material innovations for advancements in fan-out packaging," July 2018.