Heterogeneous Integration Hybrid Substrate with Ajinomoto Build-Up Film

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Abstract
The design, materials, process, and fabrication of a hybrid substrate for the heterogeneous integration of chips with 50µm-pitch (minimum) by fan-out chip-last panel-level packaging are presented. The hybrid substrate consists of a fine metal linewidth (L), spacing (S), and thickness (H) RDL (redistribution-layer) substrate, solder joints with underfill, and a build-up package substrate. The dielectric material for the fine metal L/S/H RDL-substrate is an Ajinomoto build-up film (ABF).

Key words
Hybrid substrate, Ajinomoto build-up film, fine metal L/S RDL-substrate, heterogenous integration packaging

I. INTRODUCTION

In this study, the hybrid substrate consists of a fine metal L/S/H RDL-substrate, solder joints enhanced with underfill, and a build-up package substrate [1-12]. In [11, 12] we have developed a hybrid substrate based on a photoimageable dielectric (PID) for heterogeneous integration of multiple chips. Unfortunately, it yields un-even (not flat) metal layers of the fine metal L/S/H RDL-substrate. In this study, instead of the PID, we use the Ajinomoto build-up film (ABF) as the dielectric material to fabricate the fine metal L/S RDL-substrate of the hybrid substrate. It is fabricated by a fan-out chip-last (RDL-first) process on a large temporary glass panel (515mm x 510mm). The new hybrid substrate (with a minimum L/S/H = 2µm/2µm/3µm) with the ABF yields much flatter metal layer of the RDLs and thus much better electrical performance. This new hybrid substrate is supporting the heterogeneous integration of one large chip (10 x 10mm) and one smaller chip (5 x 5mm). The thermal reliability of the structure will be demonstrated by simulation. Some recommendations will be provided.

II. THE STRUCTURE

Figure 1 schematically shows the structure under consideration. The two chips (Chip 1 and Chip 2) are supported by a hybrid substrate, which is fabricated by combining the fine metal L/S/H RDL-substrate (20mm x 15mm x 53µm) and the build-up package substrate (23mm x

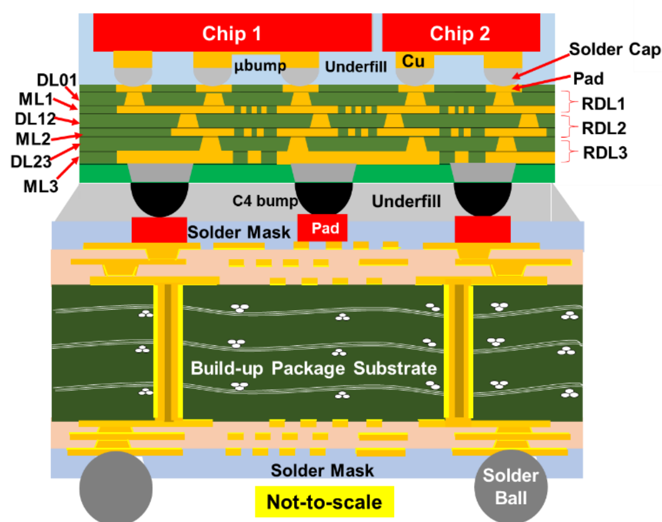
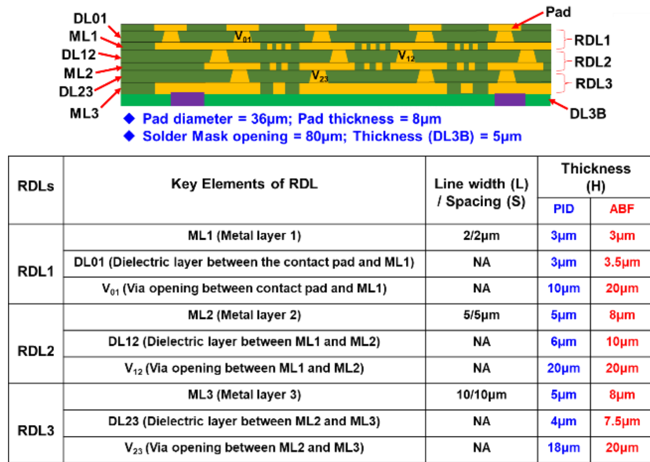


Fig. 1 Cross section of the structure.

23mm x 1.3mm) through the C4 (controlled collapse chip connection) solder joints and underfill.

The fine metal L/S/H RDL-substrate is shown in Figure 2 with dimensions. It can be seen that there are three RDLs, each consists of a dielectric layer (DL) and a Cu metal layer (ML). The DL material of [11, 12] is PID and of this study is an ABF with the materials properties shown in Table 1. The L/S/H of ML1 (metal layer 1) are 2µm/2µm, of ML2 are 5µm/5µm, and of ML3 are 10µm/10µm, which are the same



RDLs	Key Elements of RDL	Line width (L) / Spacing (S)	Thickness (H)	
			PID	ABF
RDL1	ML1 (Metal layer 1)	2/2μm	3μm	3μm
	DL01 (Dielectric layer between the contact pad and ML1)	NA	3μm	3.5μm
	V_{01} (Via opening between contact pad and ML1)	NA	10μm	20μm
RDL2	ML2 (Metal layer 2)	5/5μm	5μm	8μm
	DL12 (Dielectric layer between ML1 and ML2)	NA	6μm	10μm
	V_{12} (Via opening between ML1 and ML2)	NA	20μm	20μm
RDL3	ML3 (Metal layer 3)	10/10μm	5μm	8μm
	DL23 (Dielectric layer between ML2 and ML3)	NA	4μm	7.5μm
	V_{23} (Via opening between ML2 and ML3)	NA	18μm	20μm

Fig. 2 Dimensions of the fine metal L/S RDL-substrate.

TABLE 1 ABF Material Properties

Items	ABF (RDL-Substrate)	ABF (Build-up Substrate)
Curing Condition, °C for min	200 for 90	190 for 90
CTE (25 - 150°C), 10^{-6}/°C	37	39
CTE (150 - 240°C), 10^{-6}/°C	98	117
Tg, °C	156	153
Dielectric Constant (Dk), 5.8GHz	3.2	3.2
Loss Tangent (Df), 5.8GHz	0.011	0.017
Young' Modulus (23°C), GPa	7.5	5.0
Tensile Strength (23°C), GPa	125	98
Elongation (23°C), %	5.4	5.6

as [11, 12]. The dielectric layer between the contact pad and ML1 (DL01) is 3.5µm, DL12 (dielectric layer between ML1 and ML2) is 10µm, and DL23 (dielectric layer between the ML2 and ML3) is 7.5µm, which are different from [11, 12] as shown in the table of Figure 2. All the vias between the metal layers are 20µm, which are also different from [11, 12].

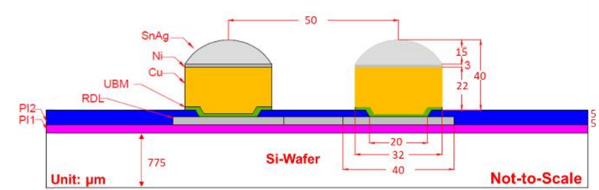
III. TEST CHIPS AND WAFER BUMPING

(A) Test Chips

The dimensions of Chip 1 are 10mm x 10mm x 150µm and of Chip 2 are 5mm x 5mm x150µm. There are 3592 daisy-chained pads on Chip 1 and 1072 daisy-chained pads on Chip 2. The minimum pitch of these chips is 50µm. The material and geometry of the microbump (µbump) of both chips are the same (Figure 3): the Ti/Cu (0.1/0.2µm) UBM (under bump metallurgy) pad size is 32µm-diameter, the passivation (PI2) opening is 20µm-diameter, the Cu-pillar is 32µm-diameter and 22µm-tall, the SnAg solder cap is 15µm with a barrier (Ni = 3µm).

(B) Wafer Bumping

The process flow of the wafer bumping of the test chips is shown in Figure 3 and the µbumps are shown in Figure 4.



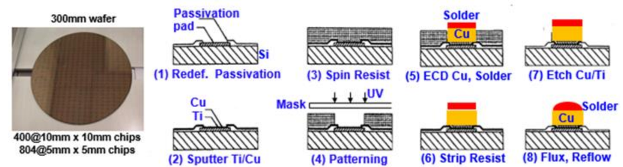


Fig. 3 Wafer bumping of test chips.

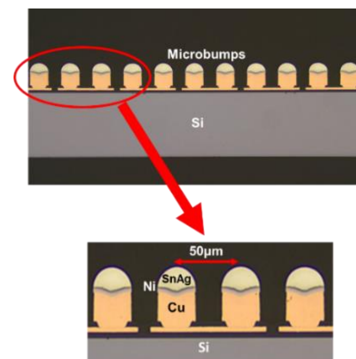


Fig. 4 µbumps on test chips.

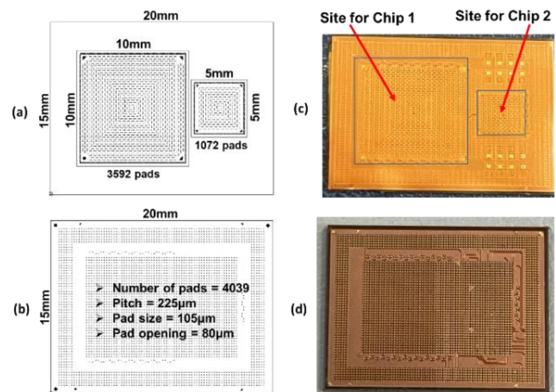


Fig. 5 RDL-substrate. (a) Top view. (b) Bottom-view. (c) Fabricated top-view with glass removed and Ti/Cu etched. (d) Fabricated bottom-view.

IV. FINE METAL L/S/H RDL-SUBSTRATE

The top-view and bottom-view of the fine metal L/S/H RDL-substrate are shown in Figure 5(a) and 5(b), respectively. It can be seen that there are 4664 pads for the µbump from the chips and there are 4039 pads for the C4-bumps from the build-up package substrate.

The process in fabricating the fine metal L/S/H RDL-substrate is shown in Figure 6. A sacrificial layer

(1μm-thick light-to-heat conversion released film) is slit coating on a temporary glass panel (515mm x 510mm x 1.1mm) and then a Ti/Cu seed layer is PVD (physical vapor deposition) on the top. The contact pad can be obtained by photoresist, laser direct imaging (LDI), development, ECD (electrochemical deposition) Cu, and stripping off the photoresist. Then, laminate a 12.5μm-thick raw ABF with nano-filler (Table 1) on the whole panel. There are two operating stages of the ABF: (1) at the first stage, the temperature is 120°C for 30s at vacuum condition and then press (0.68MPa) for 30s with the temperature and vacuum on, and (2) at the second stage, the temperature is 100°C and press (0.58MPa) for 60s. The first DL (dielectric layer) DL01 (3.5μm-thick) of RDL1 is drilled by a UV laser to obtain the blind via. It is followed by PVD the Ti/Cu, photoresist, LDI and development, ECD the Cu, strip off the photoresist, and etch off the TiCu to obtain the first ML (metal layer) ML1 of RDL1. DL12 and ML2 of RDL2, and DL23 and ML3 of RDL3 can be obtained by repeating the same process steps.

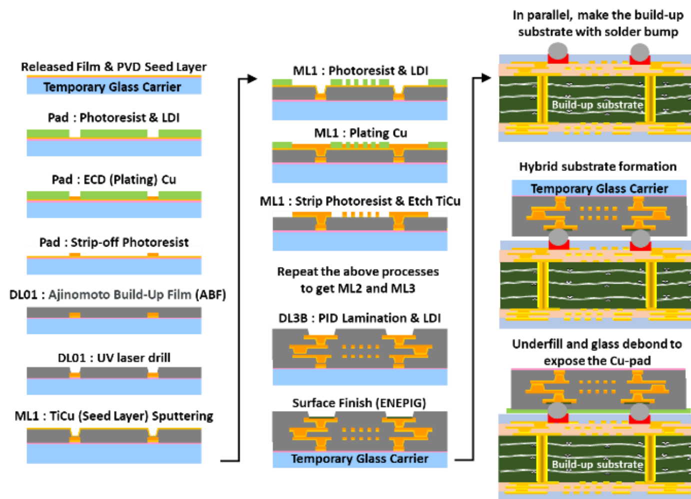


Fig. 6 RDL-substrate process flow.

The 5μm-thick solder mask (passivation) can be obtained by laminating a 10μm-thick raw dry film PID and LDI. Then, the surface is finishing with electroless nickel electroless palladium immersion gold (ENEPIG). The fabrication of the fine metal L/S/H RDL substrate is completed. The top-view and bottom view of the RDL-substrate are shown in Figures 5(c) and (d), respectively.

The SEM image of the RDL substrate is shown in Figure 7. Table 2 shows the metal L, S, and H from design and fabrication. For RDL1, L = 2.4μm (not 2μm), S = 1.8, 2.0μm (not 2μm), and H = 3.2, 3.5μm (not 3 μm). For RDL2, L = 5.1, 5.0μm (not exactly 5 μm), S = 4.8, 4.4μm (not exactly 5μm), and H = 7.2, 7.4μm (not exactly 8μm). For

TABLE 2 L/S/H Comparison: design vs. fabricate

RDLs	Items	Design (μm)	Measured (μm)
Metal of RDL1 (ML1)	Linewidth (L)	2	2.4, 2.4, …
	Spacing (S)	2	1.8, 2.0, …
	Thickness (H)	3	3.2, 3.5, …
Metal of RDL2 (ML2)	Linewidth (L)	5	5.1, 5.0, …
	Spacing (S)	5	4.8, 4.4, …
	Thickness (H)	8	7.2, 7.4, …
Metal of RDL3 (ML3)	Linewidth (L)	10	9.9, 10.3, …
	Spacing (S)	10	9.4, 9.2, …
	Thickness (H)	8	8.2, 8.6, …

RDL3, L = 9.9, 10.3μm (very close to 10μm), S = 9.4, 9.2μm (not exactly 10 μm), and H = 8.2, 8.6μm (close to 8μm). Thus, there are rooms for improvements, e.g., better estimation of compensation of photoresist, LDI, ECD Cu, Cu etching, etc.

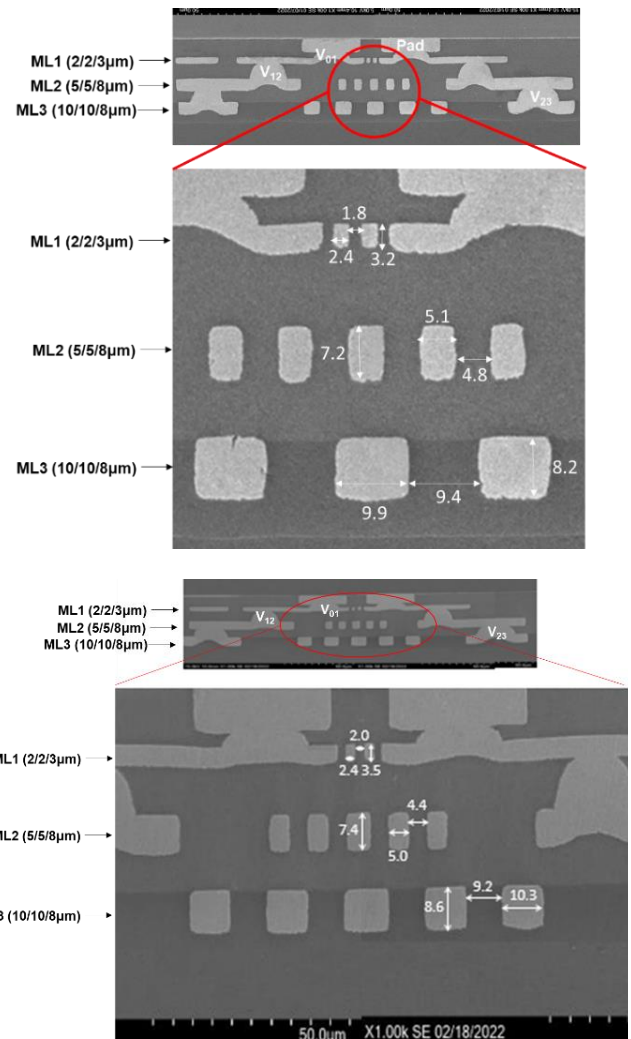


Fig. 7 Images of the cross section of the fine metal L/S/H RDL substrate.

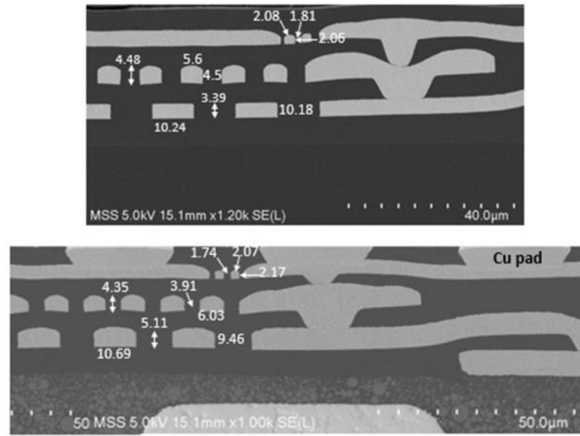


Fig. 8 Image of the fine metal L/S RDL substrate with PID [11, 12].

Figure 8 shows the image of the fine metal L/S/H RDL-substrate with PID as dielectric material. It can be seen that the metal lines are not as flat as those shown in Figure 7 with ABF as dielectric material.

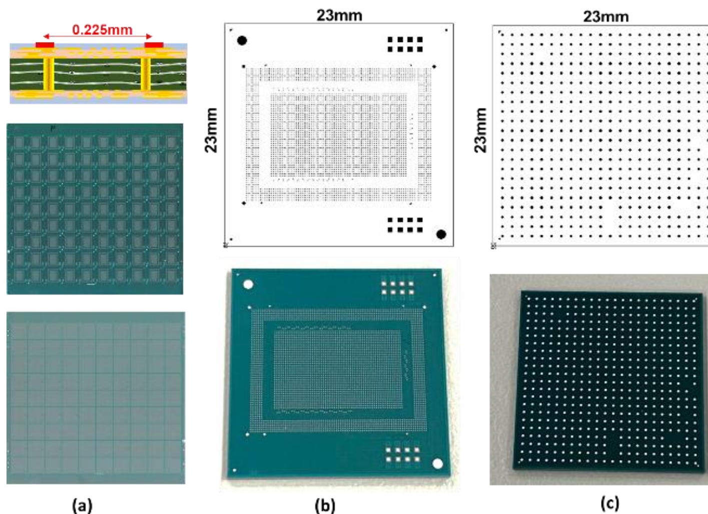


Fig. 9 (a) Panel for fabricating the build-up substrate. (b) Top view. (c) Bottom-view.

V. BUILD-UP PACKAGE SUBSTRATE

Figure 9 shows the top-view and bottom-view of the 2-2-2 build-up package substrate (23 mm × 23 mm × 1.3 mm) which is also made from an ABF with SiO_2 normal filler (Table 1), and its cross section is shown in Figure 10. The C4 bumps are fabricated by stencil printing a Sn3Ag0.5Cu solder paste with a 29-μm-thick stainless-steel stencil on the build-up substrate. During solder-reflow process, due to the surface tension of the molten solder, which creates smooth truncated spherical 30-μm diameter solder bumps [11, 12].

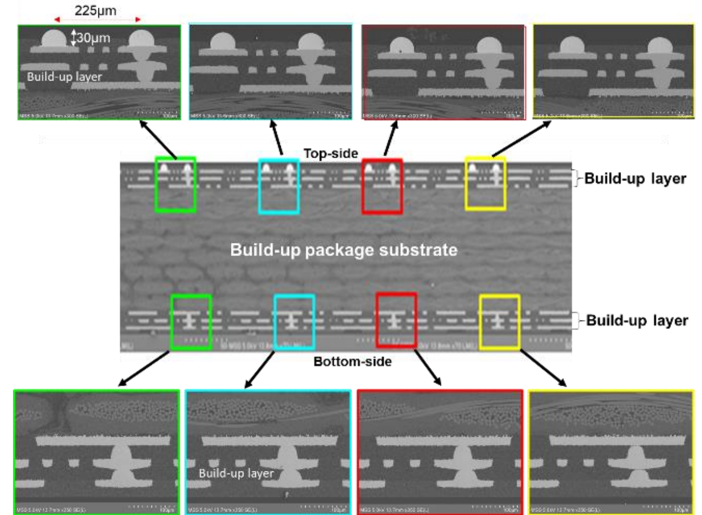


Fig. 10 Cross section of the build-up substrate.

VI. HYBRID SUBSTRATE

The hybrid substrate is fabricated by combining (assembling) the fine metal L/S/H RDL-substrate (Figure 7) and the build-up package substrate with C4 solder bumps [13] (Figure 10). In order to remove the contamination from the Cu pads of the fine metal L/S/H RDL-substrate, first apply water-soluble flux (Wf-6070SP-6-1) at the fine metal L/S/H RDL-substrate. It is followed by placing the RDL-substrate on a hot plate and heating up to 190°C for 2.5 minutes and cooling down then rinse with warm water. Then, the flux (WF 6317) is applied on the build-up package substrate.

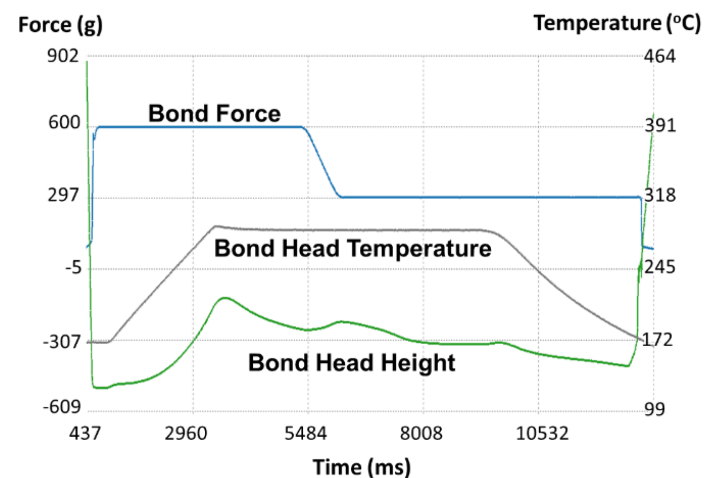


Fig. 11 Hybrid substrate bonding profile.

The bonding profile of the assembly is shown in Figure 11. It can be seen that the bond head temperature at contact is 170°C, the bond stage temperature is 175°C, and the bonding temperature is 285°C for 6s. The bonding force is reduced from 600g to 300g during bonding. Flux cleaning is by hot

water shower. A typical sample of the hybrid substrate assembly is shown in Figure 12. It can be seen the top views of the hybrid substrate with and without the temporary glass carrier. It can also be seen the cross section which consists of the build-up substrate, RDL-substrate, and the C4 solder joints. The hybrid substrate is properly assembled.

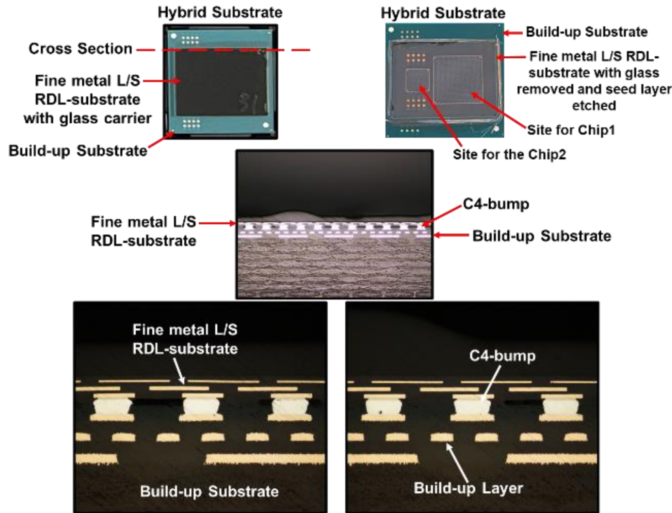


Fig. 12 Hybrid substrate, Top view and cross-sectional view.

Figure 13 shows the metal lines (ML1, ML2, and ML3) in the hybrid substrate fabricated with the ABF (top) and the PID in [11, 12] (bottom). It can be seen that the metal lines with ABF are much flatter than those with PID. However, the hybrid substrate fabricated with ABF is thicker than that with PID.

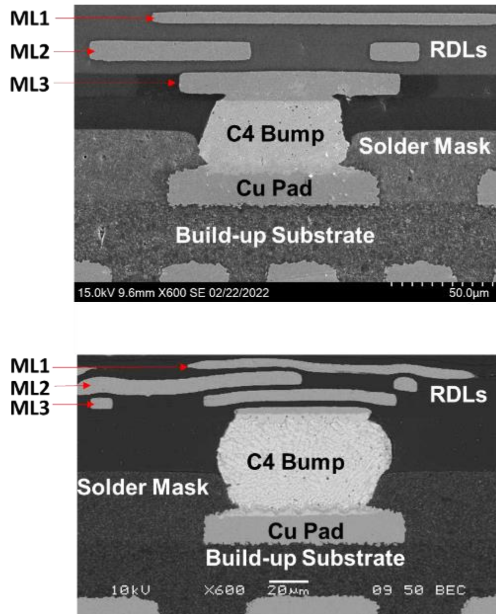


Fig. 13 Images of the fine metal lines in the hybrid substrate. Top (ABF). Bottom (PID).

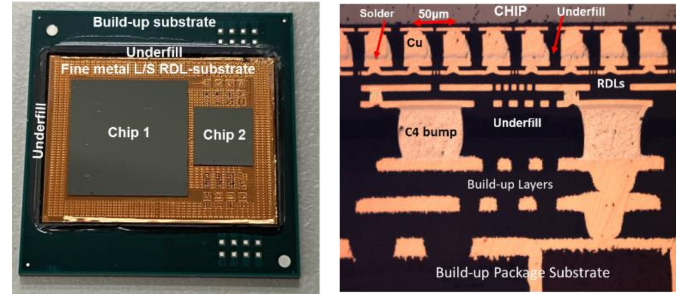


Fig. 14 Top view and cross section view of the assembly.

VII. FINAL ASSEMBLY

The final assembly of the heterogeneous integration of chips on the hybrid substrate is performed by chip-to-substrate bonding. Figure 14 shows the top view and cross section view of the assembly.

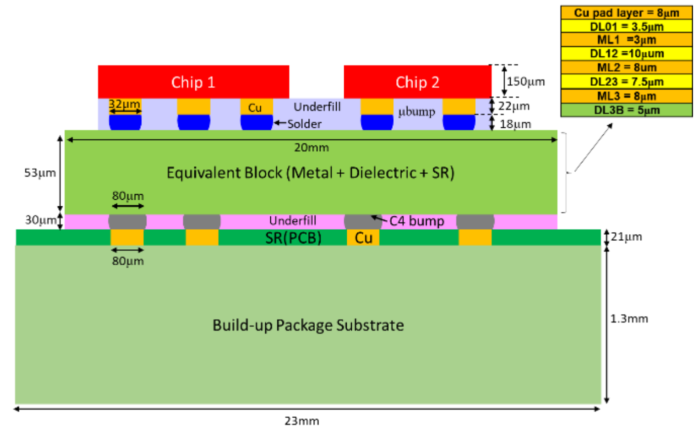


Fig. 15 Cross section of structure for modelling.

VIII. FINITE ELEMENT SIMULATION

(A) Assumptions

The first assumption of the analysis is to use an equivalent block (53µm-thick) to represent the fine metal L/S/H RDL-substrate as shown in Figure 15. The material property of the structure is shown in Table 3. The equivalent Young's modulus, equivalent CTE (coefficient of thermal expansion), and equivalent Poisson's ratio are calculated as below.

For equivalent Young's modulus:

$$\frac{121\times(8+3+8+8)+7.5\times(3.5+10+7.5)+7.5\times5}{(8+3+8+8)+(3.5+10+7.5)+5} = 65.32\text{GPa}$$

For equivalent CTE:

$$\frac{16.3\times(8+3+8+8)+37\times(3.5+10+7.5)+37\times5}{(8+3+8+8)+(3.5+10+7.5)+5} = 26\times10^{-6}/^{o}\text{C}$$

For equivalent Poisson's ratio:

TABLE 3 Material Properties for modelling.

Material	Young's modulus (GPa)	Poisson's ratio	CTE (10^{-6}/°C)
Silicon	131	0.278	2.8
Copper	121	0.34	16.3
Solder	49 - 0.07T(°C)	0.3	21 +0.017T(°C)
Underfill	4.5	0.35	50
ABF	7.5	0.3	37
Solder Mask (RDL)	7.5	0.3	37
Equivalent block	65.32	0.32	26.45
Solder Mask (PCB)	4.1	0.3	39
PCB	$E_x = E_y = 22$; $E_z = 10$	0.28	$A_x = \alpha_y = 18$; $\alpha_z = 70$

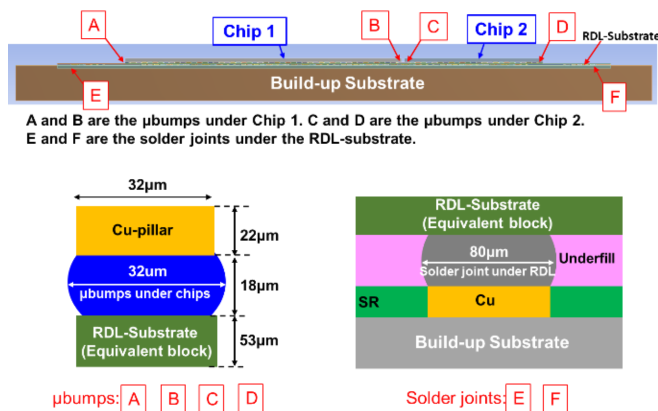


Fig. 16 Structure, µbump, and solder joint.

The second assumption is that the 2D generalized plane-strain method is adopted in this study.

(B) Finite Element Modelling

Figure 16 shows the cross section of structure for simulation. The bumps between the chips and the fine metal L/S/H RDL-substrate are µbumps (A, B, C, and D) and the bumps between the RDL-substrate and the build-up substrate are C4-bumps (E and F). Figure 17 shows the finite element model. It can be seen that finer meshes have been used for the critical µbumps B and C. All the other bumps are not shown in Figure 17.

The material properties of the structural elements are shown in Table 3. It can be seen that all the materials are assumed to be constants except the Sn3Ag0.5Cu solder, which is assumed to obey the generalized Garofalo creep equation [13]:

$$d\varepsilon/dt = 500{,}000\ [\sinh(0.01\sigma)]^5 \exp[-5{,}800/T(\mathrm{k})],$$

where ε is the strain, σ is the stress in Pa, and T is the temperature in Kelvin. The CTE and Young's modulus of the solder are, respectively, 21.3 + .017T and 49 - .07T, and T is the temperature in Celsius.

$$\frac{0.34\times(8+3+8+8)+0.3\times(3.5+10+7.5)+0.3\times5}{(7+3+8+8)+(3.5+10+7.5)+5} = 0.32$$

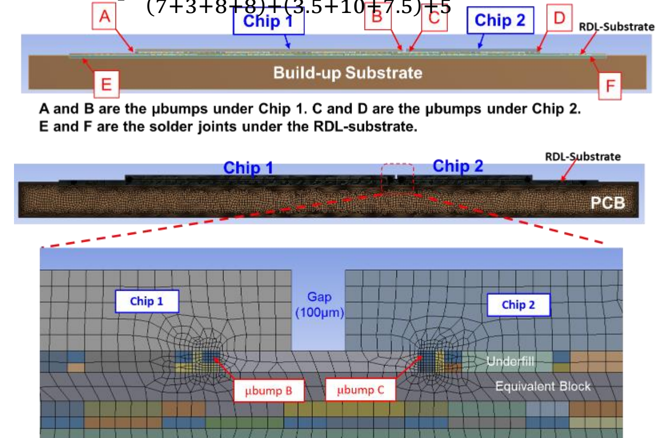


Fig. 17 Finite model for structural analysis.

The kinetic boundary condition is thermal cycling. Five temperature cycles are executed, and the temperature profile is: -40 ⇆ 85°C. The cycle time is 60 minutes and the ramp-up, ramp-down, dwell-at-hot, and dwell-at-cold are each 15 minutes

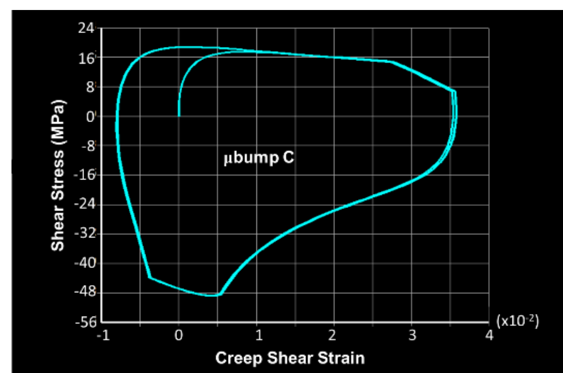


Fig. 18 Creep shear strain – shear stress hysteresis loops of µbump C.

(C) Simulation Results – Hysteresis Loops

It is important to study the creep responses for multiple cycles by observing when the hysteresis loops become stabilized. Figure 18 shows the creep shear strain – shear stress hysteresis loops at µbump C. It can be seen that the creep shear strain vs. shear stress loop is stabilized after the second cycle.

(D) Simulation Results - Deformations

The deformed shape and undeformed shape of the structure are shown in Figure 19. It can be seen at 450s (85°C), the hybrid substrate expands more than the chips and the structure is deformed in a concave shape (smiling face), Figure 19(a). At 2250s (−40°C), the hybrid substrate shrinks more than the chips and the structure is deformed into a convex shape (crying face), Figure 19(b).

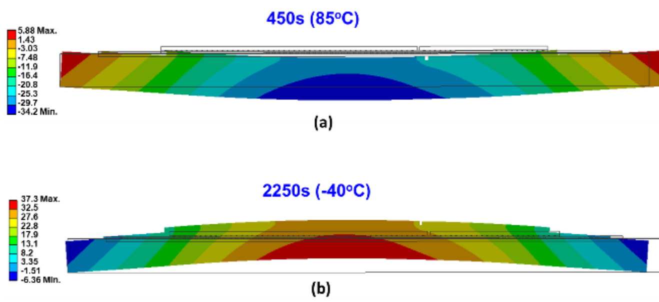


Fig. 19 Deformed shape (color contours) and un-deformed shapes (dark lines) of the structure at (a) 450s and (b) 2250s.

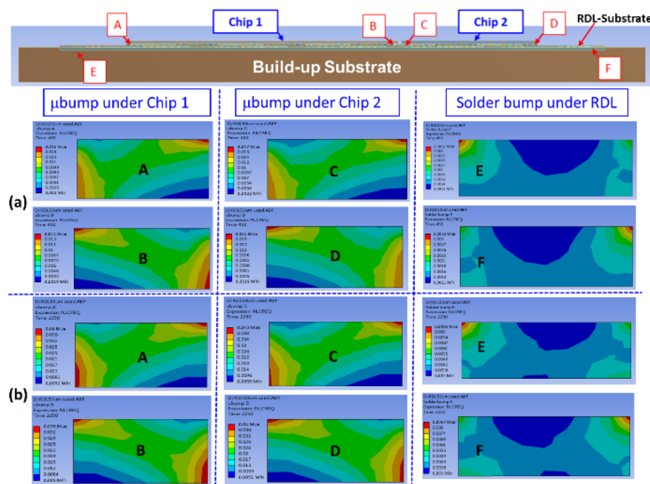


Fig. 20 Accumulated creep strain contours at various µbumps and solder joints.

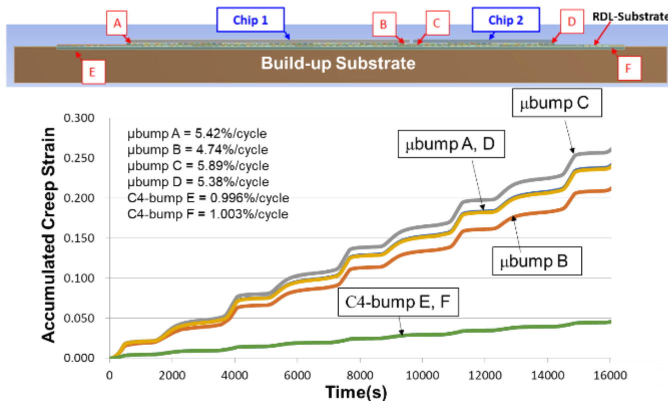


Fig. 21 Maximum accumulated creep strain time history at various µbumps and solder joints.

(E) Simulation Results – Accumulated Creep Strain

The accumulated creep strain contour distributions at the critical µbump solder joints A, B, C, and D and the critical C4-bump solder joints E and F are shown in Figure 20 and the maximum accumulated creep strain time history at these locations are shown in Figure 21.

It can be seen that the maximum accumulated creep strain occurs near the corner of all the joints A, B, C, D, E, and F. Also, the maximum accumulated creep strain per cycle in the µbump solder joints A, B, C, and D is at least four times larger than that in the C4-bump solder joints E and F. This is because the thermal expansion mismatch between the chips and the RDL substrate is larger than that between the RDL substrate and the build-up package substrate. Also, the solder volume of the µbump solder joints is smaller than that of the C4-bump solder joints. Furthermore, the stiffness of the µbump could be larger than that of the C4-bump. The maximum accumulated creep strain per cycle in the µbump joints is 5.89% and it occurs at a very small area. Thus, this structure should be reliable for most operating conditions.

(F) Simulation Results – Creep Strain Energy Density

The creep strain energy density contour distributions at the µbump joints A, B, C, and D and the C4-bump solder joints E and F are shown in Figure 22 and the maximum creep strain energy density time history at these joints are shown in Figure 23. It can be seen that the maximum creep strain energy density occurs near the corner of the joints A, B, C, D, E, and F. Also, the maximum creep strain energy density per cycle in the µbump joints A, B, C, and D is at least six times

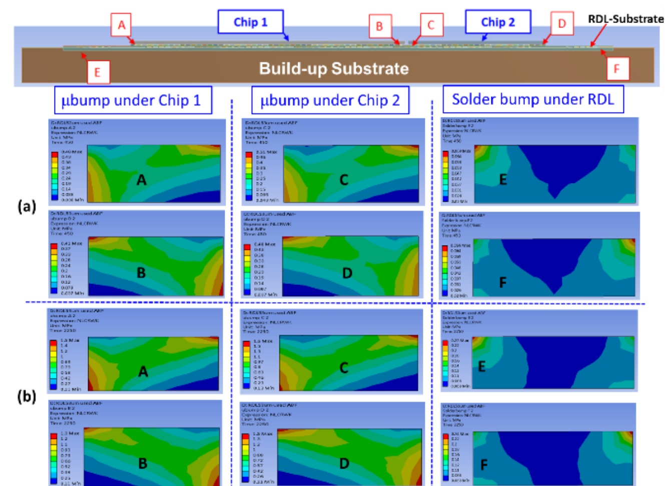


Fig. 22 Creep strain energy density contours at various µbumps and solder joints.

larger than that in the C4-bump solder joints E and F. Again, this is because the thermal expansion mismatch between the chips and the RDL substrate is larger than that between the RDL substrate and the build-up package substrate. The maximum creep strain energy density per cycle in the µbump joints is only 2.61 MPa and it occurs at a very small area. All the other areas have very small creep strain. Again, this structure should be reliable for most operating conditions.

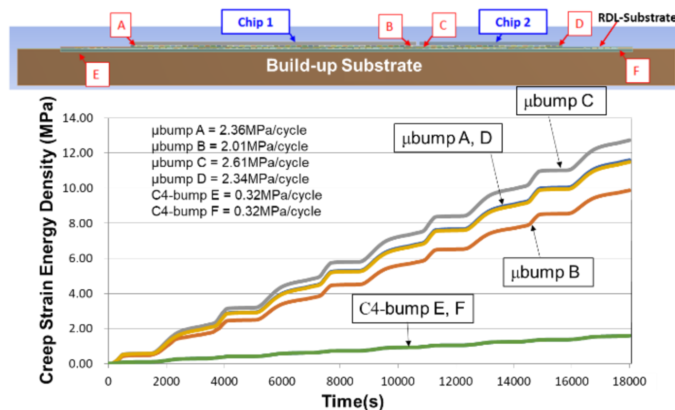


Fig. 23 Maximum creep strain energy density time history at various µbumps and solder joints.

XIII. SUMMARY

Some important results and recommendations are summarized as follows.

- The design, materials, and assembly process of the fine metal L/S/H RDL-substrate with ABF have been provided and the SEM images have been demonstrated the RDL-substrate has been properly done.
- The SEM images of the build-up package substrate have been demonstrated the substrate and the C4 bumps have been properly done.
- A hybrid substrate with ABF for heterogeneous integration of two chips has been developed. This hybrid substrate is fabricated by combining the fine metal L/S/H RDL-substrate and the build-up package substrate with solder joints which are enhanced with underfill. The dielectric material for the fine metal L/S/H RDL-substrate is the ABF instead of the PID used in [11, 12].
- The metal lines of the fine metal L/S/H RDL-substrate made by ABF are much flatter that those made by PID. However, the thickness of the fine metal L/S/H RDL-substrate made by ABF is thicker than that made by PID.
- The thermal reliability of a heterogeneous integration of two chips on the hybrid substrate has been performed through finite element method and demonstrated.
- Drop test on the heterogeneous integration final assembly is recommended.

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