Abstract
The state-of-the-art and outlooks for 2.3D IC integration will be investigated in this study. Emphasis is placed on the design, materials, process, advantages and disadvantages, challenges (opportunities), and examples of 2.3D IC integration for chiplet design and heterogeneous integration packaging. Also, some recommendations of 2.3D IC integration will be presented.

Key words
Fine metal L/S RDL-substrate, build-up package substrate, hybrid substrate, 2.3D IC integration,

(A) INTRODUCTION
The very first 2.3D IC integration paper was published by STATSChipPac [1] at IEEE/ECTC 2013. Their motivation is to replace the TSV-interposer (2.5D IC integration) by a fan-out fine metal L/S RDL-substrate (or organic interposer). The 2.3D structure consists of a build-up package substrate [or high-density interconnect (HDI)], solder joints with underfill [2, 3], and a fine metal L/S RDL-substrate, Figure 1. Since then, there are many publications [4-35]. [1, 4-6, 18, 20, 21] are by fan-out with chip-first packaging, while [7-33] are by fan-out with chip-last packaging.

For 2.3D IC integration by fan-out with chip-last (or RDL-first) packaging process [7-33], the fine metal L/S RDL-substrate and the build-up package substrate are fabricated separately. Kurita, Motohashi, et al. [7, 8], Huemoeller, Lim, Jayaraman, et al. [9, 10, 11], Suk, You, et al. [12, 13], Lin, et al. [14, 15, 16], Chang, Lai, Fang, Cao, Lee, Yin, et al. [17-23], and Li et al. [24] build the fine metal L/S RDL-substrate first, then bond the chips on the fine metal L/S RDL-substrate, underfilling and EMC (epoxy molding compound) molding, and finally assemble the module (chips + fine metal L/S RDL-substrate) on the build-up package substrate.

On the other hand, in Miki, Murayama, et al. [25, 26], Kim [27], and Lau, Chen, Peng, et al. [28-33], the fine metal L/S RDL-substrate and the build-up package substrate are first interconnected into a hybrid substrate through the solder joints that are enhanced with underfill [28-31] or through the interconnection-layer [32, 33]. Then, test the combined substrate and make sure it is a known-good hybrid substrate.

Finally, they bond the chips on the known-good hybrid substrate. In this case, the yield loss of the hybrid substrate especially the fine metal L/S RDL-substrate is easier to control and smaller. Also, there is a very little chance to lose the known-good dies. Furthermore, the logistic is simpler; after receiving the known-good hybrid substrate from the substrate houses, the OSAT (outsourced semiconductor assembly and test) houses just bond the chips/HBMs on the known-good hybrid substrate.

In this study, the recent advances and trends of 2.3D IC integration will be discussed. Some of the challenges (opportunities) of 2.3D IC integration will also be presented.
Finally, some recommendations of 2.3D IC integration will be presented.

(B) 2.3D IC INTEGRATION WITH FAN-OUT (CHIP-FIRST) PACKAGING

(B1) STATSChipPac’s 2.3D eWLB (Chip-First)
At ECTC2013, STATSChipPac proposed [1] using the chip-first fan-out flip chip (FOFC)-eWLB (embedded wafer level ball grid array) to make the RDLs for the chips to perform mostly lateral communications, Figure 2. Their objective is to replace the TSV-interposer, microbump, and underfill by the fine metal L/S RDL-substrate.

(B2) MediaTek’s Fan-Out (Chip-First)
During ECTC2016, MediaTek [4] proposed similar TSV-less interposer RDLs fabricated with fan-out chip-first wafer-level packaging technology as shown in Figure 3. Instead of the C4 bumps like Figure 2, they used a microbump (Cu-pillar + solder cap) to connect the bottom RDL to a 6-2-6 package substrate.

(B3) ASE’s FOCoS (Chip-First)
During ECTC2016, ASE [5] proposed using the fan-out wafer-level packaging technology (chip-first and die-down

Fig. 2 STATSChipPac: fanout (chip-first)

Fig. 3 MediaTek: fanout (chip-first)

Fig. 4 ASE: fanout (chip-first)

Fig. 5 TSMC: fanout (chip-first)

(B4) TSMC’s InFO_oS and InFO_MS
Figure 5 schematically illustrates TSMC’s fan-out RDL-substrates for heterogeneous integrations [6]. Figure 5(a) shows the integrated fan-out on substrate (InFO_oS) for heterogeneous integration, which eliminates the micro bumps, underfill, and TSV interposer with the RDLs. Figure 5(b) shows the integrated fan-out with memory on substrate
(InFO_MS), which is meant for higher performance applications.

![Fig. 6 Amkor: fanout (chip-last) and chip bonding first](image)

**(C) 2.3D IC INTEGRATION WITH FAN-OUT (CHIP-LAST) PACKAGING**

For 2.3D integration with fan-out (chip-last or RDL-first) packaging, the fine metal L/S RDL-substrate and the build-up package substrate are fabricated separately. Then, there are at least two different assembly processes: (a) bond the chips/HBM onto the fine metal L/S RDL-substrate first and then assemble the module (chips/HBM + fine metal L/S RDL-substrate) on the build-up package substrate as will be shown in sections (C1) through (C6), and (b) first combine the fine metal L/S RDL-substrate and the build-up package substrate into a hybrid substrate and test to make sure it is a good substrate, and then bond the chips/HBM on the known-good hybrid substrate as will be shown in sections (C7) through (C9).

**(C1) NEC/Renesas’ Fan-Out (Chip-Last or RDL-First) Packaging**

The very first papers on fan-out RDL-first (chip-last) were published by NEC Electronics Corporation (now Renesas Electronics Corporation) at IEEE/ESTC 2010 [7] and IEEE/ECTC 2011 [8]. The FTI (feedthrough interposer) used in their SMAFTI (SMArt chip connection with FeedThrough Interposer) is a film with ultra-fine linewidth and spacing RDLs. The dielectric of the FTI is usually a SiO₂ or polymer, and the conductor wiring of the RDLs is Cu. The FTI not only supports the RDLs underneath the chip, but it also provides support beyond the edges of the chip. Area array solder bumps are mounted at the bottom-side of the FTI, which are to be connected to the next-level of interconnect such as the package substrate. Epoxy molding compound (EMC) is used to embed the chip and support the RDLs and solder bumps. For more information on FTI, please read [7, 8].

**(C2) Amkor’s SWIFT (Chip-Last)**

Since 2015 Amkor have been promoting their silicon wafer integrated fan-out technology (SWIFT) [9-11], which is very similar to [7, 8]. Figure 6 shows a typical cross section of SWIFT. It can be seen that the TSV-interposer is replaced by the fine metal L/S RDL-substrate, which is fabricated by a fan-out chip-last (or RDL-first) packaging process.

**(C3) Samsung’s Si-less RDL Interposer**

During ECTC2018, Samsung [12, 13] proposed the use of chip-last or RDL-first fan-out packaging to eliminate the TSV-interposer for high performance computing heterogeneous integration applications (Figure 7). First of all, the RDLs are built on a bare glass - either in a wafer or a panel format. In parallel, wafer bumping of the logic and HBM chips will be done. Then, the following processes are done: fluxing, chip-to-wafer or chip-to-panel bonding, cleaning, underfill dispensing and curing. Those steps are followed by EMC compression molding. Then, backgrinding the EMC, chips, and HBM cube and C4 wafer bumping are done. After those steps, one can attach the whole module on the build-up package substrate. Finally, solder ball mounting and lid attachment are done. Samsung called the resulting structure a Si-less RDL interposer [12].

Samsung’s test vehicle is shown in [13]. The RDL interposer is 55mm x 55mm and consists of 5-RDLs including bonding layer, signal and ground layers. Samsung showed that the thermal cycling performance of the C4 solder joint in the organic-interposer module is better than that of the TSV-interposer module [13]. This is because of the thermal expansion mismatch between the silicon-interposer and build-up package substrate is larger than that between the organic-interposer.

**(C4) TSMC’s Multilayer RDL Interposer (Chip-Last)**

Figure 8 shows TSMC’s multilayer RDL-interposer for heterogeneous device and module integration [14, 15, 16]. The structure consists of: (a) the chips are attached on an organic or inorganic RDL interposer with microbumps and underfill, (b) the RDL interposer is attached to a build-up package substrate with C4 bump with underfill, and (c) the
package substrate is attached to a PCB with BGA (ball grid array) solder ball. Figure 8 shows some images of the assembly. It can be seen that the chips and DRAM are attached to a multilayer RDL-interposer with μbumps and then attached to a package substrate with C4 bumps. There are 6 RDLs with various via structures such as stagger vias, two stacking vias, and four stacking vias. Recently, they integrated both a large amount of high density integrated passive devices (IPDs) and fine pitch Si-based connection block of convenient IP migration [16].

Fig. 8 TSMC: fanout (chip-last) and chip bonding first

Vias. In parallel, they perform the wafer bumping for the microbump. Then, they perform the chip-to-RDL-wafer bonding, underfilling, and molding. It is followed by debonding the temporary carrier, C4 bump mounting, and dicing into individual modules. Finally, the module is attached on a build-up package substrate. Recently, they have demonstrated the electrical, thermal, mechanical and reliability performance of their fan-out chip-last 2.3D packaging [17-23] and renamed the FOCoS to FOBGA (fan-out ball grid array) [21].

Fig. 10 ASE: fanout (chip-last) and chip bonding first

(C5) ASE’s FOCoS (Chip-Last)
Figures 9 and 10 show ASE’s FOCoS with fan-out chip-last process [17-23]. First, they fabricate an RDL-interposer on a temporary glass carrier. It can be seen from Figure 12 that there are at least 4 RDLs with stacked vias and non-stacked vias. In parallel, they perform the wafer bumping for the microbump. Then, they perform the chip-to-RDL-wafer bonding, underfilling, and molding. It is followed by debonding the temporary carrier, C4 bump mounting, and dicing into individual modules. Finally, the module is attached on a build-up package substrate. Recently, they have demonstrated the electrical, thermal, mechanical and reliability performance of their fan-out chip-last 2.3D packaging [17-23] and renamed the FOCoS to FOBGA (fan-out ball grid array) [21].

Fig. 11 SPIL: fanout (chip-last) and chip bonding first

(C6) SPIL’s Large Size Fan-Out 2.3D (Chip-Last)
During IEEE/EPTC 2021, SPIL presented a paper on 2.3D IC integration [24] with a very large package size (6000mm²) and a 6-layer fine metal L/S = 2μm (minimum) RDL-substrate as shown in Figure 11. They demonstrated the qualifications such as the thermal cycling test and high temperature storage life test of their test vehicle.
(C7) Shinko’s 2.3D Organic Interposer (Chip-Last)
Figure 12 shows Shinko’s 2.3D organic interposer for high performance computing applications [25, 26]. It can be seen from Figure 12 that Shinko use NCF (non-conductive film) as the underfill between the organic interposer and build-up package substrate. Also, between the organic RDL interposer and the build-up package substrate, they use Sn-Bi solder alloy instead of the SnAgCu. In fabricating the organic RDL interposer they use a temporary carrier and a rigid layer, so they don’t have to switch to another temporary carrier before chip-to-panel bonding. Figure 12 shows the SEM images of the organic interposer (thin-film layer). It can be seen that the metal L/S are 2/2 μm with stacking vias. In parallel, they perform the wafer (Cu-pillar + solder cap) bumping. The pitch is 40 μm for the large chip and 55 μm for the small chip. The chip-to-panel bonding is by TCB (thermocompression bonding). Figure 12 shows the cross section of the assembly between the organic interposer and the build-up package substrate. It can be seen that the interconnect material is SnBi.

(C8) Samsung’s Cost-Effective 2.3D (Chip-Last)
At ECTC 2021, Samsung presented a cost-effective 2.3D packaging by using fanout panel level RDL [27]. Their fine metal L/S (7/8μm) RDL-substrate consists of a 3-layer coreless substrate with 2 RDLs and an eight-layer (3-2-3) package substrate as shown in Figure 13.

(C9) Unimicron’s 2.3D IC Integration (Chip-Last)
The feasibility of the design, materials, process, and fabrication of a heterogeneous integration of two chips with 50-μm pitch on a 2.3D hybrid substrate (Figure 14) by a fan-out RDL-first panel-level packaging has been demonstrated [28, 29, 30]. In order to increase throughput, the fine metal L/S (2μm) RDL-substrate has been fabricated on a temporary glass panel. The hybrid substrate has been fabricated by soldering the fine metal L/S RDL-substrate on a build-up package substrate and underfilled. The 50-μm pitch microbumped chips are bonded to the hybrid substrate and underfilled. Reliability of the assembly has been demonstrated by the thermal cycling simulation. It is found that: a) the creep response of the microbump solder joints between the chips and the RDL substrate is larger than that between the RDL substrate and the build-up package substrate and b) the maximum creep responses pre cycle are too small and localized to create reliability concerns in most operating conditions for mobile products. The hybrid substrate has been shown to pass the drop test [30].
In [28-30], the dielectric material for the fine metal L/S RDL-substrate is PID (photoimageable dielectric). Recently, the dielectric material has been changed to ABF (Ajinomoto build-up film), which leads to much flatter metal traces of the RDLs as shown in Figure 15 [31].

The fine-metal L/S RDL-substrate and the build-up package substrate, or HDI substrate, can also be combined through an interconnect layer [32, 33] into a hybrid substrate. This is very similar to [28-31] except the C4 solder joint and underfill are replaced by an interconnect layer as shown in Figure 16. For more information on the design, materials, process, fabrication, and reliability of the heterogeneous integration of three chips on a hybrid substrate with an interconnect layer by a fan-out RDL-first panel-level package, please read [32, 33].

(D) OTHER 2.3D IC INTEGRATION STRUCTURES

(D1) Shinko’s Coreless Organic Interposer
In 2012, Shinko proposed to use the coreless package substrate to replace the TSV-interposer (Figure 17). For sure, the cost in making the coreless substrate is much lower than that in making the TSV and RDLs (which require semiconductor equipment). Warpage could be an issue.

(D2) Cisco’s Coreless Organic Interposer
Figure 18 shows a heterogeneous integration designed and manufactured with a large organic interposer (TSV-less interposer) with fine-pitch and fine-line interconnections by Cisco [36]. The organic interposer has a size of 38mm x 30mm x 0.4mm. The minimum line width, spacing, and thickness of the front side and back side of the organic interposer are the same and are, respectively, 6μm, 6μm, and 10μm. It is a 10-layer high density organic interposer (substrate) and the via size is 20μm. The major manufacturing steps for making the organic interposer are the same as those for the organic build-up package substrate. These include a) plating through-hole (PTH) generation and filling for the core layer, b) circuitization of the core layer, and c) building Cu wiring layers on two sides of the core layer with SAP.

A high-performance application-specific IC (ASIC) die measured at 19.1mm x 24mm x 0.75mm is attached on top of the organic interposer along with four high-bandwidth memory (HBM) dynamic random-access memory (DRAM) die stacks. The 3D HBM die stack with a size of 5.5mm x 7.7mm x 0.48mm includes one base buffer die and four DRAM core dice that are interconnected with TSVs and fine-pitch micro-pillars with solder cap bumps. The pad size and pitch of the front side of the organic interposer are 30μm and 55μm, respectively. Figure 18 shows a top view of the organic interposer manufactured and the cross-sectional view of the good solder joint made between the HBM die-stacks and the organic interposer [36].
are attached to the inorganic interposer (RDLs) with microbump (Cu-pillar + solder cap). Then, the RDLs interposer is attached to the build-up package substrate with C4 bump.

(E) SUMMARY

Some important results and recommendations are summarized in the follows.

- 2.3D IC integration is meant to replace the 2.5D IC integration by combining the fine metal L/S RDL-substrate and the build-up package substrate into a hybrid substrate. Currently, it is in small volume production, and it will be in high volume production by the end of 2022. Eventually, 2.3D IC integration will take away some of the market shares from 2.5D IC integration.
- 2.3D IC integration with fan-out (chip-first) process is simpler and lower cost than that with fan-out (chip-last or RDL-first) process. However, the advantages of 2.3D IC integration with fan-out (chip-last) are for: (a) larger die size, (b) larger package size, (c) less die shift issue, and (d) finer metal L/S of the RDLs.
- For 2.3D IC integration with fan-out (chip-last), there are at least two different assembly processes: (a) first bond the chips/HBM on the fine metal L/S RDL-substrate and then assemble the module (chips/HBMs + fine metal L/S RDL-substrate) on the build-up package substrate, and (b) first combine the fine metal L/S RDL-substrate and the build-up package substrate into a hybrid substrate and test to make sure it is a good substrate, and then bond the chips/HBMs on the known-good hybrid substrate. Due to higher assembly yield, logistic, and less chance to lose the KGDs, the latter assembly process is recommended.
- there are at least two different processes, namely chip-bonding first (Figure 3) and chip-bonding last (Figure 4). Because of the simple logistic and less chance to throughout the known-good dies, it is recommended to use the chip-bonding last process (Figure 4).
- The ever increase demands for larger size of the fine metal L/S RDL-substrate and the build-up package substrate post great challenges (opportunities) on designs, materials, processes, and assemblies in high-yield manufacturing. Due to the large size of the structure and the thermal expansion mismatch among the structural elements, reliability could be an issue.
- The ever increase demands for smaller feature size (down to submicron) of the fine metal L/S RDL-substrate post great challenges (opportunities) on designs, materials, processes in high-yield manufacturing.
- Besides the 2.3D IC integration with fan-out packaging technology, there are other 2.3D IC integration structures such as those given by Shinko (coreless substrate), Cisco (organic interposer), Amkor (SLIM), and SPI (NTI).

(D3) Amkor’s SLIM

Figure 19 shows Amkor’s SLIM (silicon-less integrated module) [9, 11, 37, 38]. The key difference between SWIFT and SLIM is that hybrid RDL is used for SLIM. In order to lower the metal L/S (go down to submicron), the hybrid RDL is fabricated with inorganic RDL first and organic RDL last. Figure 19 shows the 0.5 μm metal L/S (RDL1) made by the semiconductor process and equipment (inorganic RDL method) and RDL2 and RDL3 made by the polymer and ECD (organic RDL method).

(D4) SPI’s NTI

During ECTC2016, SPI proposed the NTI (non-TSV interposer) for 2.3D IC integration with coreless inorganic interposer [39]. First, they used the 65nm process technology to make the RDLs with a 0.4 μm-pitch minimum on a wafer. Then, they performed the chip-to-wafer bonding on the RDLs, underfilled the gap between the chips and the RDL interposer and molded the chips with EMC. Figure 20 shows the cross section of the assembly. It can be seen that the chips

Fig. 19 Amkor’s SLIM

Fig. 20 SPI’s NTI
REFERENCES


