Double Sided Integrated GaN Power Module with Double Pulse Test (DPT) Verification

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Abstract

Wide Bandgap devices (WBG) have led to an era of high speed and high voltage operations that were not previously achievable with silicon devices. However, packaging of these devices in the power module has been a challenge due to higher switching rates which can cause several amperes of displacement current to flow through the parasitic capacitance of the package thus impacting the gate driver operation and the switching ability of the device. The severity of this current increases in thin packaging substrates unlike the traditional inorganic substrates e.g. DBC and thus a thorough investigation is needed before it can be used with WBG semiconductors. The objective of this paper is to discuss ways to reduce as well as manipulate the parasitic capacitance at different locations in the power modules to reduce the magnitude of the peak and RMS value of the displacement current and have a better gate drive signal and power waveform. To study this, a Double Pulse Test (DPT) simulation study has been conducted to show how an intelligent distribution of parasitic capacitance benefits the device functioning. This has been validated through experimental fabrication and DPT of dense power module following proposed guidelines. A detailed description of the design of a high-speed capable DPT circuit and measurement setup has been specified to show the steps needed for reliable testing and measurement.

Key words

GaN power module; thin substrate; substrate current; coupling capacitance; Double Pulse Test.

I. Introduction

Modern WBG power semiconductor devices, such as SiC and GaN transistors, have switching frequencies to 10MHz for Power Electronics Converter applications due to their low C_{oss}. This makes highly efficient and high dv/dt operation possible [1], [2]. Such devices are gaining even more acceptance in consumer and industrial applications. They are used in Solid State Transformer for creating high DC link voltage and in Traction applications for creating dense power modules with high switching frequency capability, higher power handling capacity with smaller die size [3] [4]. Though the devices can operate at temperatures up to 500ºC the packaging materials are limiting use to 175ºC. Most commercial power modules are packaged with ceramic-based substrates that have high thermal conductivity and can operate to at least 250°C [5]. However, the thermal resistance can be high due to the typical thicknesses of 635um to 1mm for Al_2O_3. Compared to ceramics, recent organic based thin substrates using epoxy resin composite dielectrics (ERCD) loaded with Al_2O_3 and AlN particles, can have thermal conductivities of one third that of traditional Al_2O_3 plate, but with thicknesses of only 80um to 120um the thermal resistance is lower than 380 µm Al_2O_3 and is available at 30% the cost [6]. Although, traditional PCBs use epoxy, the material has low thermal conductivity of 1-1.5W/m.K,limiting use in many high power and high speed converter power modules.

A 2D planar power module structure with a top copper and bottom copper layer separated by a dielectric leads to the formation of a coupling or parasitic capacitance. The thinner substrate, 80µm or 120µm, causes higher coupling capacitance leading to higher substrate and Common Mode (CM) currents occurring from high speed switching ($i = Cdv/dt$). Thus, a need for careful interconnect layout is necessary for low parasitic inductance and capacitance in the power loop and gate drive circuitry [7]. Consequently, combination of high dv/dt, coupling capacitance, parasitic inductance, and base-plate grounding are all important in determining the reliable functioning of a power module.

Discussions on gate and power loop parasitic inductance have been a prevalent topic of discussion in the literature for preventing false tripping and managing voltage overshoot in conventional and advanced packaging structures for WBG semiconductors [8]–[10]. However, very little literature with a detailed study on the implications of coupling capacitance in power modules for fast switching transients application is available.

A study on the effect of coupling capacitance on single-sided cooled DBC has been carried out in [11]. It discusses the impact of such capacitance on WBG switching dynamics and substrate current which is a contributor to common mode (CM) current. A subsequent paper by the same authors talks about different heatsink/baseplate grounding techniques and layouts needed for better switching performance and lesser coupling coefficient [12]. However, reducing the surface area of copper trace at all locations may not only be detrimental thermally but even electrically as will be shown in this paper. The use of a low permittivity air cavity in the bottom copper underneath the switch node pad has been discussed in [13]. Although it reduces the coupling capacitance at the critical location of concern. It reduces the thermal performance of the module as air has a poor thermal conductivity and the cavity is below the device copper pad. Few papers talk about EMI suppression through interstitial layers in DBC substrates following an approach common in multi-layered PCB, where inner layers act as EMI shield to the baseplate [14], [15]. Although, this is a proven solution still, fabrication for thick DBC substrates from a commercialization point of view may be costly and may find more application in thin substrates (organics or thin Alumina). Additionally, such interstitial layers add to the thermal resistance. In [7], [16] it has been suggested that DC+ power supply trace C_{DC+} and DC- power supply trace C_{DC-} parasitic capacitance (Figure 1) have a higher value than that of the switching node C_{SN} parasitic capacitance to reduce CM current, this allows a portion of the baseplate current to circulate back within the module. Although, this is valid when the ratio of individual capacitances of C_{DC+} and C_{DC-} is much higher than C_{SN}, the author of this paper has found that this trend is not monotonically decreasing and that a specific ratio of capacitances should be maintained to minimize the RMS and peak CM current.

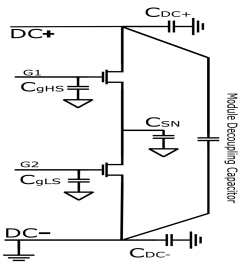


Fig. 1: Module Schematic.

The contribution of this paper is to provide an approach to the modification of the ratio of parasitic capacitance between the center point of the totem-pole switching node (C_{SN}), (C_{DC+}) and (C_{DC-}) such that the maximum amount of baseplate current passing through the C_{SN} returns back through decoupling capacitors, C_{DC+} and C_{DC-}, instead of returning through the isolation barrier of the main power supply to the circuit as opposed just increase or decrease in C_{DC+} and C_{DC-} as suggested in [7], [12], [16]. Coupling to the gate driver circuits is also considered in the simulation as both switch node and baseplate current circulate back through parasitic capacitance [17]. This is followed by detailed description of the design, layout, fabrication and electrical testing of a half-bridge (totem-pole) stack of two laterally conducting GaN power devices with integrated gate driver.

II. Module Design, Layout and Fabrication

The double-sided cooled GaN intelligent power module (IPM) integrates GaN power devices, gate drivers, and power and gate decoupling capacitors into a compact package for increased functionality, performance, and density. The topside of GaN devices is flip-chip bonded onto a highly thermally conductive epoxy-resin insulated metal substrates (eIMS) with a stackup of 4oz Cu/120um dielectric/2mm Cu. Different from traditional ceramic substrates (e.g. DBC), eIMS does not require an additional metal baseplate due to the integrated baseplate which reduces the potential failure point (solder layer between substrate and baseplate) and additional thermal interface, leading to better mechanical reliability and thermal performance. The backside of GaN devices is soldered on Copper (Cu) spacer for thermal spreading and electrical connection of Source to GaN Substrate.

A. Power Loop Design

Due to the fast-switching characteristics of GaN HEMT, minimizing the parasitic inductance is critical for maximizing the switching speed and power conversion efficiency. Hence, power decoupling capacitors are employed to decouple the parasitic inductance contributed by terminals and act as local source for transient charge supply for voltage stabilization. Additionally, the wire bondless and planar interconnection enable a parallel conductor plate structure and result in a significant magnetic field canceling. The power terminals are marked as DC+, DC-, and SN as as seen in Figure 2(d). This structure leads to a low power loop inductance of only 1.5nH.

As discussed in section I and shown through simulation in section III, proper ratio of C_{DC+} and C_{DC-} with respect to C_{SN} is necessary to reduce the substrate/baseplate current magnitude. Two different double sided module, one with proper capacitance ratio and one without has been designed with the same fabrication steps to show the difference in experimental results and validate the guidelines for capacitance ratio in section III. The balanced capacitance ratio based module has been referred as optimized module. Optimized and Non-Optimized

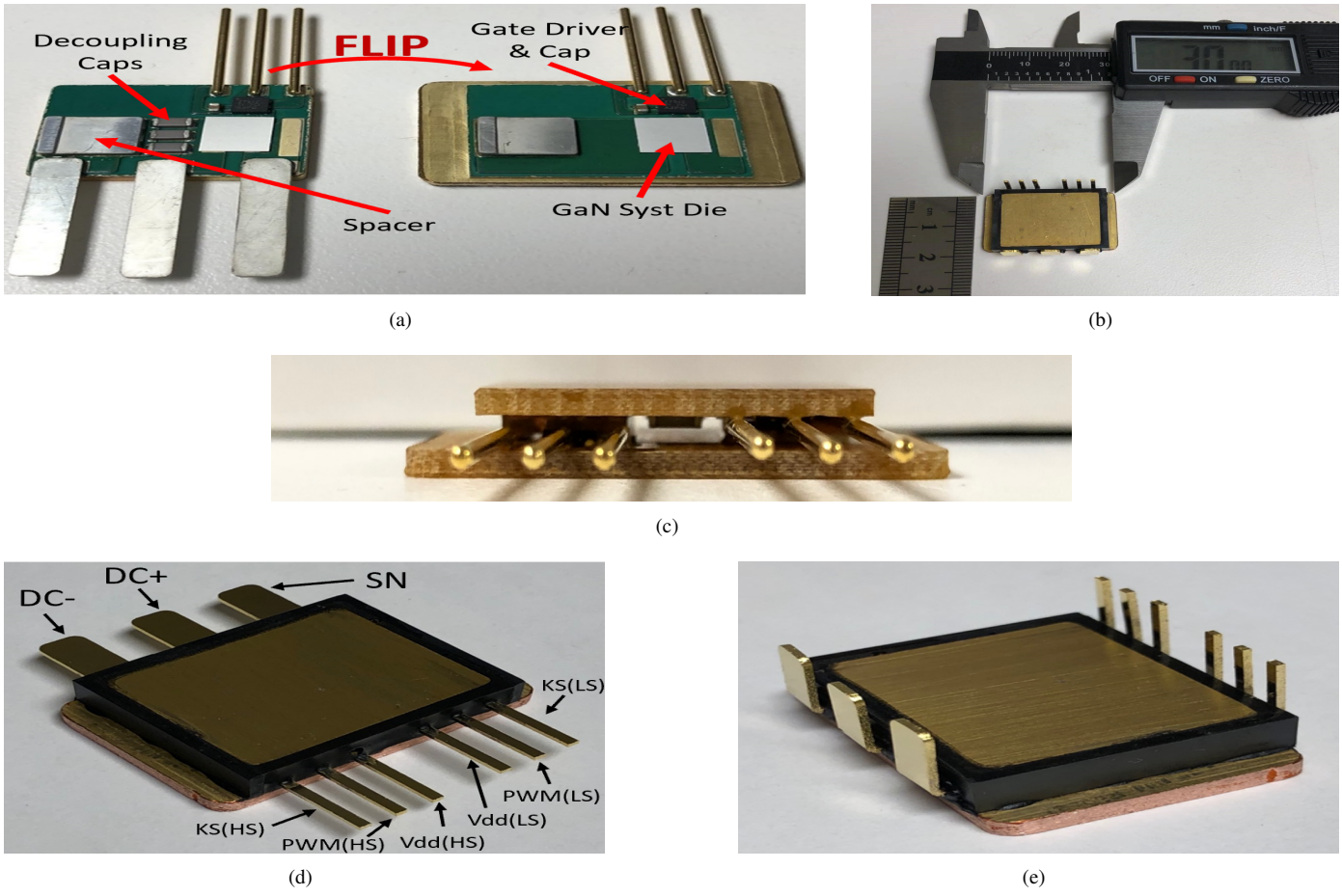
module's Capacitance values calculated through ANSYS Q3D have been shown in Table 4.

B. Gate Loop Design

The signal terminals: Vdd(HS/LS), KS(HS/LS), and PWM(HS/LS)) of Figure 2(d) are isolated from the power terminals with kelvin source KS(HS/LS) copper trace following guidelines for layout mentioned in [8] for lower crosstalk.

C. Fabrication

Figure 2(a-e) show the module fabrication process. The first step is the high temperature soldering for bonding GaN devices, gate drivers, capacitors, spacers and terminals on the left and right eIMS (Figure 2(a)) using Sn95Sb5 solder. Next, lower temperature solder joins the assembly together using Sn96.5Ag3Cu0.5 (or SAC305). Finally, a PPS plastic ring is attached to the bottom eIMS by a thermal-cure epoxy-based adhesive and the entire assembly is encapsulated with a thermal-cure epoxy molding compound. The terminals can be bent upward for single-sided cooling or be flat for double-sided cooling. The module size is 20 x 30 x 5.7 mm, excluding terminals.



(a) (b) (c) (d) (e)

Fig. 2: (a) Left and Right Assembly (b) Dimension of the module (c) Full assembly without encapsulation (d) Final power module with PPS plastic ring (e) Final power module with bent terminals

III. Simulation: Proof of Concept

Simulation was performed with varying C_{DC+} and C_{DC-} for a fixed C_{SN}. This was repeated twice with two different values of C_{SN} to show the efficacy and the sensitivity of the method. The values of C_{DC+}, C_{DC-} and C_{SN} are listed in Table 1. Different values for C_{DC+} and C_{DC-} were not considered in simulations as there was no effect on the magnitude of baseplate current.

For simulations with values of Table 1.a it can be seen in Figure 3 that as the value of C_{DC+} and C_{DC-} is increased from 37pF to 800pF the peak to peak substrate current through C_{SN} decreases from 29.1A to 7.8A. However, this trend does not continue and after C_{DC+} and C_{DC-} cross 800pF the peak to peak substrate current increases to 8.8A.

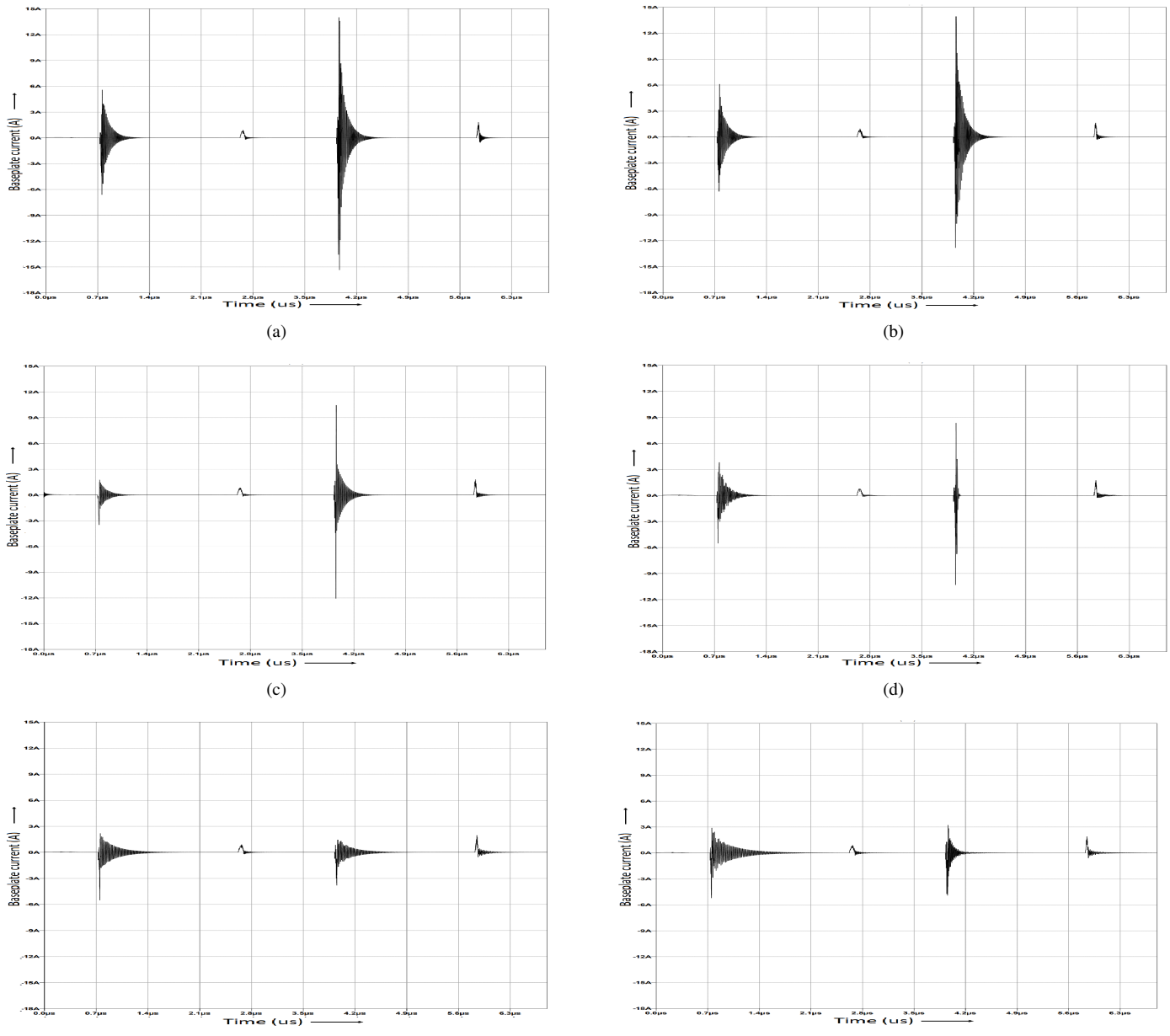
TABLE I: Parasitic Capacitance Values.

Table 1.a

Parameter	**Values (pF)**					
C_{DC+}	37	93	200	400	800	1200
C_{DC-}	37	93	200	400	800	1200
C_{SN}	93					

Table 1.b

Parameter	**Values (pF)**			
C_{DC+}	20	50	100	200
C_{DC-}	20	50	100	200
C_{SN}	5			



(a) (b) (c) (d) (e) (f)

Fig. 3: Baseplate current: (a) $C_{DC+/-}$ = 37pF (b) $C_{DC+/-}$ = 93pF (c) $C_{DC+/-}$ = 200pF (d) $C_{DC+/-}$ = 400pF (e) $C_{DC+/-}$ = 800pF (f) $C_{DC+/-}$ = 1200pF

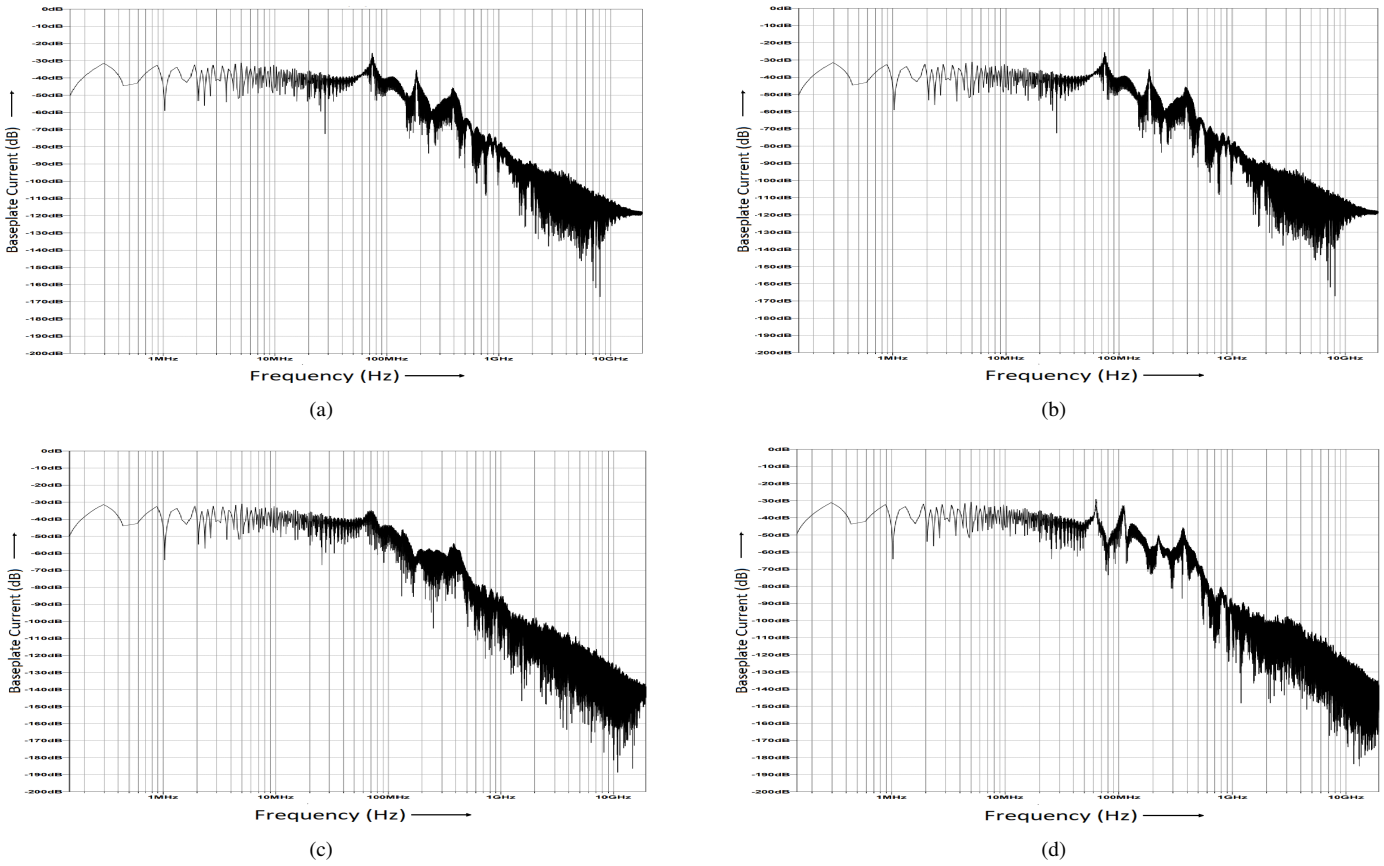


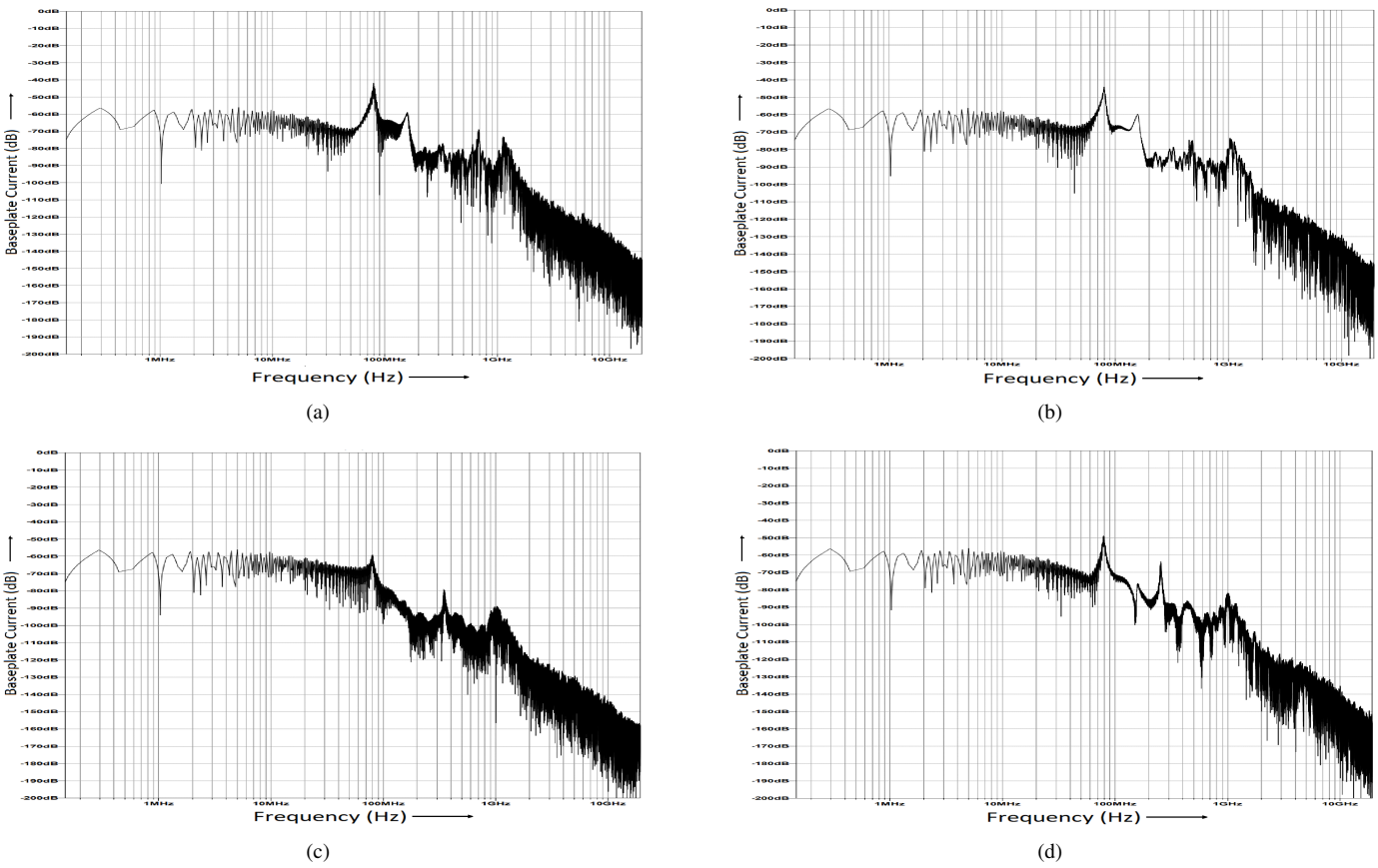
Fig. 4: FFT: (a) $C_{DC+/-}$ = 37pF (b) $C_{DC+/-}$ = 400pF (c) $C_{DC+/-}$ = 800pF (d) $C_{DC+/-}$ = 1200pF

A frequency domain analysis was also carried out to see the pattern of decrease and increase of the magnitude of the current in decibels(dB) over a range of frequencies. Frequency domain analysis helps to differentiate between conducted and radiated EMI in high frequency applications. From Figure 4(a) to Figure 4(b) there is no visible decrease in the dB but for Figure 4(c) there is a decrease in 10dB at 70MHz and above, which suggests a decrease in CM current at ringing frequencies above 70MHz. This helps in selecting the values of common mode transient immunity (CMTI) and the impedance of the components such as the choke and digital isolator (discussed in section IV) should offer for signal integrity of digital signals, probe bandwidth selection, and value of power/gate decoupling capacitor. Further, similar to the trend in time domain analysis, going from Figure 4(c) to Figure 4(d) there is an increase in 7dB at 70MHz and above suggesting detrimental operational performance of the module.

Authors have found that the idea of frequency domain analysis becomes exclusively important when the magnitude of C_{SN} is lower and changing C_{DC+} and C_{DC-} may not reflect much of a change in the time domain analysis but show significant change in the frequency domain. Such magnitude of capacitance can be common in modules laid out in X-Z dimensions instead of X-Y. No doubt packaging solutions aiming to decrease C_{SN} is always better as it decreases the amount of current passing through the substrate to the baseplate. Still, having the idea of a precise layout with the intelligent distribution of coupling capacitance (C_{DC+} and C_{DC-}) along with reduced C_{SN} allows enhancement of module switching performance even in scenarios where reduction of C_{SN} is not possible.

The time domain waveform from Table 1.b are not shown as they do not show visually much change. However, in Figure 5 there is a decrease of 3dB beyond 80MHz while going from Figure 5(a) to Figure 5(b) and a further increase of 14dB from Figure 5(b) to Figure 5(c). Again, in Figure 5(d) there is an increase of 10dB compared to in Figure 5(c). Thus frequency domain analysis aids in intricate design.

Hence, results show that only for a certain ratio of C_{DC+} and C_{DC-} with respect to C_{SN} does the current decrease. Precise tuning of capacitance ratio is important for larger area module such as three-phase or multi-die modules where the ratio is high. Although there is no general ratio capacitance applicable to all cases, the use of simulation for each case is necessary to understand and solve coupling current problem.



(a) (b) (c) (d)

Fig. 5: (a) FFT: $C_{DC+/-}$ = 20pF (b) $C_{DC+/-}$ = 50pF (c) $C_{DC+/-}$ = 100pF (d) $C_{DC+/-}$ = 200pF

IV. Design of DPT Circuit and Measurement

DPT is commonly used for measuring switching dynamics, however, high speed measurement requires special consideration in its layout, component selection, probe loading and EMI shielding. The circuit should be capable of handling high speed signals with high CMTI or less crosstalk.

A. Component Selection Criteria

A.1. Power Component Selection

The required inductor value is calculated using (1) which in conventional DPT circuit should achieve the load current after the first pulse. However, the purpose of the experiment in this paper is to measure the substrate current magnitude at various voltage edge rates and hence both pulse edges have been utilised to see the differential behavior in the magnitude of the substrate current through substantial change in the inductor current.For the circuit in Figure 6

$$L = V_{dc} * \frac{dI}{dt} \tag{1}$$

where, L is the inductor value needed to achieve the required load current at a certain $\frac{dI}{dt}$, V_{dc} is the DC bus voltage. A series combination of three inductors each with a value of 26uH has been used to reduce the effective winding parasitic capacitance to 22pF.

The value of the DC bus capacitor is calculated using (2) and in a double pulse these capacitors are what supplies the pulsed current. Hence,

$$C_{bus} = \frac{L * I^2}{(2 * V_{dc} - \Delta V_{dc}) * \Delta V_{dc}} \tag{2}$$

A capacitor of 330uF was found suitable and implemented with multiple film capacitors of 30uF, 50uF, 100uF for faster pulse delivery along with a 1MΩ bleeding resistor.

A.2. Gate driver and Signal Conditioning Component Selection

The gate charge Q_g for the device is 17.1nC. Thus the source and sink current for the driver are based on (3) for the desired t_r: rise time and t_f: fall time

$$I_{g,source/sink} = \frac{Q_g}{t_r/t_f} \tag{3}$$

The above calculation provides the minimum gate current i.e. I_g which the driver should support. The selected driver had a source/sink current of 4A/8A more than the minimum calculated.

One key aspect of the DPT board designed was a low isolation capacitance for minimal impact of the (CM) current generated due to the substrate current. To achieve higher module speed the selected gate driver is non-isolated hence isolation is provided through a digital isolator with a high CMTI of 100kV/us and isolation capacitance of just 1pF, whereas the DC-DC converters supplying the isolator and the gate driver have an isolation capacitance of 3.4pF. Thus for each path of the high side(HS) and low side (LS) switch the total capacitance is less than 5pF which is comparable to present research achievements elsewhere [18], [19].

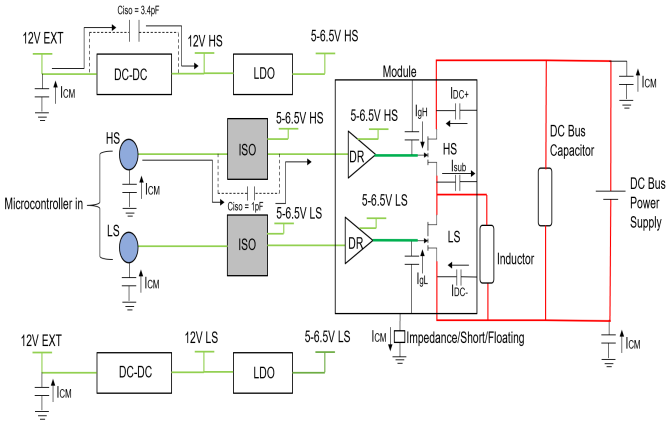


Fig. 6: DPT Schematic.

B. Measurement

The devices are from GaN Systems Inc. which for a typical >50A device, has a rise and fall time from 14ns to 22ns at a low current (16A) and although the edge rate at rated current is not provided in the datasheet, the devices are typically faster as the operating current increases. Hence, bandwidth of the probes and oscilloscope must be carefully selected. The device used in this module is rated 80A and operated near single digit nanoseconds edge rate. The minimum bandwidth of the measuring equipment can be calculated using (4) [20]:

$$HFI = \frac{0.35}{min(t_r, t_f)} \tag{4}$$

where, HFI stands for highest frequency of interest. Single ended voltage probes for measuring switching performance was selected to have at least 10 times bandiwdth of HFI.To monitor baseplate voltage differential probe was selected with a bandwidth of nearly twice the baseplate current ringing frequency. Monitoring of baseplate voltage was not critical but was used for checking proper grounding. The details of the probes have been listed in Table 2.

B.1. Voltage Measurement

As double sided module is inaccessible for measurements of the traditional Gate to source voltage (V_{gs}), drain to source voltage (V_{ds}) and switch drain current (I_d), the voltage across the positive DC+, DC- and the SN for the power signals and at the driver input signal pins between PWM(HS) and KS(HS) for high side driver voltage and between PWM(LS) and KS(LS) for low side driver voltage were measured. Any attempt of customised measuring solution in a dense module only deteriorate the module performance.

B.2. Current Measurement

Two types of current measurement were performed: one for inductor current and another for substrate current. It was determined through tests that the ringing frequency of the current was 60MHz, hence the bandwidth selection of the current probe as mentioned in Table 3. If the aim was to measure the switching performance then resistive shunts are preferable as they can have high bandwidth till 2GHz.

TABLE II: Voltage Probes for Driver and Power Signal.

Probe	RMS Voltage(V)	Peak Voltage(V)	Bandwidth(MHz)	Rise Time(ns)	Input Capacitance(pF)
TPP1000	300	Not mentioned	1000	0.35	3.9
TPP0850	1000	2500	800	0.43	1.8
THDP0100	2300	6000	100	<3.95	2.5

TABLE III: Current probe for Inductor Current and Baseplate Current.

Probe	RMS Current Rating(A)	Peak Current Rating(A)	Bandwidth(MHz)	Rise Time(ns)
TCP0030A	30	50	120	2.92

V. Experimental Results

The experiments were conducted with two different phase leg modules which have been named as optimized and non-optimized module as mentioned earlier. Figure 7 shows the DPT experimental setup of the schematic shown in Figure 6. The tests were performed with 400V DC bus voltage with phase-leg power module mounted on the board as shown in Figure 7(b). Both the phase-leg module varieties has two GaN devices of 650V/80A, three power decoupling capacitors of 4.7nF each, two gate drivers and two gate driver bypass capacitor of 1uF. Additional power decoupling capacitors of 1.5uF in total were placed on the power terminals to boost decoupling action as close as possible to the device pads. The modules were run with 0Ω gate resistance which allowed the highest dv/dt operation of the GaN switches, and consequently the worst-case CM current to be generated. All measurements were performed with the probes mentioned in Table 2 and 3. The DPT pulses were sent through TMS320F28335 microcontroller of Texas Instruments's C2000 series.

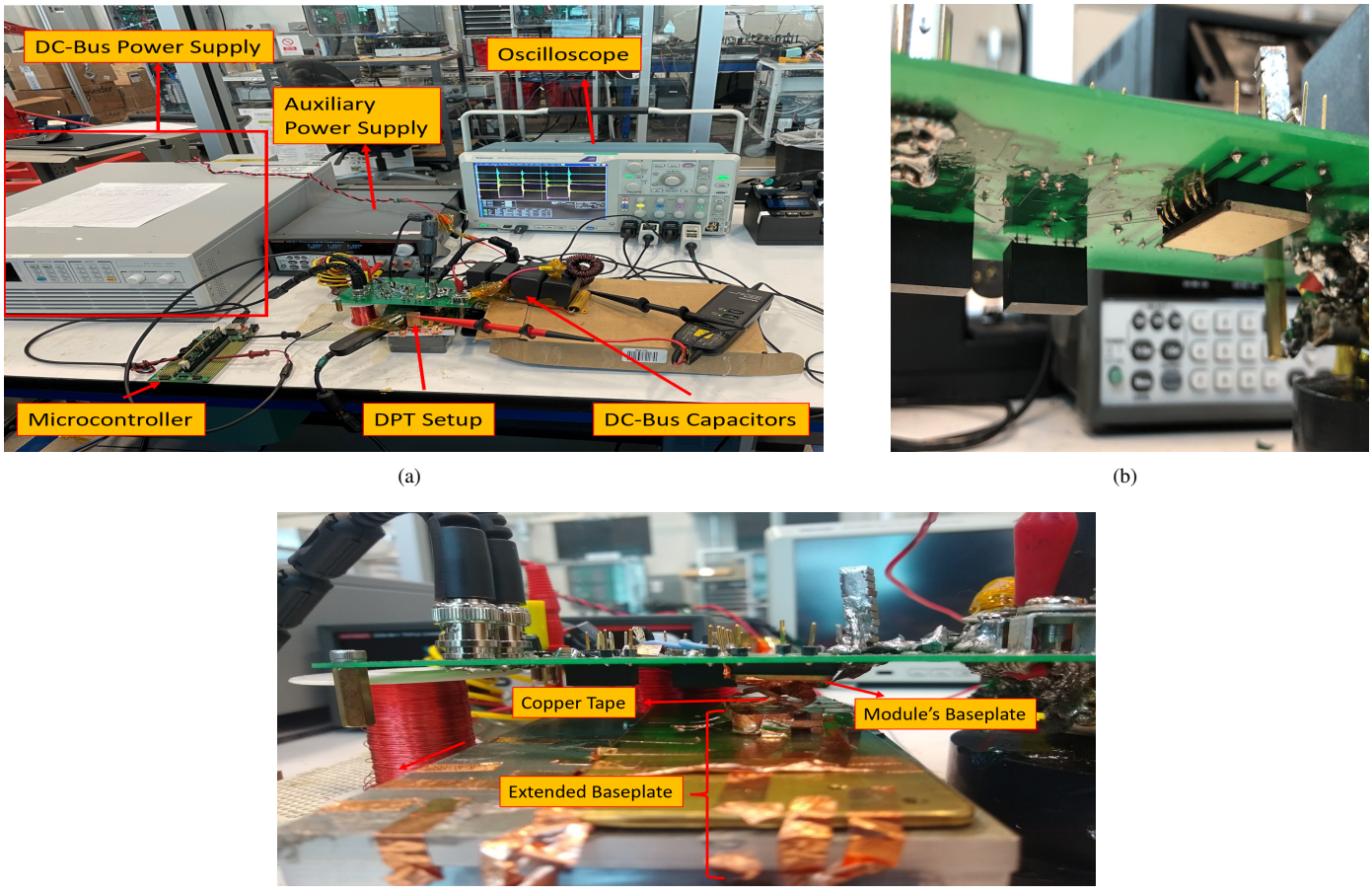


Fig. 7: (a) Experimental Setup (b) Phase-leg module mounted from the bottom side of the DPT board

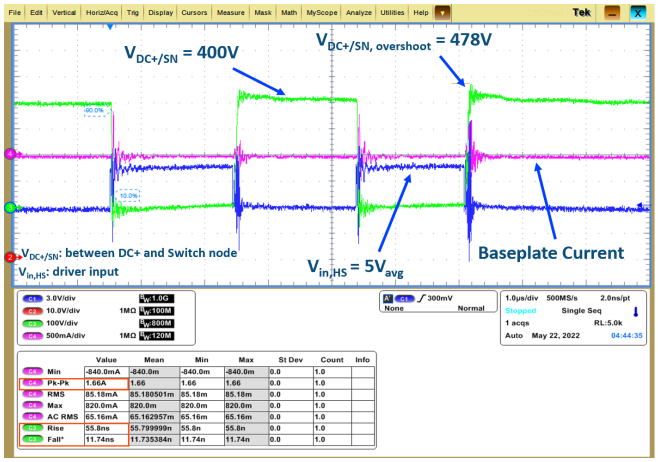
The results of the optimized and non optimzed module's experimental results have been categorised under two different baseplate grounding configurations: grounded baseplate and floating baseplate. The results presented in Figure 8 are for floating baseplate and Figure 9 are for grounded baseplate.

Figure 8 shows the voltage across the DC+ and SN terminal ($V_{DC+/SN}$), voltage at the baseplate, baseplate peak to peak current ($I_{b(pk/pk)}$) and PWM signal at the input of the HS gate driver i.e. PWM(HS) pin (denoted as: $V_{in,HS}$) during the switching event. The $I_{b(pk/pk)}$ current is the most important parameter as that is what is expected to reduce with the optimized module. However, other parameters should not show detrimental results in pursuit of improvement of just one parameter and hence has been measured as well. The $I_{b(pk/pk)}$

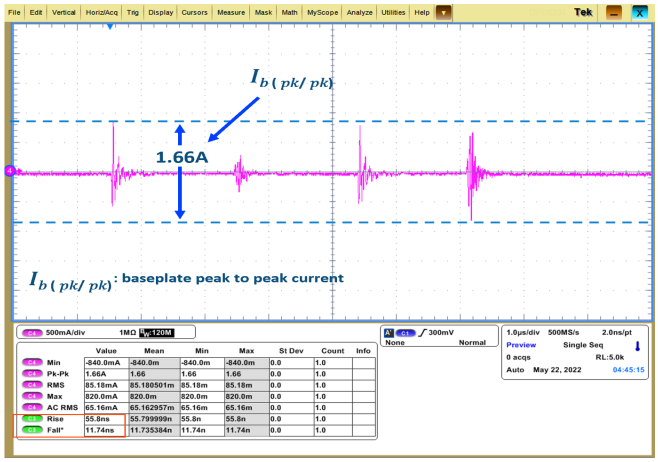
is measured considering all four switching events as shown in Figure 8(b). This is due to the measurement limitation of the oscilloscope hence, for individual switching events the magnitude may be slightly less. However, this deficit in measurement can be ignored for this analysis as the decrease is almost equal in all current magnitudes and thus just looking at the measured peak to peak value is acceptable. The magnitudes of parasitic capacitance for the non-optimized and optimized module are shown in Table 4. The layout has been modified such that C_{SN} is unchanged for fair comparison.

TABLE IV: Parasitic Capacitance: Optimized and non-optimized module.

Parameter	Values(pF)	
	Non-Optimized	Optimized
C_{DC+}	37	150
C_{DC-}	97	150
C_{SN}	93	
C_{gHS}	2.1	2.1
C_{gLS}	2.1	2.1



(a)



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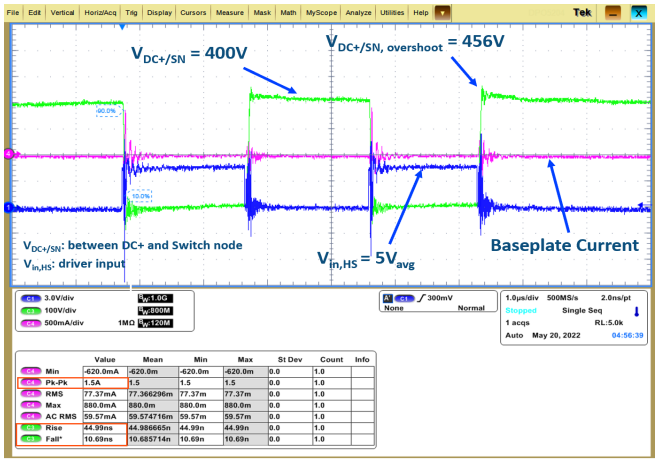

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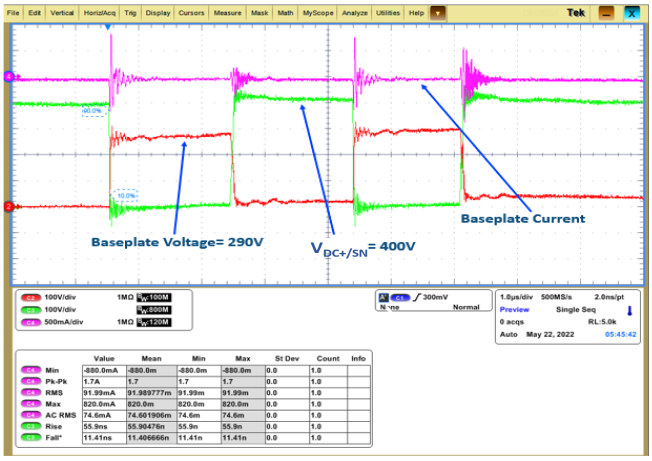
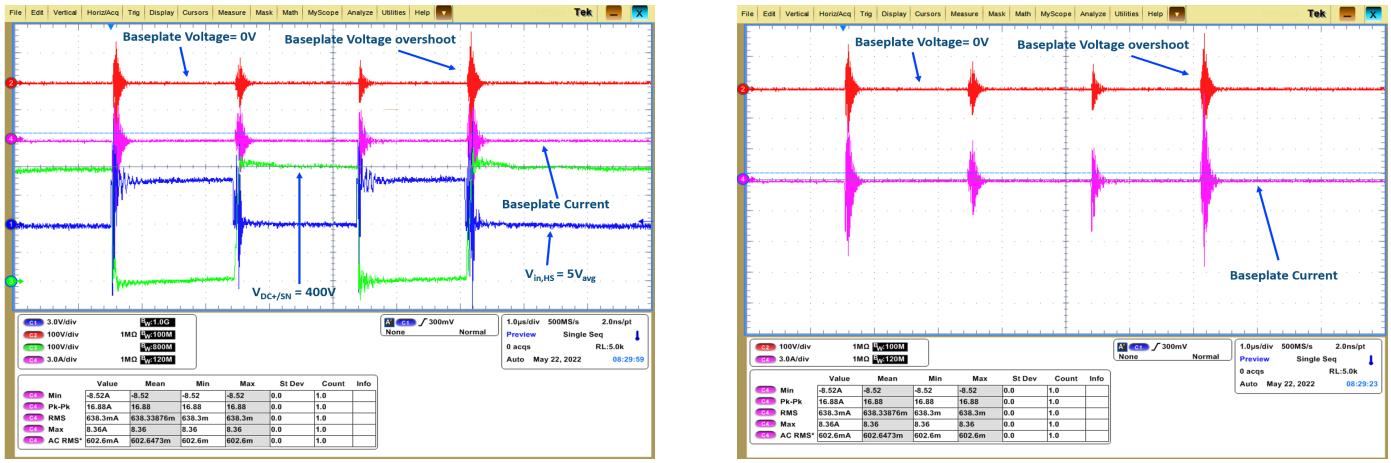


(d)

Fig. 8: (a) Baseplate floating non-optimized module (b) Non-optimized module peak to peak baseplate current (c) Baseplate floating optimized module (d) Floating Baseplate voltage

Comparing results between Figure 8(a) and Figure 8(c) shows a decrease of 0.16A in $I_{b(pk/pk)}$ in the optimized module. Importantly, this decrease is at faster voltage edge rates (green colored measurements) which means if the optimized module were to be run at slower edge rate than non-optimized module this magnitude of would be further lesser. Also, the measured ($V_{DC+/SN}$) overshoot has decreased by 22V for the optimized module. Since this decrease was not quite visible in the simulations hence the authors believe that this may be a probing issue. Figure 8(d) shows the baseplate voltage with magnitude just 100V lesser than the DC bus voltage, this may not be acceptable in many applications and hence testing with grounded baseplate was performed next.

Figure 9 shows the same trend with respect to $I_{b(pk/pk)}$ with grounded baseplates where the magnitude can be more severe without proper grounding technique. Results for the optimized module has been published as non-optimized module could not sustain DC bus voltage of more than 250V due to the high magnitude of baseplate current causing high CM current in the signal circuit. This paper will not go into the details of grounding techniques and all baseplate grounding was done through direct shorting with the power ground (DC-). Figure 9(b) shows the expounded view of the baeplate current and voltage from Figure 9(a). It can be seen that the baseplate voltage is zero at non-switching interval. However, the peak-to-peak baseplate voltage overshoot during a switching event may reach almost 50% of the DC bus voltage without proper grounding.



(a) (b)

Fig. 9: (a) Baseplate grounded optimized module (b) Peak to peak baseplate current and voltage

VI. Conclusion

In this work design, fabrication, analysis and experimental validation of two thin substrate based power modules differentiating in their layout with regards to ratio of capacitance for better electrical performance was carried out. First, Finite Element Analysis based simulation was performed as a proof of concept to show the differential decrease in the peak to peak baseplate current with a proper ratio of C_{DC+} and C_{DC-} with respect to C_{SN}. Also, for structures with low C_{SN}, it was shown that frequency domain analysis is a better method to choose the proper ratio of the capacitance as time domain analysis may not provide sufficient insight. Finally, experimental results validated the improvement in the proposed optimized module's switching performance with reduced peak to peak baseplate current at higher edge/switching rates. Importantly, there wasn't any trade off with other parameters such as voltage overshoot. This study concluded that with proper layout of thin packaging substrates and especially thin organic substrates, traditional Al_2O_3 based DBC can be replaced for high power and high switching frequency applications at a much cheaper price.

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