

Board-Level Reliability of Lead-Frame Based Substrate and Surface Finishing Technology

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Abstract

Lead-frames have been widely used in the semiconductor package assembly field, and QFN (Quad flat no leads) has the advantages of miniaturization and cost reduction of the semiconductor package. It has had limited use in automotive or defense products because of its board-level reliability. Nevertheless, due to the advantages of QFN packages, there is a trend toward using QFNs in automotive packaging. Automotive use would also require a wettable flank design of the QFN leads and automated optical inspection (AOI) of solder joints. New lead forming and surface finish technologies, including wettable flank design, are expected to improve reliability and enable AOI inspection, but much research is needed.

This study investigated the board-level reliability of various QFN lead designs and surface finishes. All lead frames with different structures and surface finish types were assembled under the same conditions and then mounted on a daisy chain printed circuit board to evaluate board-level reliability. Accelerated thermal cycling (TC) tests were performed per IPC-9701A rev 2/2006 over a temperature range of -40°C to 125°C and 6080cycles. Lastly, each package type tested was cross-sectioned, and failure analysis was performed by observing the solder joint crack for all leg samples.

Keywords

Lead-Frame, Rt-QFN, Surface finish, Solder joint, Board level reliability.

I. Introduction

With the development of lead-frame technology, the QFN package has been spotlighted as surface mounted package to overcome the disadvantages of the initial through-hole package and reduce the package size [1]-[4]. As the automotive electronics industry has developed rapidly, many attempts have been made to apply this QFN package to automotive semiconductor devices. QFN is a low-cost component type and would be desirable for Automotive and Defense applications, but reliability assessments have proven it unreliable. Also, QFN devices are difficult for AOI equipment to inspect because the height of the solder fillet is sometimes not high enough to be visible with AOI equipment. The wettable flank design has increased the height of the fillet.[5]-[8]. Despite earlier efforts, the reliability of the QFN package itself has still been recognized

as questionable, and various measures to improve the board-level reliability are still being studied [9]-[13].

To quantify any reliability improvements for the automotive market area, we must test these devices at a harsher temperature cycling condition than is typically used for computer and data products. This study aimed to investigate the effect of the design and surface finish of the lead-frame substrate on the board-level reliability in terms of improving the reliability of the QFN packages. Regarding the structure of the QFN package, the Rt-QFNTM (which is a pre-molded lead-frame of Haesung DS [14]-[16]) structure with a wettable flank shape for improving solder wetting and the general flat lead design of QFN was evaluated. In addition, in terms of the surface finish of the QFN package, Ni/Pd/AuAg plating conditions were compared with the commonly used Sn finish conditions.

II. Assembly of QFN Package

All QFN or Rt-QFN substrates were manufactured at Haesung DS' manufacturing line. Depending on the leg configuration, they were provided with a bare Cu surface or Ni/Pd/AuAg surface finish. In the case of the Sn surface, tin plating was performed during the package assembly process (right before sawing process) with bare Cu substrate. Ni/Pd/AuAg surface finish was completed through electroplating during the lead-frame manufacturing process. It was controlled to hundreds of nm for the Ni layer and tens of nm for the Pd and AuAg layers.

All legs shown in Table 1 were manufactured through die attach, wire bonding, epoxy molding, and sawing under the same conditions, except for the following cases.

In the case of leg B, immersion Sn treatment was added after package sawing to treat the Cu surface of the side exposed after package sawing.

In the case of leg D, a 2-step cut process in which sawing is divided into two steps was applied. By performing Sn plating after the first sawing and then performing the second sawing again, a QFN structure with a side wettable flank shape was fabricated.

Figure 1 shows each leg's surface finish and the shape of the bottom side of the package. Also, as shown in fig. 2, all QFN packages were made in the same 7 X 7 mm² form with 48 leads and one pad.

Leg	Substrate Design	Surface finish	No. of PKG	No. of PCB
A	QFN	Sn plating	64	4
B	QFN	Sn plating + Immersion Sn	64	4
C	QFN	Ni/Pd/AuAg (w/ roughening)	64	4
D	QFN w/ 2step cut	Sn plating	64	4
F	Rt-QFN	Sn plating	64	4
G	Rt-QFN	Ni/Pd/AuAg (w/ roughening)	64	4

Table 1. Leg configuration by QFN design and surface finish

	Leg A	Leg B	Leg C	Leg D	Leg F	Leg G
Type	QFN (Normal)	QFN (Normal)	QFN (Normal)	QFN (2-step cut)	Rt-QFN (wetttable flank)	Rt-QFN (wetttable flank)
Finish (Plating)	Electron Tin	Electron Tin + immersion Tin	u-PPF (Ni/Pd/AuAg)	Electron Tin	Electron Tin	u-PPF (Ni/Pd/AuAg)
Sub. thickness	0.200mm	0.200mm	0.200mm	0.200mm	0.185mm	0.185mm
Shape						

Fig. 1. Leg information and the form of the package bottom side.

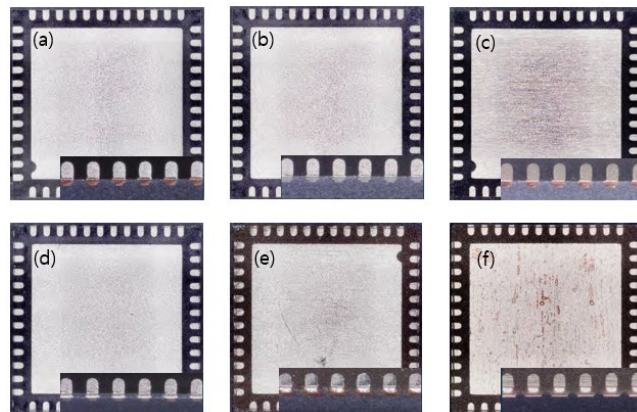


Fig. 2. Bottom side images of assembled QFN packages; (a) Leg A, (b) Leg B, (c) Leg C, (d) Leg D, (e) Leg F, (f) Leg G.

III. Board-Level Reliability Test

Each of the manufactured QFN packages was mounted on a PCB board through solder paste printing and reflow for board-level reliability testing (Fig. 3). A total of 64 packages per leg were mounted on 4 PCB boards. The height of the solder fillet was measured with Keyence VHX-6000 equipment (Fig. 4). The fillet height of all legs showed values exceeding 0.100mm, and in particular, leg B with immersion Sn treatment added to the side exhibited the highest fillet height. After that, a total of 24 boards corresponding to 6 legs were loaded into a chamber capable of controlling temperature and humidity with electrical connections completed.

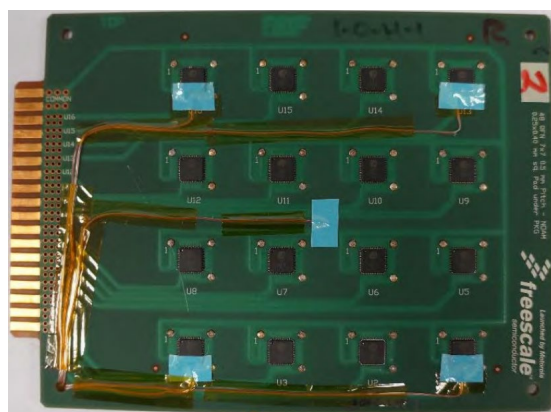


Fig. 3. PCB board image with QFN package mounted.

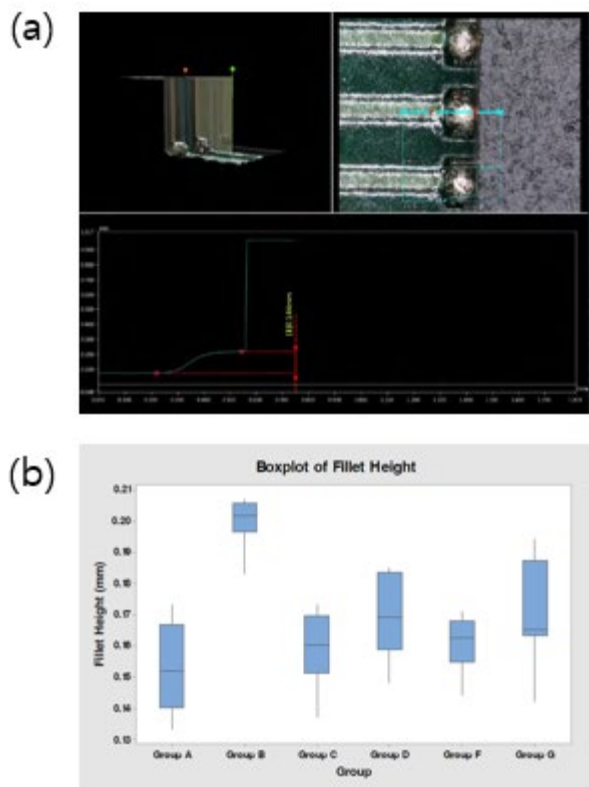


Fig. 4. (a) 3D image of the solder fillet and (b) Solder fillet height after mounting QFN package on PCB board.

Accelerated thermal cycling (ATC) testing of the varied construction legs was performed per IPC-9701A rev 2/2006 up to 6080 cycles with -40°C to 125°C cycling temperature range. I3 Electronics initially carried out the ATC test until 3750 cycles, then stopped due to the covid-19 issue, and then testing was completed until the 6080 cycle mark by UL. Testing under environment cycling involved continuous monitoring with event detection per IPC-9701. Failure was defined as the first interruption for a period of one microsecond or less and an increase in daisy chain resistance to $1000\ \Omega$ or more. Confirmation of the failure was validated by nine or more additional events within 10% of the cycles to initial failure. Additionally, resistance measurements were taken every 250 cycles at room temperature, and the failure criteria was determined to be a 10% increase in resistance. Manual resistance measurements were considered secondary confirmations of the event detections.

Figure 5 shows the Weibull plots of all test legs. Leg A and D, electroplated Tin finish with either normal QFN or 2-step cut QFN design in gray, are statistically indistinguishable during ATC testing and have been combined into a single plot with a characteristic life of 2716 cycles. The 2-step cut did not improve the fatigue life performance. Leg B immersion Tin treatment added with a normal QFN performed considerably better than the electroplated tin

finish, with a characteristic life of 3753 cycles. The addition of immersion tin improved the solder wettability, as shown in Fig. 4, and the fatigue life was slightly improved. Still, it showed unsatisfactory cycle performance of fewer than 5000 cycles. Leg F, which has the same finish as legs A and B, electroplated tin, but uses the Rt-QFN structure with a wettable flank, outperformed leg B immersion Sn with a characteristic life of 4527 cycles. This is expected due to a longer crack path caused by the round shape of the solder joint by the Rt-QFN wettable flank lead design.

Lastly, legs C and G, the normal QFN and Rt-QFN designs with Ni/Pd/AuAg surface finish, had the same highest with a characteristic life of about 7500 cycles.

Because the legs C and G dataset showed statistically different results from the other four legs, legs C and G are plotted using a 3-parameter Weibull distribution. In contrast, other legs were plotted by using a 2-parameter Weibull distribution. (Legs C and G are very poor fits to 2-parameter Weibull plots.) Despite the different lead designs, legs C and G exhibited almost identical statistical reliability data sets, from which we can see that the surface finish condition had an overwhelming effect on board-level reliability.

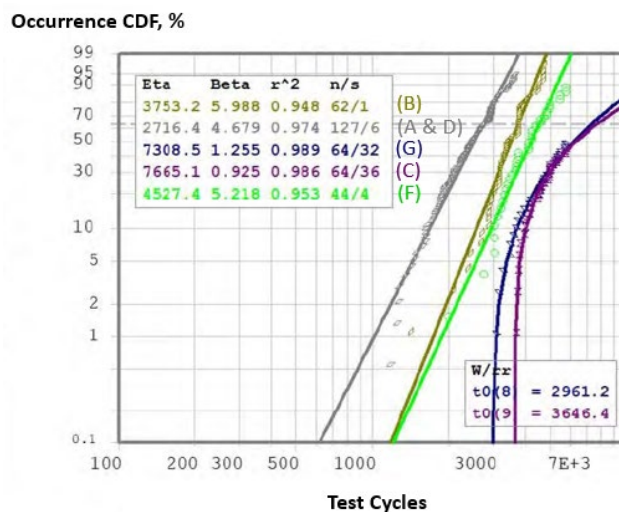


Fig. 5. ATC Test Weibull plots of QFN packages.

A cross-section analysis of the solder joint of QFN packages was performed after cycling failure to verify the ATC results. Figure 6 shows the X-section images of all legs. It can be seen that most of the cracks are concentrated at or near the lead-frame and solder interface, whereas no crack generation is between the solder and PCB board interface in all legs. In particular, compared to A, B, and D legs, which are Tin surface finish conditions, in the case of C and G legs, which are Ni/Pd/AuAg surface finish, it was seen that cracks exist mainly in a shorter form inside the solder.

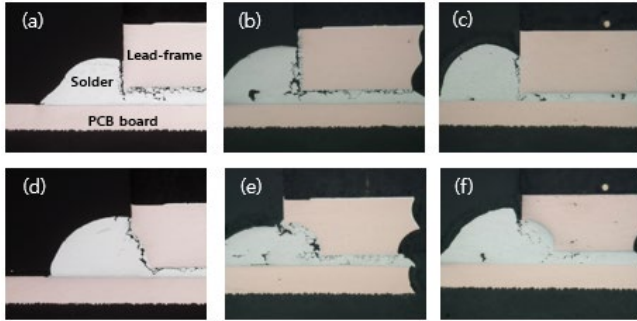


Fig. 6. X-section images of solder joint after ATC failure; (a) Leg A, (b) Leg B, (c) Leg C, (d) Leg D, (e) Leg F, (f) Leg G.

IV. Conclusion

This study investigated the effect of lead design and surface finish of the QFN lead-frame package on board-level reliability. ATC cycling tests confirmed that the Ni/Pd/AuAg surface finish exhibited the highest board-level reliability performance with a characteristic life of 7500 cycles regardless of lead design. In the case of Sn surface finish, Rt-QFN substrate with a wettable flank design showed better board-level reliability than normal QFN. Still, both showed poor performance compared to Ni/Pd/AuAg surface, showing that the surface finish significantly impacts board-level reliability.

On the other hand, as a result of the failure analysis, it was confirmed that the solder crack patterns occurring in each leg differed. For the Sn surface, many longer cracks were observed near the interface between the substrate and the solder, which lowered the board-level reliability. In the Ni/Pd/AuAg surface, solder cracks were found in a shorter form inside the solder rather than at the interface, suggesting that higher board-level reliability can be maintained.

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