Novel Micro-Textured Film Offers Promise in Universal Handling of 3D Devices

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Abstract
This paper will discuss the challenges associated with the constant evolution of IC device dimensions, and the need for carriers that can adapt quickly to the change in form factor but still maintain JEDEC standards for compatibility with existing equipment sets and pick & place tools. The paper will present a new technology inspired by gecko fibril microstructures with reversible adhesion that offers a unique approach to device handling.

Key words
Carrier, Gecko, Residue, Texture, Tray, Universal

I. Introduction
Traditional scaling is changing. Large, single monolithic devices capable of multiple functions are now being disaggregated into multiple interconnected devices. These devices, also referred to as Chiplets are the “chip of the future”, and this multi-chip assembly is rapidly becoming mainstream. This radical departure from traditional scaling methodology presents a host of challenges in chip design, design for test, manufacturing, and finally, diagnostic chip test [1].

When these Chiplets are assembled together in one assembly (either 2.5D or 3D), the yield risk is driven by the lowest yielding device. For example, costly, high-yielding memory stacks may need to be scrapped because of undetected faults on other devices in the assembly.

This trend has yielded a demand for Known Good Die (KGD) – a bare die that has been fully tested prior to packaging. This is introducing an additional step for die level testing vs. the conventional Wafer Probe Testing (WPT).

Wafer Probe Testing (WPT) has been the norm because die registrations are at precise locations. However, it's not a full and accurate test because the presence of the surrounding die reduces testing accuracy and mitigates against running certain tests, such as high current tests. Although drain and gate leakage tests (such as IDSS and IGSS) may be performed at WPT, the measured leakage values will change after singulation [2], and not to forget the defects such as side wall crack can bring additional changes. WPT is also limited for testing Through-Silicon Via (TSV), which requires probing from both sides of the die and wafer probing cannot be done from both sides because the VIA’s are not exposed.

To truly assure a KGD, the ability to access yield at each intermediate fabrication step - thinning, bond & assembly, packaging - is critical. This is driving the need for more Singulated Die Testing (SDT). SDT is more precise over WPT and can closely represent the end use performance of the die. Also, since the entire wafer need not be handled during testing, dies can be rejected/accepted individually.

SDT requires open & random access to dies during processing so they can pick & re-pick for multiple tests [3,4]. Current options (Fig 1) to present dies for SDT can be JEDEC trays, Tape & Reel or Sticky tapes, aka Dicing Tape. While the JEDEC trays are omnipresent in the final assembly environment and are exclusively used for test and handling of packaged devices, they are not so popular for handling bare die. These are molded trays that are designed for a specific device. If the device changes a new tray has to be designed to accommodate that device. Tape & Reel are used for both packaged as well as bare die handling. However, they don't offer an easy pick & re-pick required for SDT.
Sticky tapes are also used for bare die handling; however, a device can only be picked once and can never be put back for it to be used again.

Consequently, none of the current handling options are very user friendly for SDT. There's a need to have a new handling method that offers the flexibility for pick & re-picking multiple times, and that can accommodate a high mix of device sizes, as each device/chiplet type will have a different size. Also, these devices are typically thinned in order to keep a certain final component (2.5D or 3D) thickness. Thinner means they are more vulnerable during handling and transport, so the new handling method should also offer good protection.

II. Development

Keeping the above requirements in mind, Gel-Pak worked on developing a carrier with the specific target to support SDT for KGD use. To stay compatible with the existing handling equipment and PnP tools, we decided to stay with the JEDEC tray format. JEDEC trays hold devices based on custom designed pockets, which limits their use for only that device size. Instead of restricting the device movement based on a custom designed pocket, Gel-Pak worked on holding the device using tack. This no longer limits the tray to a specific device size. The tack needs to be engineered such that devices can be picked and re-picked multiple times. This required the development of a reversible adhesion, which goes against the word adhesion.

The true example of reversible adhesion is “gecko-like” grip, which can hold the device but will release it with minimum resistance in a PnP process. This led Gel-Pak to investigate bio-based adhesion and to try and understand how their gripping action works. A substantial body of work has been published in this field studying how geckos, lizards, beetles, spiders, and ants can attach themselves to different surfaces but also detach themselves very easily without disturbing the surface. The research has uncovered that it has to do with micro-texturing of their toe pads. This texture consists of fibrillar that can conform to surface irregularities, and the adhesion comes from the viscoelastic response of their outer membrane. Fig 2 shows toe pads of different species which help them move seamlessly across different surfaces.

Each species has a unique texture that helps it move, correlating across species relative to their body weight. Different industries have tried to learn and implement such micro-texturing to help solve issues ranging from optics, fog resistance, pressure sensing, tissue engineering, and microfluidics. In the field of Pressure Sensitive Adhesives (PSA), such micro-texturing has led to the development of dry adhesives, opening a new type of adhesive which offers strong bonding but easy and clean release.

Gel-Pak tried to utilize the same textured adhesive concept in developing the JEDEC carrier tray technology. We researched how others did materials and texture development. We identified a few different published research [5,6] in line with what we wanted to accomplish. The first [5] research studied 6 distinct texture patterns using a PDMS elastomer to show how the texture influenced holding force. The second [6] research demonstrated similar work, but with square textures instead of dimples. Keeping these published works into consideration and knowing the IC handling requirements, Gel-Pak decided to utilize textures that are compatible with High Volume Manufacturing (HVM), which means utilizing conventional plastics fabrication processes, such as injection molding and extrusion to fabricate, and using materials that are best suited for such process. We focused on materials engineering as well as texture engineering. Various geometric patterns were investigated. We tried 4 different pillar textures as shown in Fig 3, and over 20 different adhesive formulations and put them through various IC handling testing. Each texture/adhesive option was screened based on the following- surviving shock/vibration/drop at -10C, 20C and 50C; long-term tack growth, IC backside residue, PnP and SMT pick ability, and few other criteria.
After all the testing, we finalized our efforts on texture (a). Fig 4 is an SEM image of our adhesive molded using the texture (a). Between the viscoelastic response and the textures, we were able to generate a wide range of preload force curves (Fig 5) by leveraging different adhesive chemistries to envelop a wider preload force spectrum.

To our knowledge there was no precedence to what we were trying to accomplish with our technology development. In plastics fabrication processes, texturization is primarily used for ergonomic considerations whereas we were trying to use it to engineer tack. Injection molding of textured adhesives was also not practiced in the industry. In addition, the ASTM and other test standards don't have any tack metrology for textured surfaces.

We tried 6 different textures and over 2 dozen different adhesive formulations and put them through various IC handling testing. Each texture/adhesive option was screened based on the following: surviving shock/vibration/drop at -10C, 20C and 50C; long-term tack growth, IC backside residue, PnP and SMT pick ability, and few other criteria. After all the testing, we finalized a texture and 3 different adhesive formulations - Low, Medium & High tack. The Low tack is designed for in-process device handling only, Medium tack can be used for in-process but subsequently the bare dies can also be shipped on this carrier. High tack is specifically designed for packaged devices like QFNs (Quad Flat No-lead).

The final products were tested on a few different PnP (Royce, Besi, Muhlbauer, MRSI) and SMT (Juki) machines to validate pick ability. PnP parameters including Down force at device contact, time to draw full Vacuum, Tip & Collet size w.r.t device size and Pick speed were investigated.

With few modifications to the above-mentioned parameters all PnP equipment’s were able to successfully pick the IC devices from the trays at medium UPH rates. The key aspects were limiting down force to seal the vacuum cup with the device surface, pull vacuum to an optimum threshold and then initiate the pick.

**III. Conclusion**

Inspired by bio-based micro-structures, Gel-Pak has developed an IC tray technology that can be a universal handling solution best suited for SDT for KGD. The technology required fine-tuning adhesive technology and micro-texturing its surface to offer the tack that is just enough to hold the device but also easy to pick at high-speed
PnP processes. The technology has been successfully scaled for a few different form factors, ranging from 2-inch chip trays to as large as 300mm wafers.

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References


