Unimicron

Innovated L/S ≤ 2/2μm Line Embedded 2.1D Organic Substrate Technology

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NBD, Unimicron Technology Corp.

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Unimicron

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Unimicron Technology Corp.

- Established : 1990
- Chairman & CEO : T.J. Tseng
- Capital : US $523M

- Employees : ~12,000 (Taiwan)
  ~14,000 (China)

SiP & Market

➢ What is SiP

- A **System in Package** (**SiP**) or **System-in-a-Package** is a number of **integrated circuits** enclosed in a single module (**package**).

Source: https://en.wikipedia.org/wiki/System_in_package

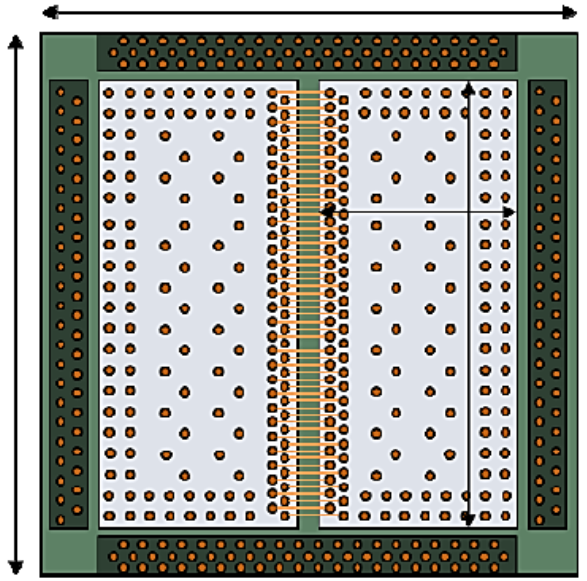
➢ Market of SiP

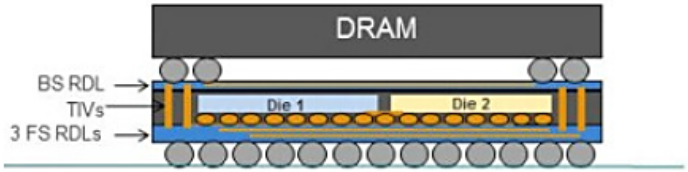
- According to a new market research report "**System in Package (SiP) Market by Technology (2D, 2.5D & 3D), Type (BGA, SMT, QFP, SOP), Interconnection Technology (Flip-Chip & Wire-bond), Applications (Communications, Consumer, Automotive, Medical) and Geography (N. America, Europe, APAC & ROW) - Global Trends & Forecasts to - 2014 - 2020**", published by MarketsandMarkets.
- The **total System in Package (SiP) market is expected to reach $18.10 Billion by 2020**, growing at a CAGR of 9.57% from 2013 to 2020.

Source: http://www.marketsandmarkets.com/PressReleases/system-package.asp

Target Spec for Split Die SiP

- Split Die Requirement : 2u L/S between die
  - Requires to support ~ 2000 D2D connections
- PoP Memory Requirement : PoP via + RDL
  - Required to leverage standard PoP package
- Si Form Factor : two ~12 mm x ~6 mm die
  - Assuming compliance with fab AR requirements
- Electrical Requirement : 3LM Interconnect
  - Required for signal, PoP and PDN/SI needs
- Package = 15mm x 15mm x <1mm
  - Required to meet the usual SP constraints
- Cost Requirement < 1c/mm2
  - In HVM
- Candidate Technologies
  - Low Cost Si Interposer (no substrate)
  - Fan Out Wafer Level Package
  - Photosensitive Organic Interposer





11/7/2014

QUALCOMM

Source: GIT2014 “2.5D and 3D Integration” Rick Radojcic / Qualcomm

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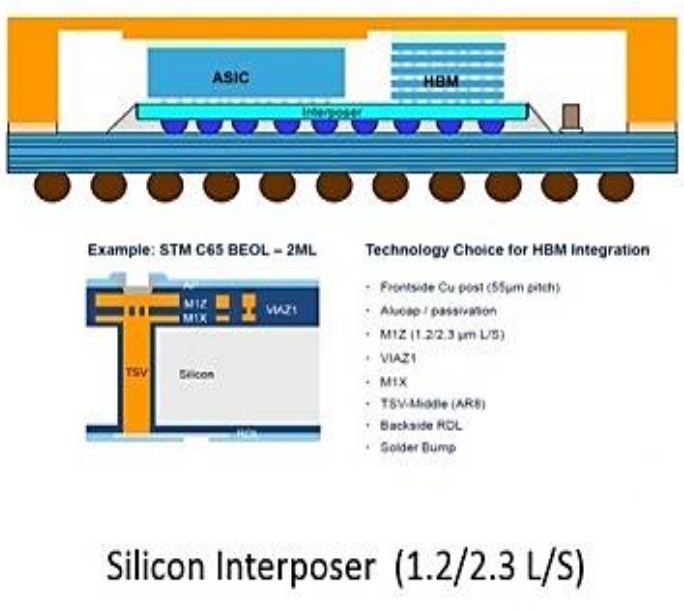
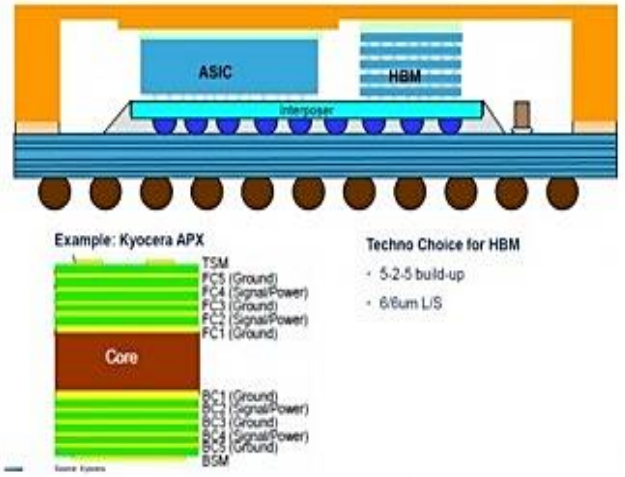
Interposers for Networking ASICS

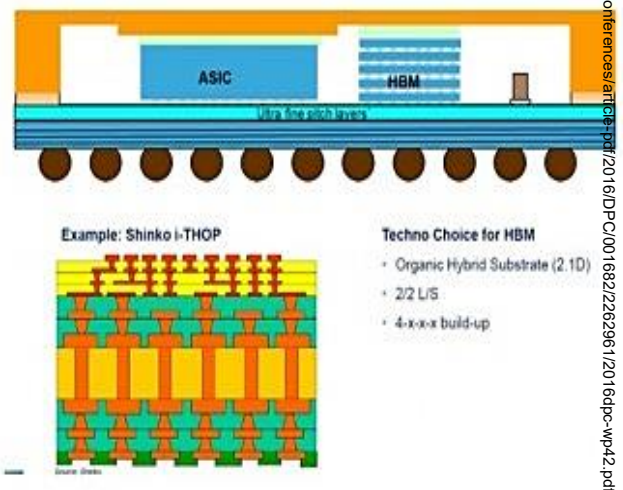
- **Higher I/O density and memory bandwidth**, required for future Networking ASIC chips, can be handled by use of **2.5D packaging** with high density interposers.
- **2.1D organic substrate solutions** are the most promising in terms of cost and supply chain simplicity.



Silicon Interposer (1.2/2.3 L/S)



Laminate Interposer (6/6 L/S)



Laminate Interposer (2/2 L/S)

Source: Georg Kimmich of ST Micro gave a presentation on Network packaging trends

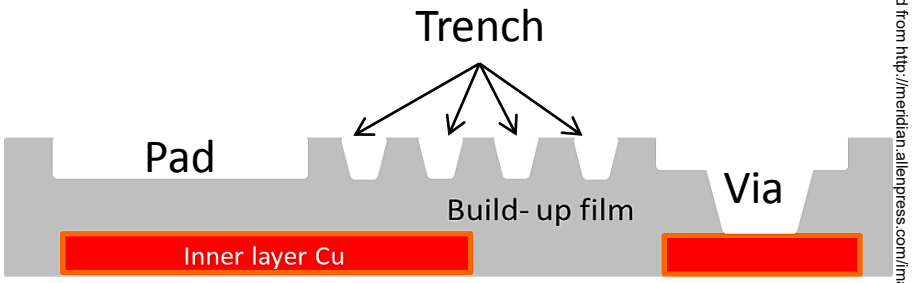
SiP Packaging Challenges

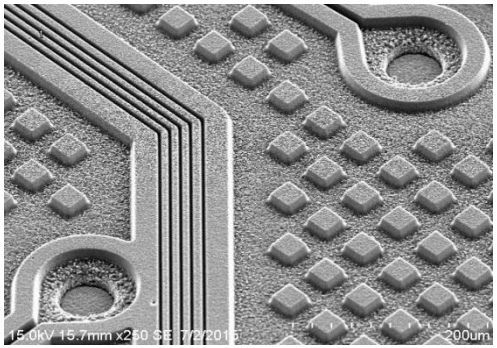
- Require **fine line and small pad size** for higher chip integration.
- Thinner package require thinner chip (need to handle <100µm wafer)
- More functionalities will create more power consumption.
- Advanced **materials & equipments cost** are higher.

Line Embedded (LE) Technology

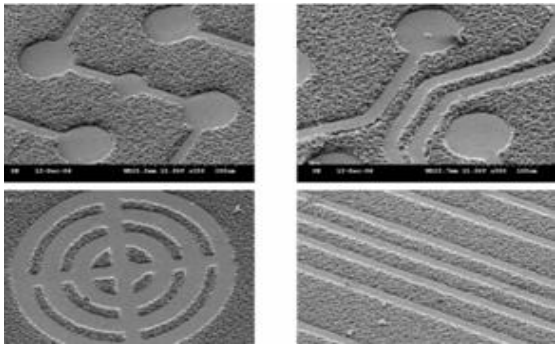
➢ LE

- Laser or photo patterning of dielectric
- Embedded circuits
- Capable of stereo copper features
- Covers FC, CSP, Coreless structures





Ablated Dielectric Pattern



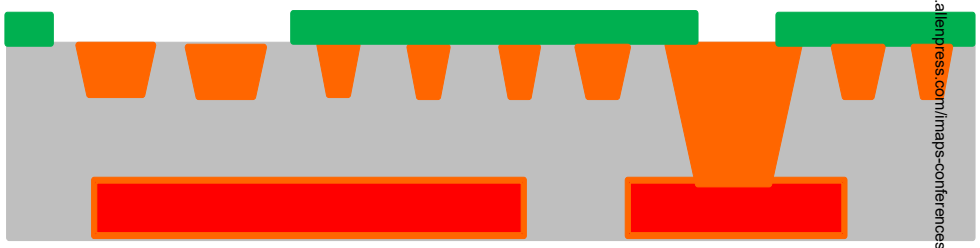
Post Cu Plated

➢ Benefit

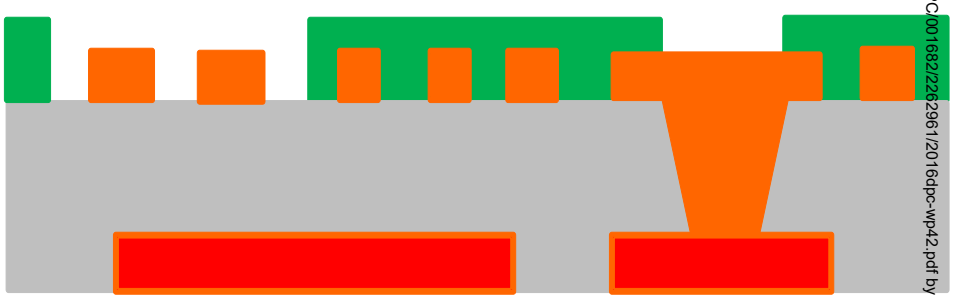
- Better electric performance with lower variation of trench width/depth.
- L/S ≤ 5/5μm fine pitch trench can be formed.
- Better design flexibility & reliability than SAP process.

Structure Comparison

- **Flat surface after formation of pattern**: helpful for covering a thinner solder mask with better uniformity of thickness.
- **Allows the design of pad-less via:** reduce both package size and format, and also can put more traces near these vias.
- **Low Z-profile**: thinner substrate.
- **Good adhesion between dielectric and copper line:** better reliability.

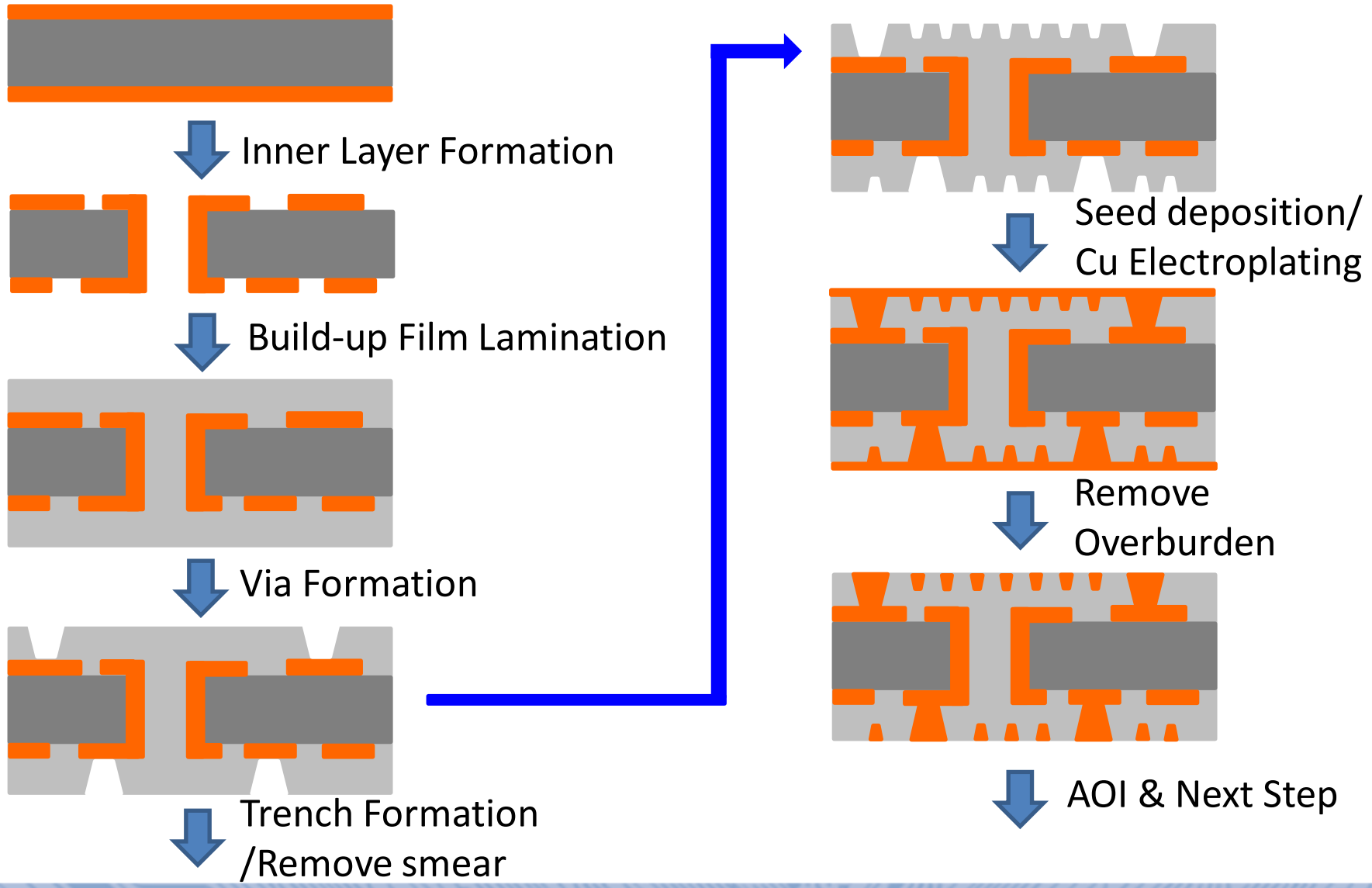


Structure of Line form by Laser Direct Ablation



Structure of Line form by SAP

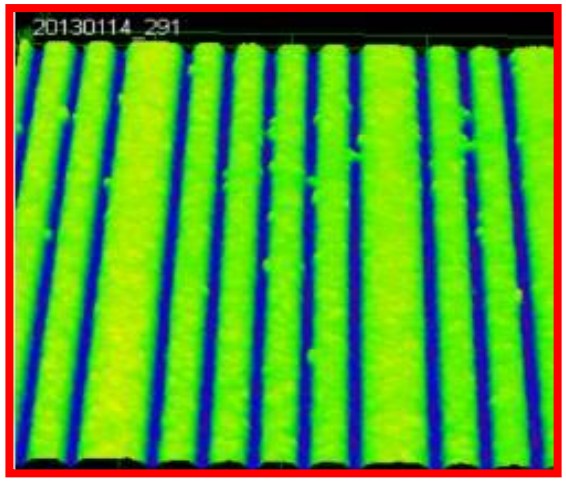
Process Flow of Line Embedded Substrate

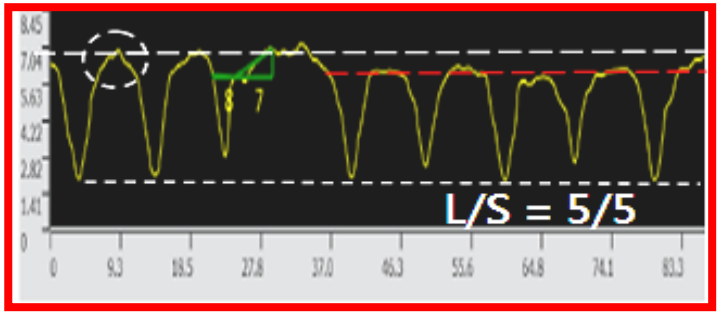


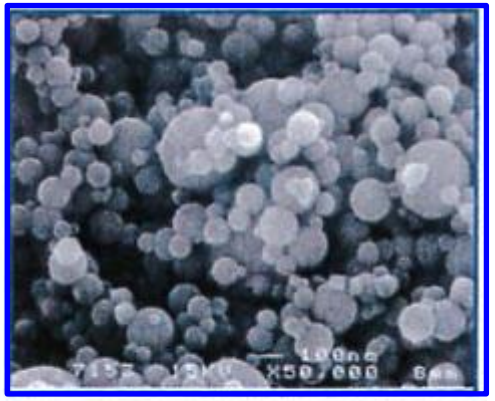
L/S≤5/5μm Development

- **Material is the key to achieve fine line:**
  - **Small filler size Material B get better laser ablation result than Material A.**

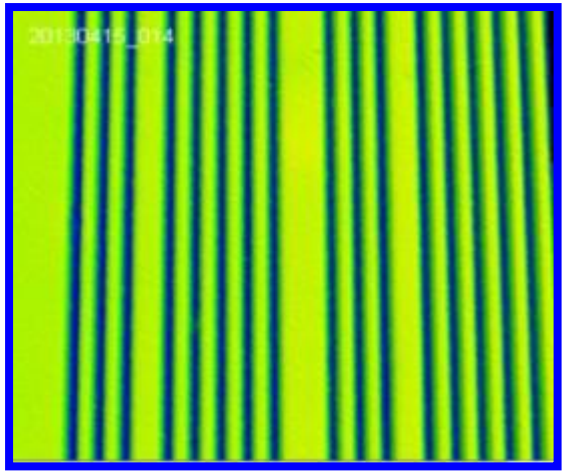
Material A (max.2μm)



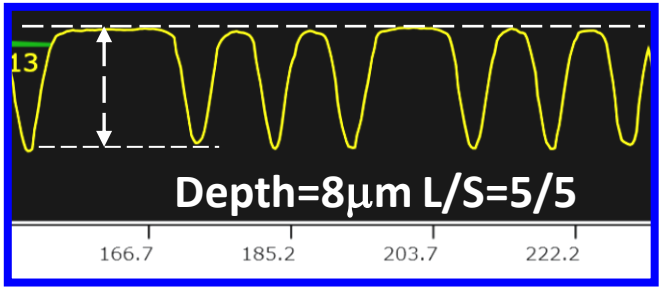




Material B (max.0.5μm)



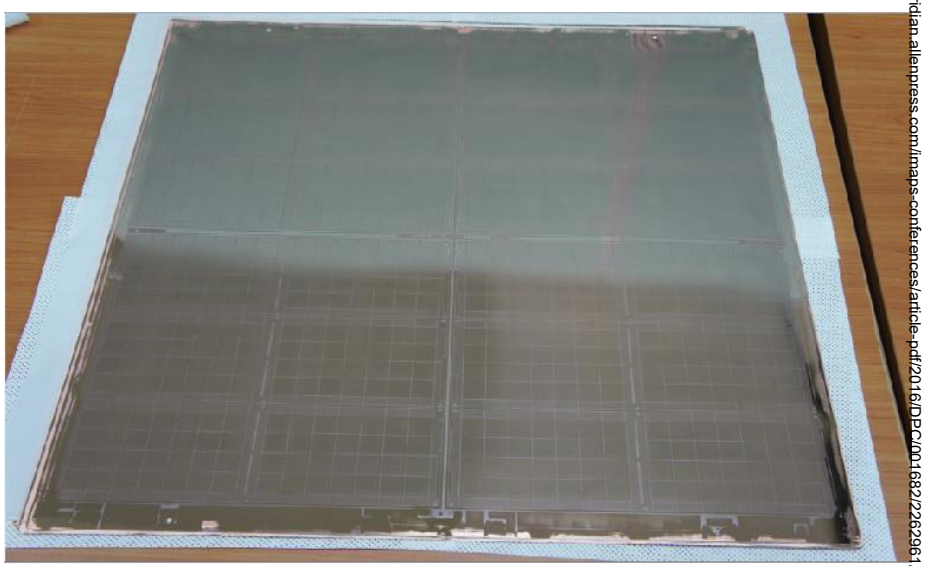
LDA Results



Cu Overburden Remove

- **Low cost and uniform Cu reduction is the key process for removing the copper above the dielectric surface for forming circuit pattern**

Before Cu Overburden Remove



After Cu Overburden Remove

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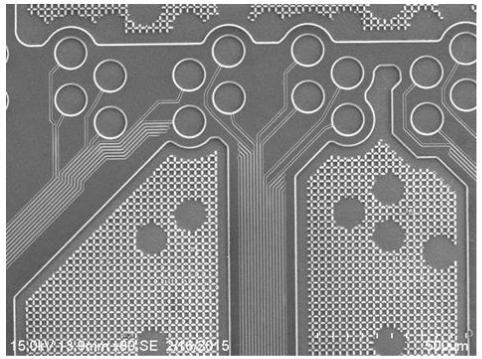
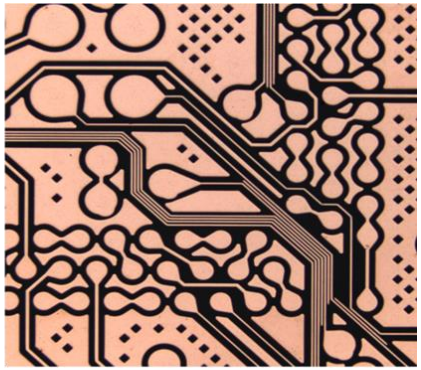
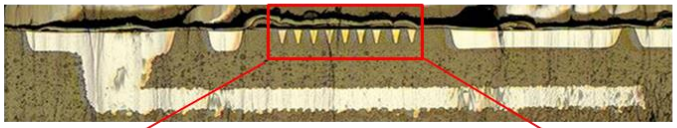
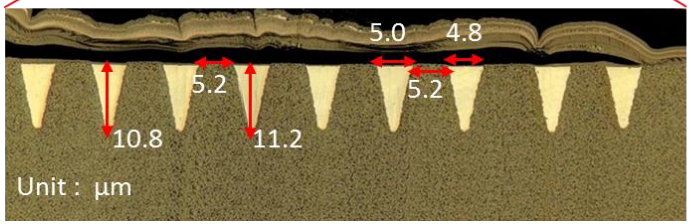
LDA LE for 5/5 & 3/3μm L/S

- Line embedded circuit patterns and SEM of L/S=5/5 & 3/3μm.
- BF material with filler is difficult to get good profile by LDA.

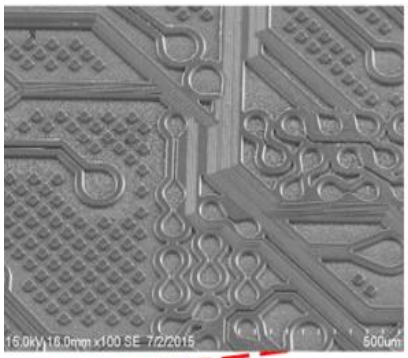








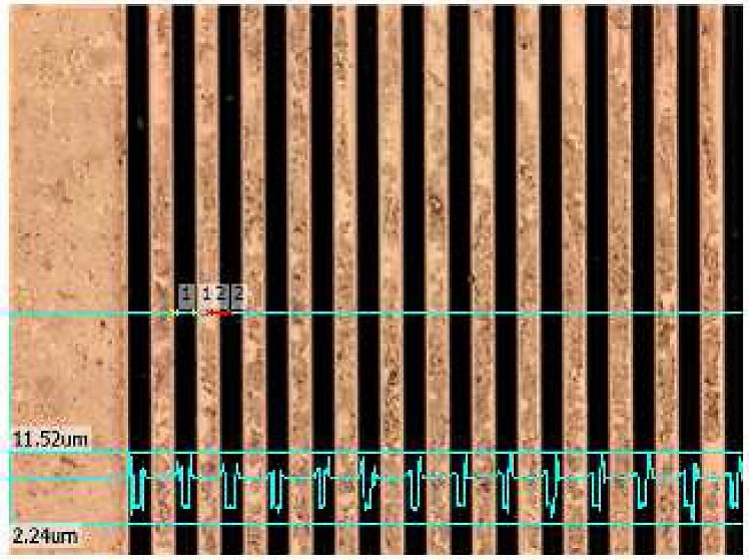
L/S=5/5μm



L/S=3/3μm

L/S≤3/3μm & Trench Geometry

- LDA result of non-filler dielectric material



L/S=3.7/2.5μm, Depth=6.8μm

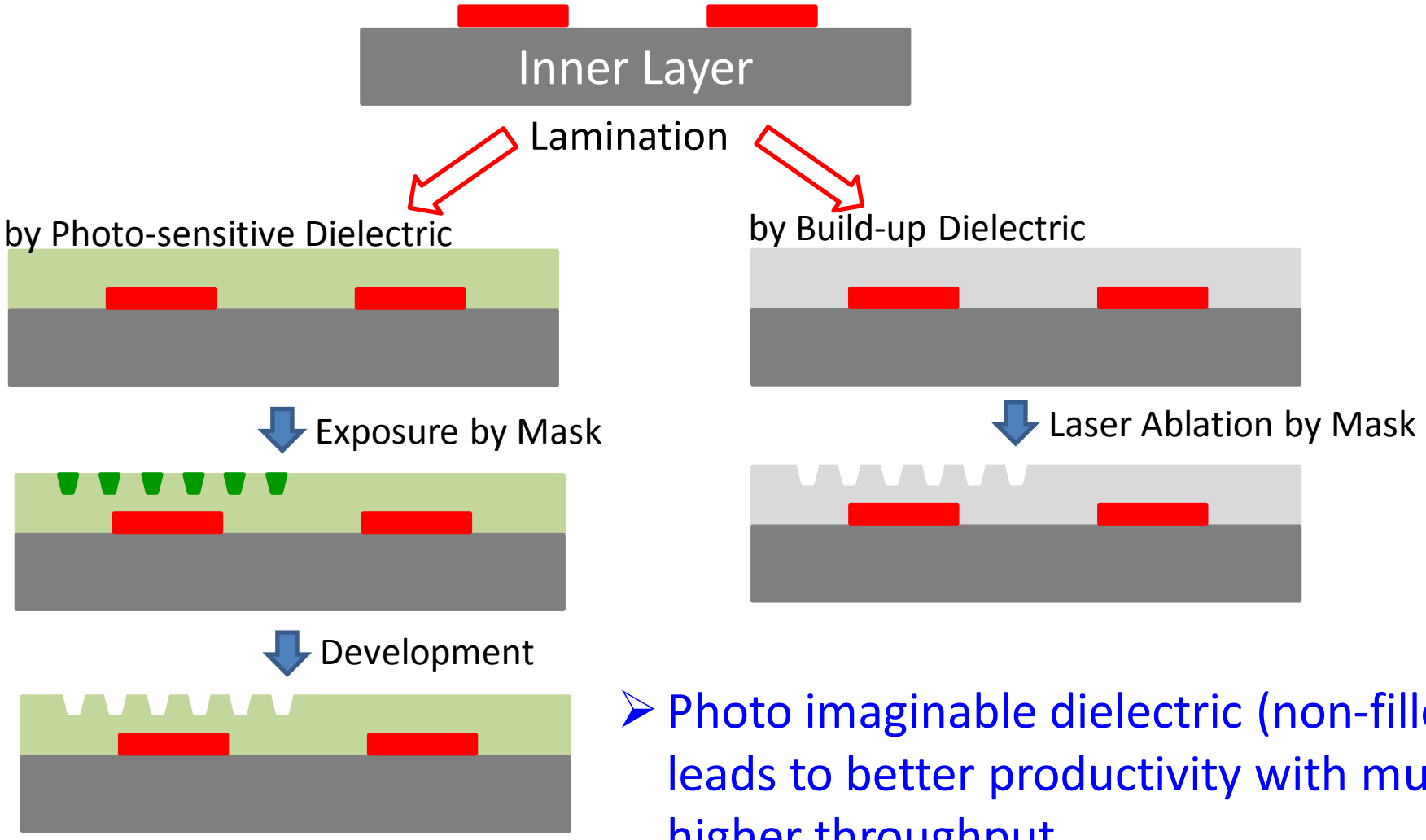
- Target of trench geometry

Now **Future**

Challenges of LDA LE

- **Small filler size material**
  - Material cost is high.
  - Non-filler type or PID material could be the alternative.
- **Tight Cu thickness spec.**
  - Introduce novel & cost effective Cu reduction process to reduce the thickness variation.
- **High cost of laser trench**
  - To improve trench shape.
  - To evaluate the cost effective laser system.
  - Photo lithography is the other alternative.

Alternative Method of Pattern Transfer



- Photo imaginable dielectric (non-filler) leads to better productivity with much higher throughput

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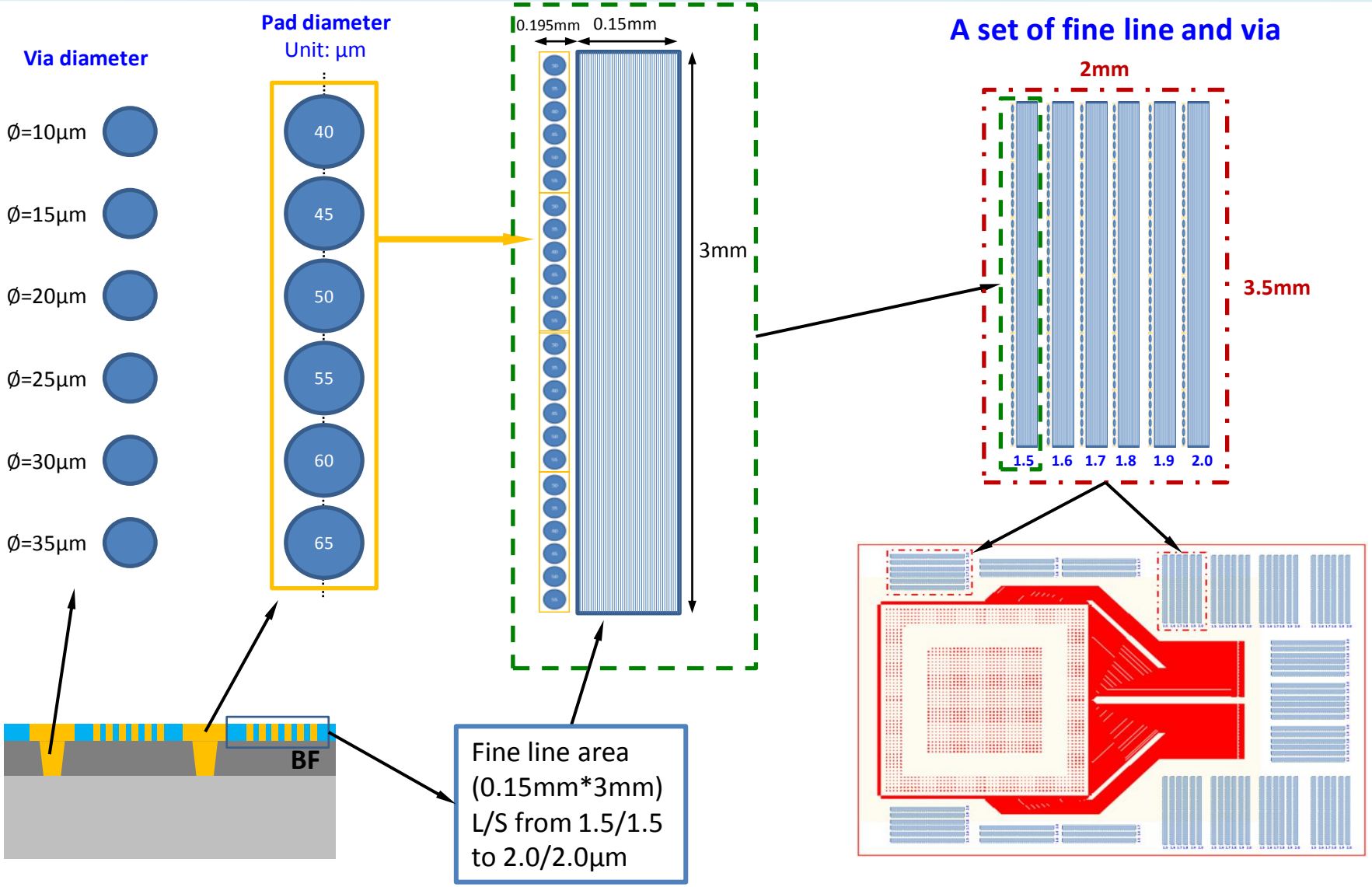
Pattern Design of Fine Line and Stacked Via



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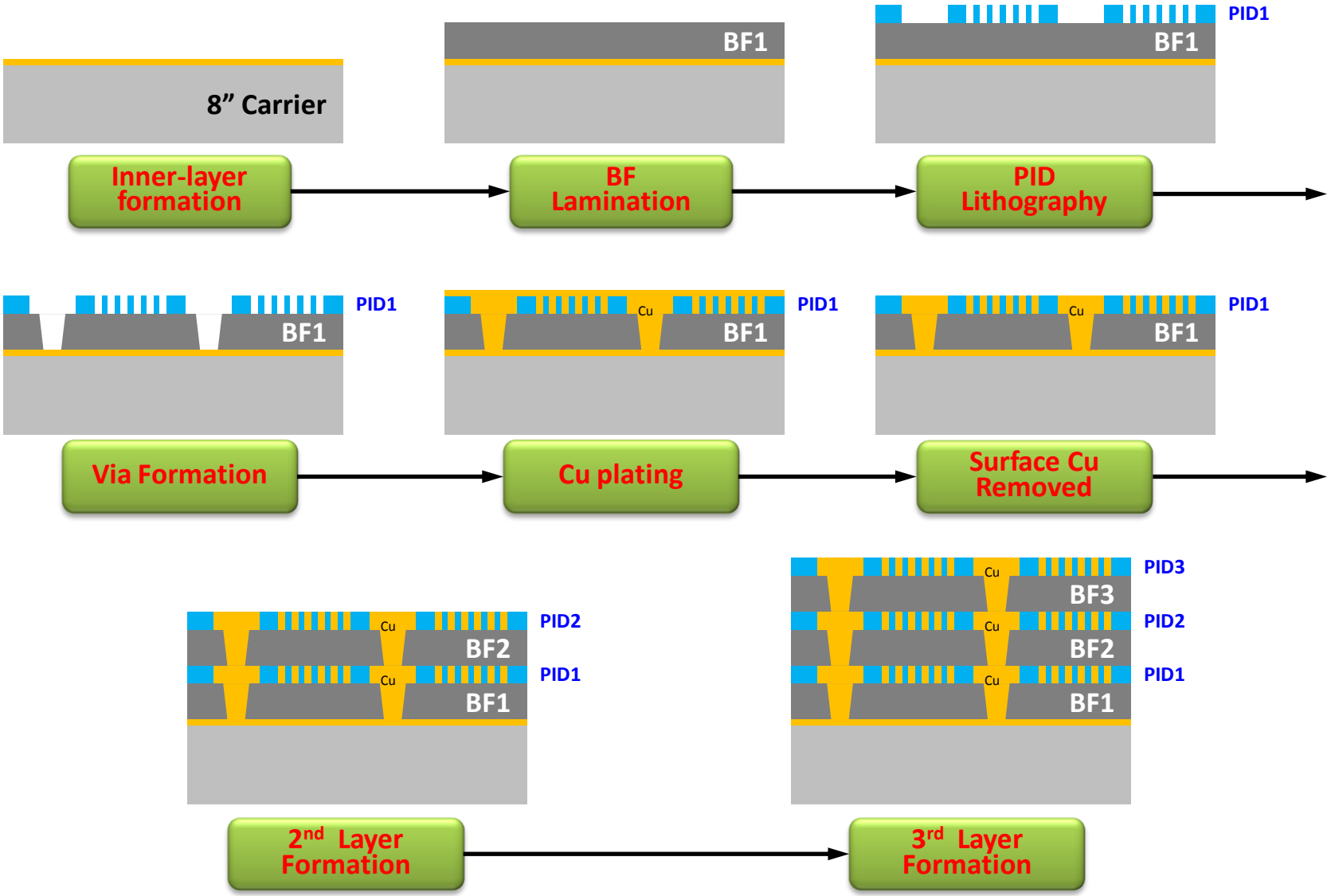
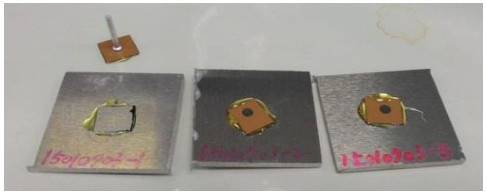
Process Flow for PID LE

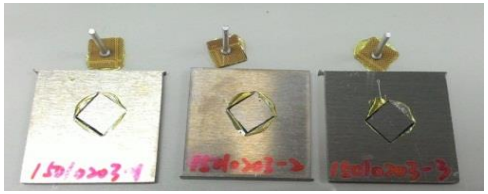


Adhesion Test

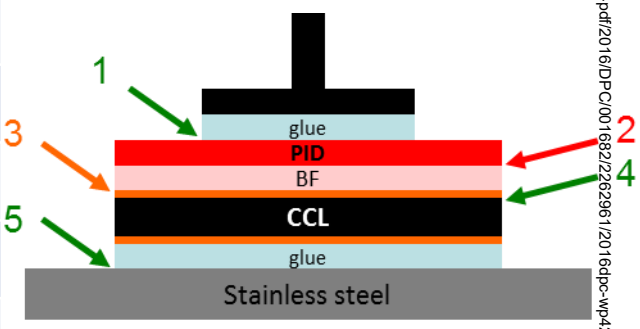
➢ Peeling test of PID on different BF

- **Peeling strength ≧21MPa.**





BF	Sample No	#	Peeling Strength (MPa)	Failure Mode
A	15010703	1	34.07	5
		2	23.63	4
		3	21.32	4
B	15010203	1	48.53	5
		2	50.79	5
		3	52.52	5
C	15011101	1	40.61	5
		2	69.24	5
		3	71.85	5



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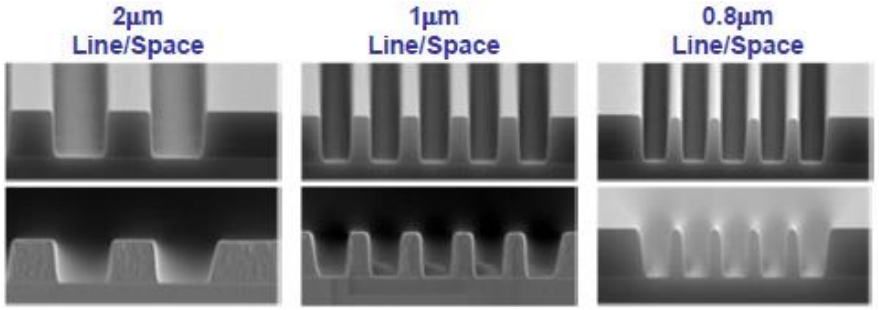
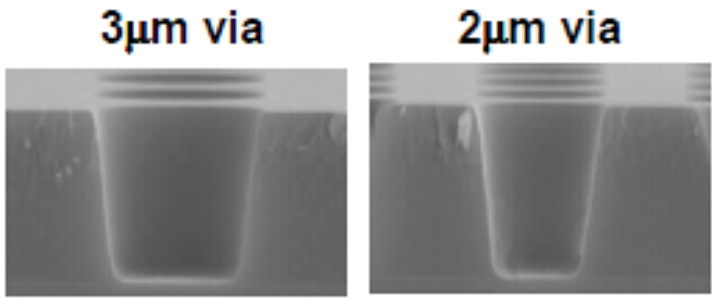
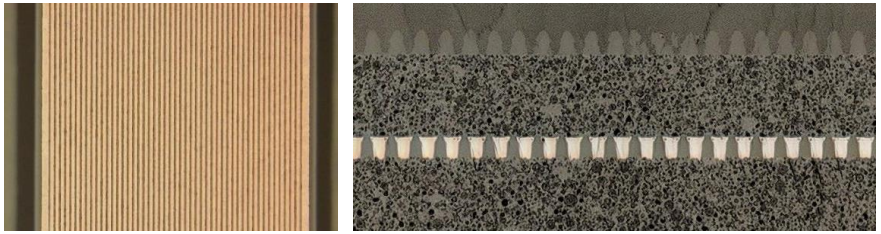
Fine Line & Small Via

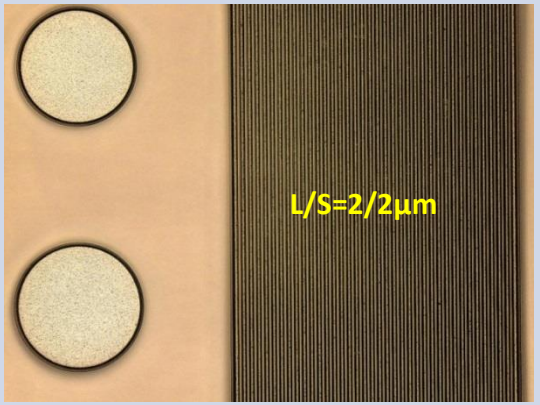
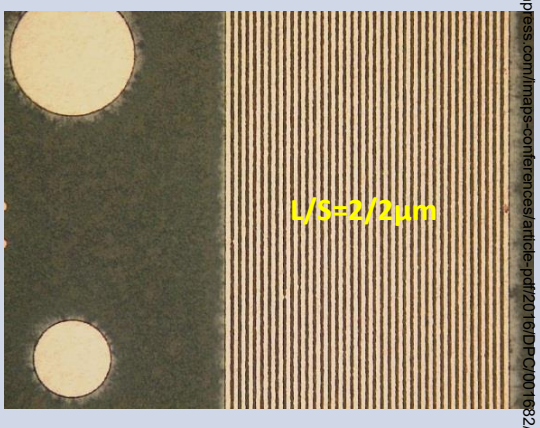
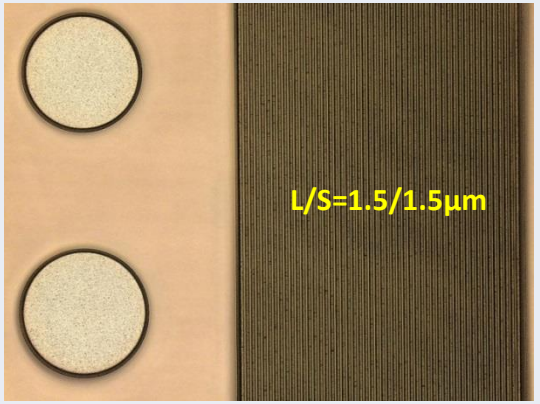
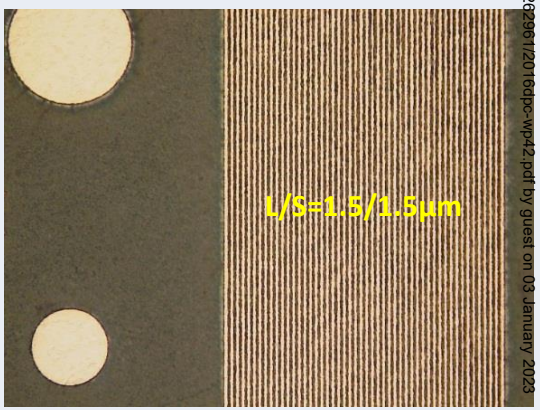
➢ PID can achieve very small via and trench.





L/S=1.5/1.5μm

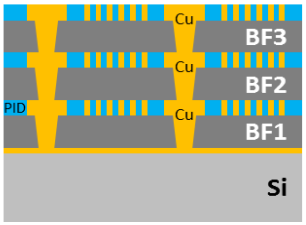


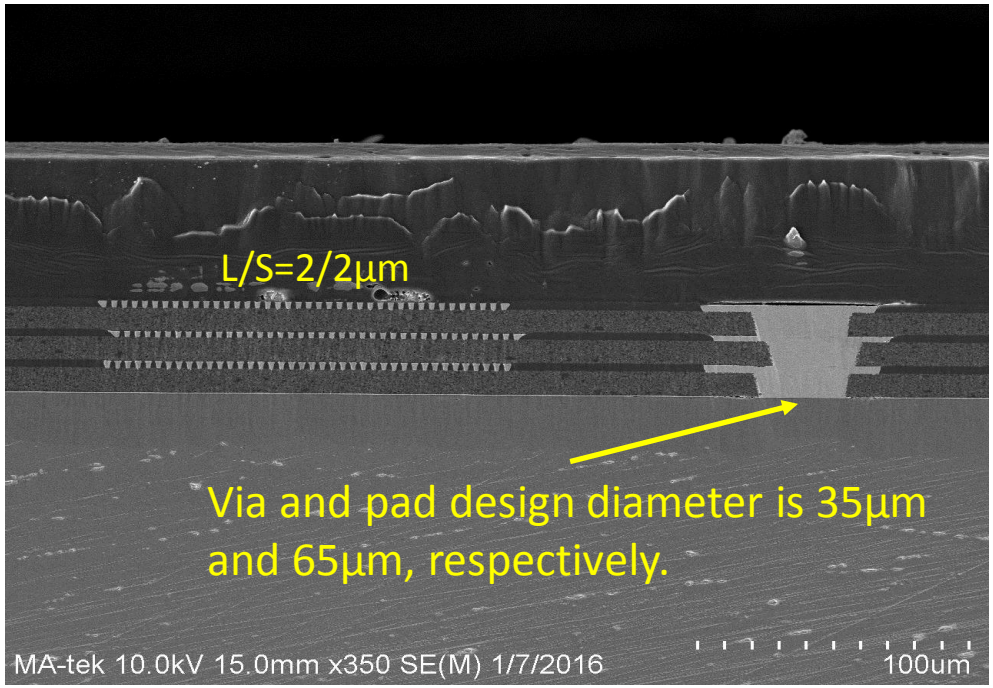
After Lithography	Via and Trench Filled
	
	

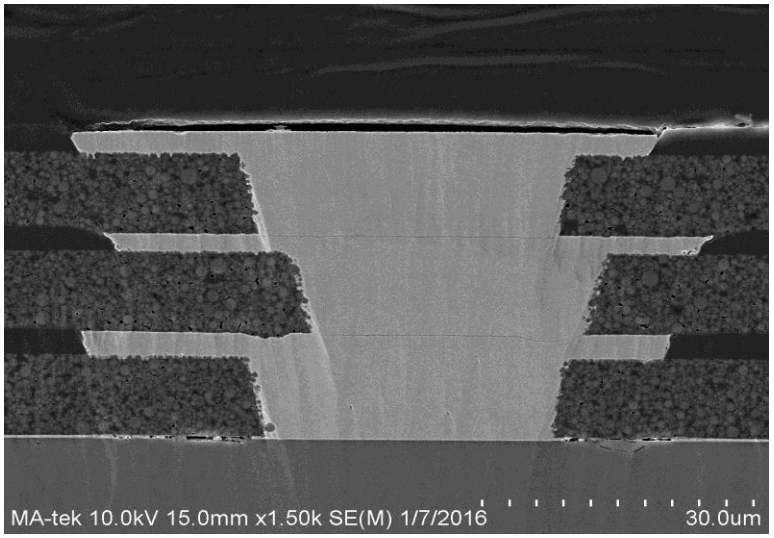
PID LE Results

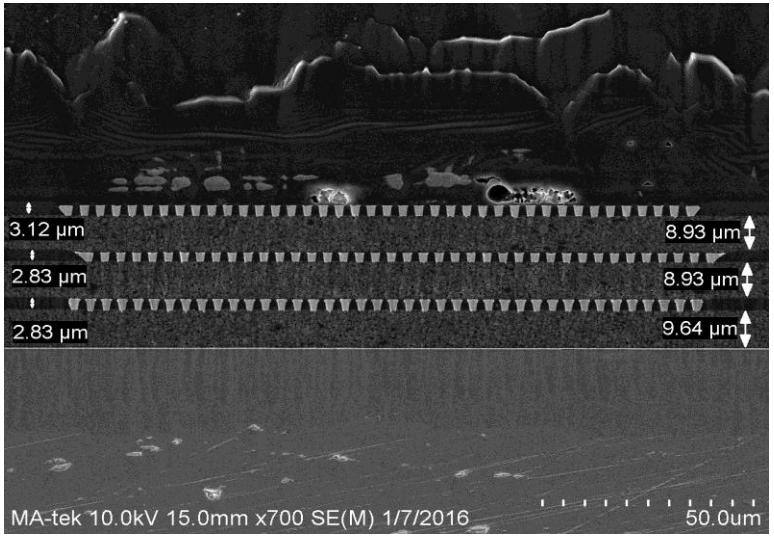
- Multilayers fine line could be achieved.
- Good Cu thickness uniformity.

Thickness (μm)	BF1	BF2	BF3
ABF	9.64	8.93	8.93
PID	2.83	2.83	3.12









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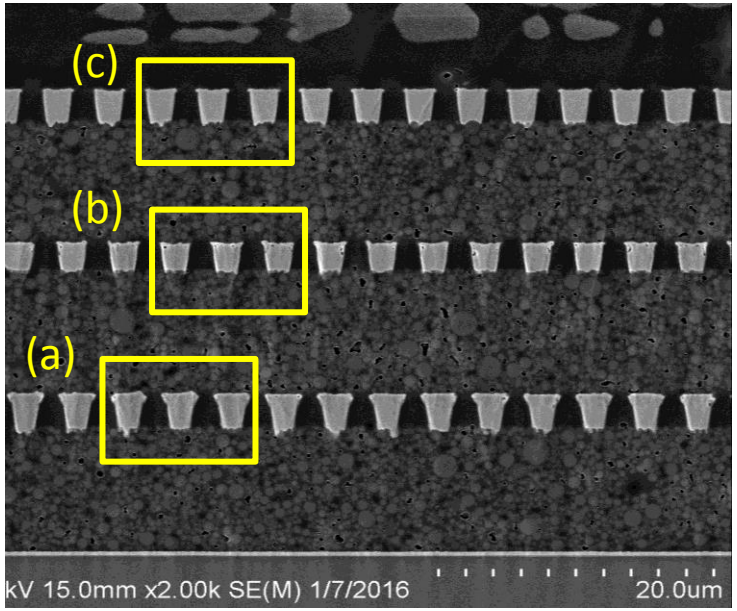
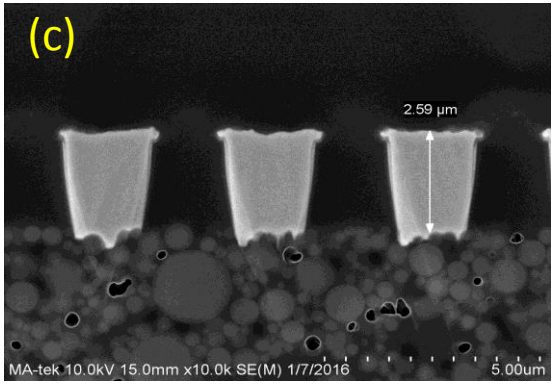
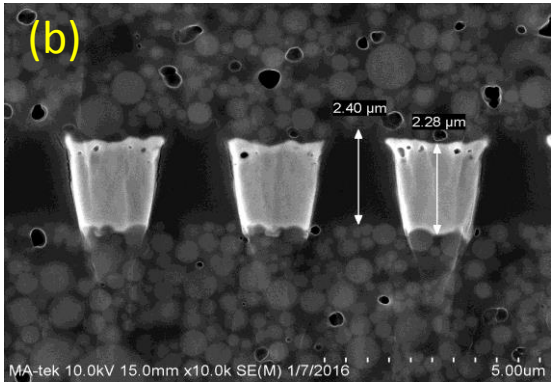
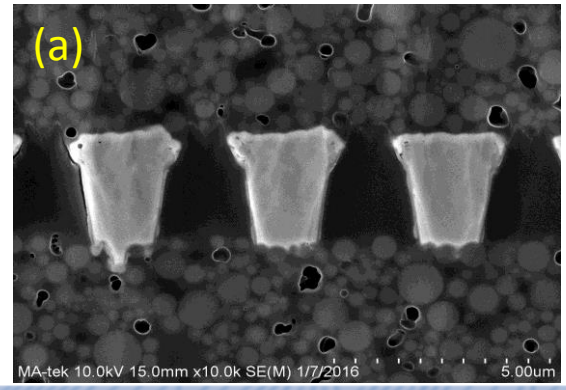
Trench (L/S=2/2μm)

Dimension (μm)		a	b	c
Line/Space	Top	2.45/1.48	2.23/1.48	2.46/1.37
	Bot.	1.50/2.30	1.59/2.18	1.68/2.10



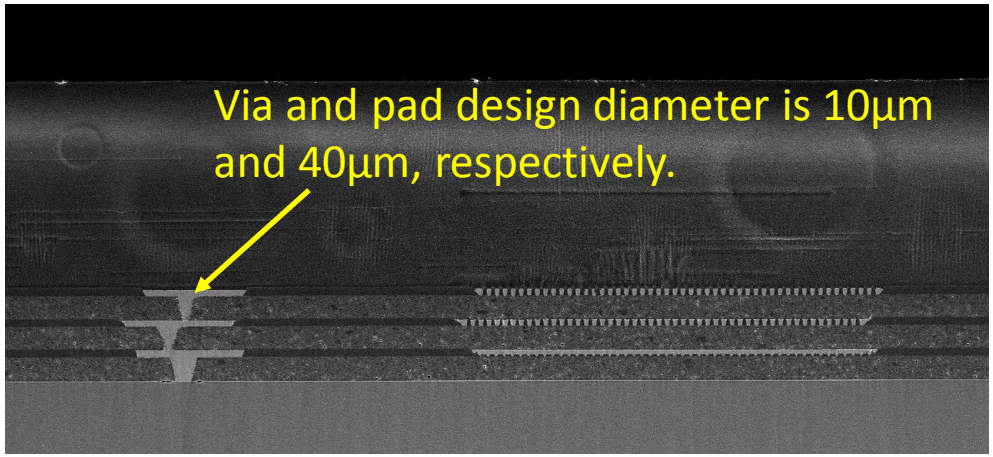


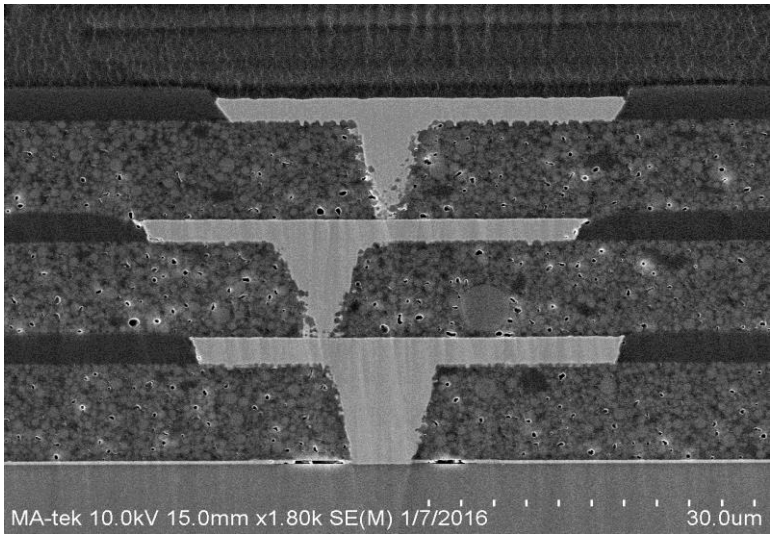


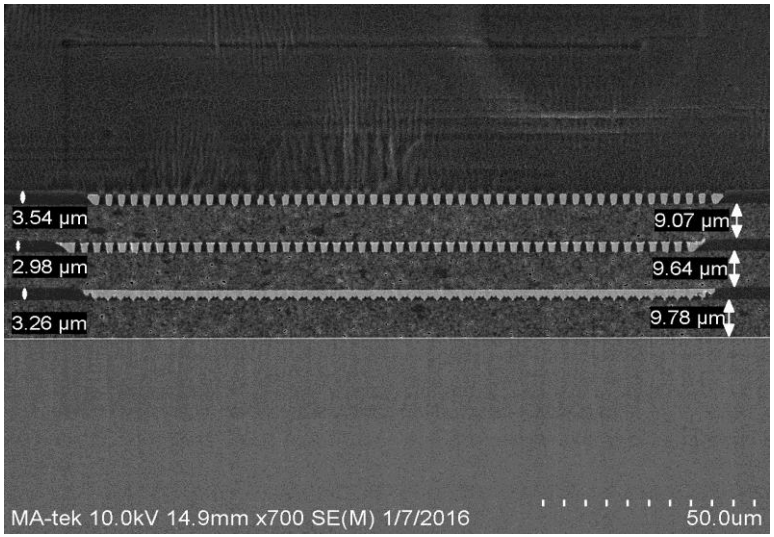


PID LE SEM of L/S=1.5/1.5µm

Thickness (µm)	BF1	BF2	BF3
BF	9.78	9.64	9.07
PID	3.26	2.98	3.54

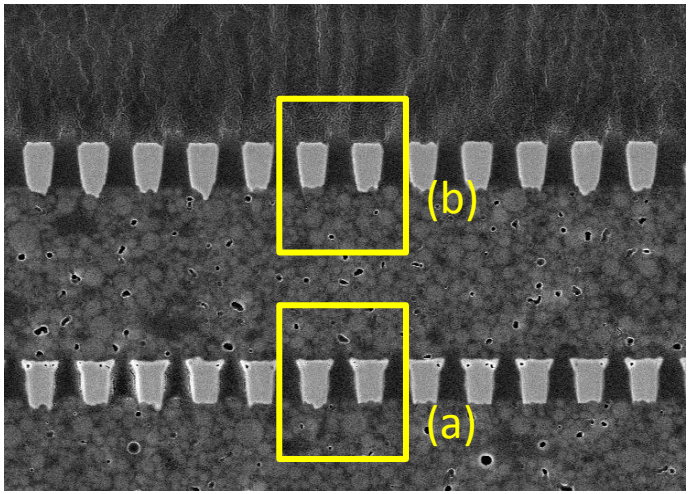


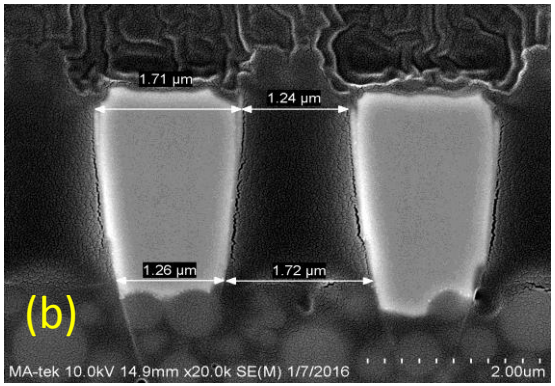


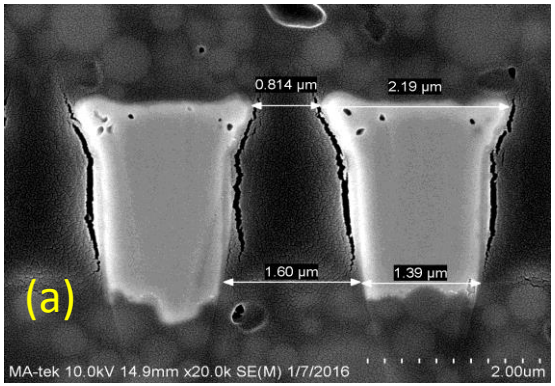


Trench (L/S 1.5/1.5μm)

Dimension (μm)		a	b
Line/Space	Top	2.19/0.81	1.71/1.24
	Bot.	1.39/1.60	1.26/1.72







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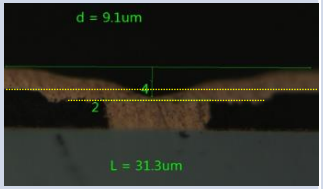
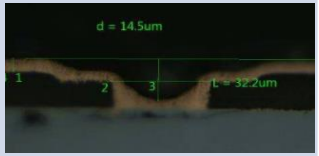
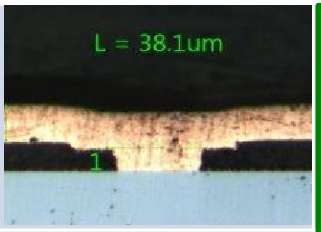
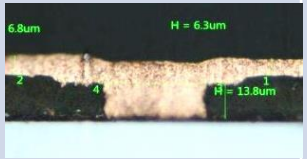
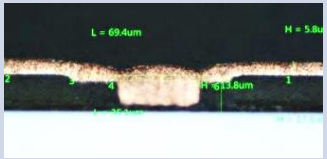
Plating Evaluation

➢ **Via/pad was fulfilled and surface Cu thickness was controlled.**

Condition #	1	2	3	4	5
Cross-section					
Remark	almost fulfilled **Cu ~6µmt**	not fulfilled	**fulfilled** Cu 14µmt	**Fulfilled** **Cu ~7µmt**	Almost fulfilled **Cu ~6µmt**

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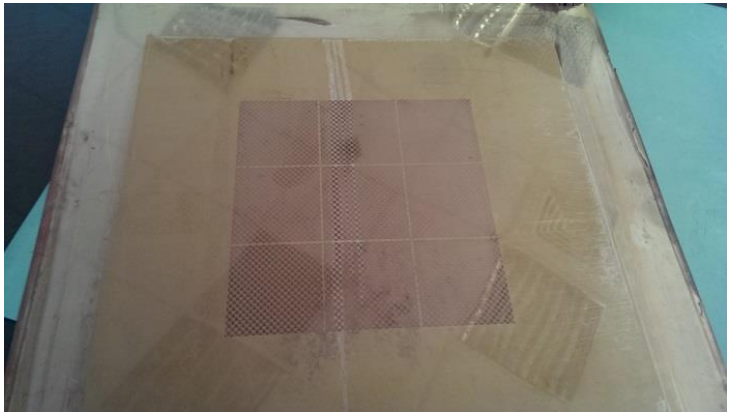
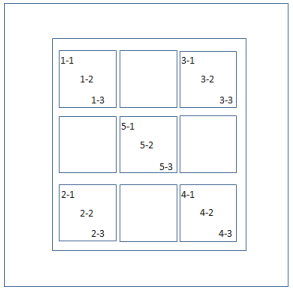
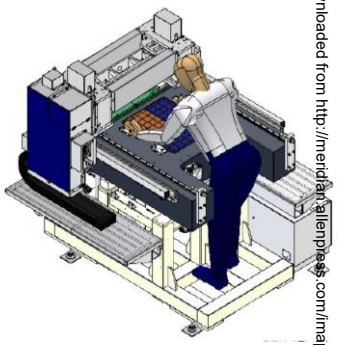
Coating Evaluation

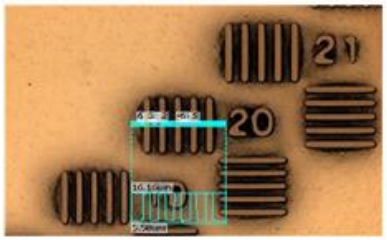
➢ Thickness uniformity of LPR on glass/organic panel

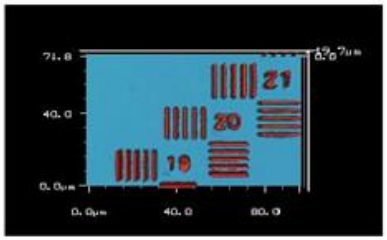


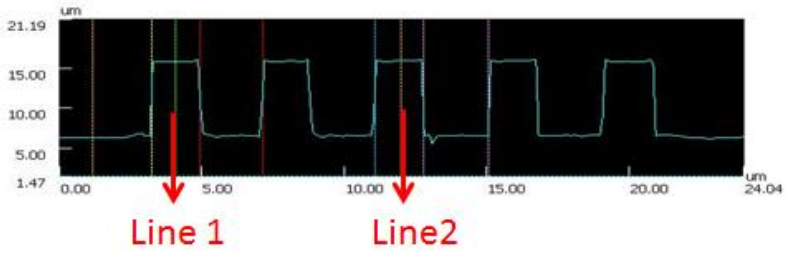


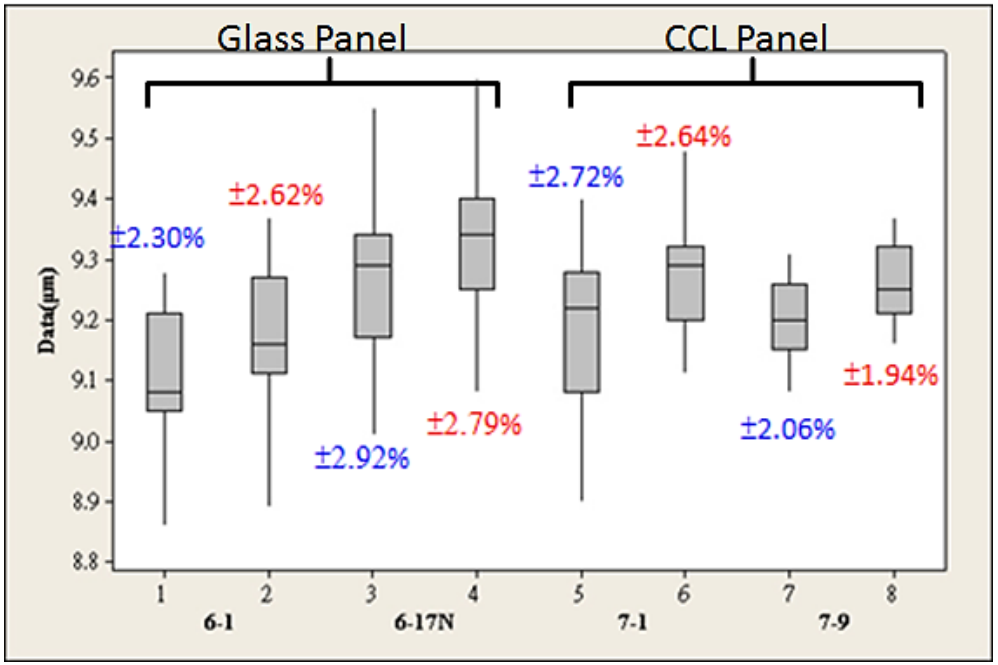


Sampling position within single panel





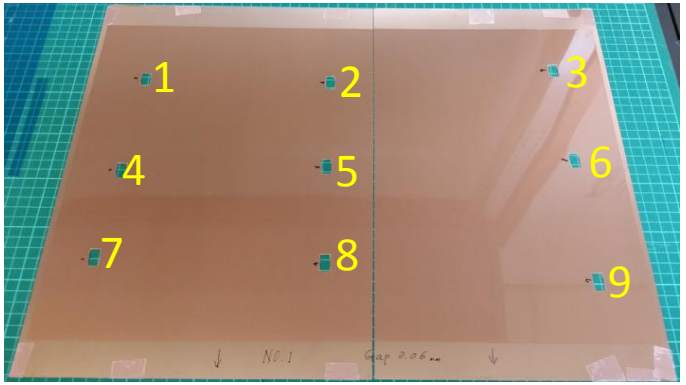


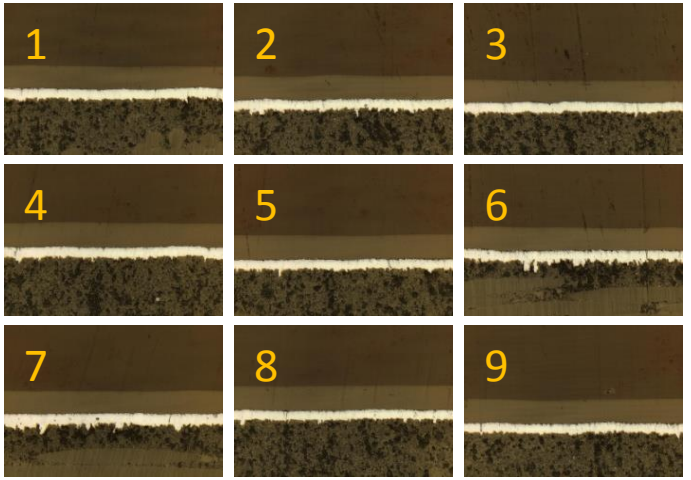


PID Coating Evaluation

Liquid PID coating on CCL:

- Over 90% material is remained on the substrate.
- Material usage is similar with spin coating on 300mm wafer.





Results:

No. 1

10.44	10.58	10.2
10.9	10.96	10.67
10.7	10.73	10.43

Average: 10.6 µm Uniformity: 3.5%

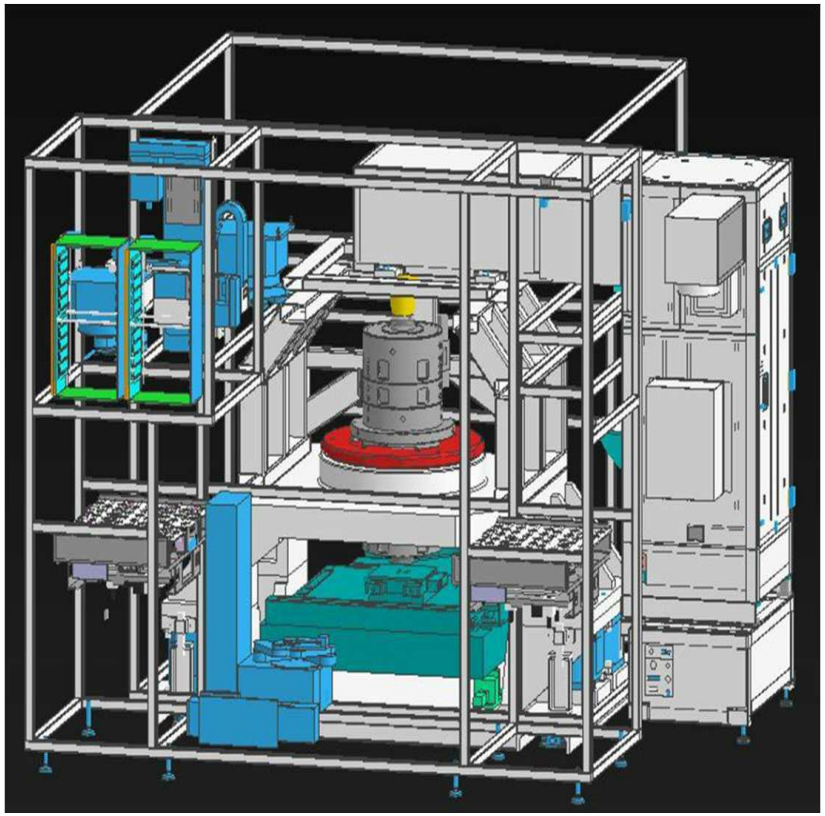
No. 2

10.42	10.61	10.21
10.77	10.88	10.53
10.76	10.77	10.15

Average: 10.6 Uniformity: 3.47%

Exposure System

- **Advanced panel stepper & coating system will be installed in Q4/2016.**



Items		Specifications
Optical capability	Reticle Size	□70mm (ϕ100mm)
	Wavelength	365nm
	Resolution	< 2μm
Working Stage	Substrate Size	□510×515mm
	Substrate thickness	0.1～2.0mm
Through put	Standard condition	30 PPH

Summary

- 508mm × 508mm 5/5μm L/S LDA LE substrate for fine line interconnection application was successfully development. L/S≤3/3μm LE technology was also demonstrate.
- PID LE could achieved L/S≤2/2μm. Reliability validation will be the focus task in the future.
- 2/2μm L/S Process line for 508mm × 508mm PID LE will be set up by E/2016.

Acknowledgment

The authors would like to thank Unimicron's NBD team for their efforts in this study.

Unimicron

謝謝您的聆聽

Thank you