Advanced Multi-Die Packaging Technology Integration IMAPS 2016: Device Packaging

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Agenda

- Product Drivers
- Packaging Constructions and Enabling Processes
- Tradeoffs
- Production Readiness

IC Packaging Evolution – System Considerations

Performance

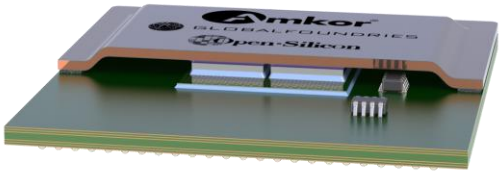
- Higher memory bandwidth
- Lower power

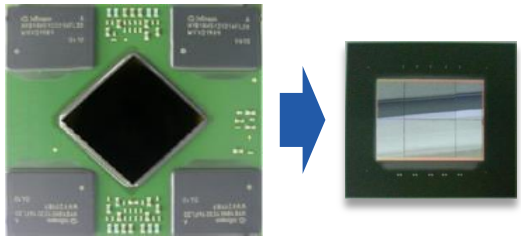
Cost Reduction

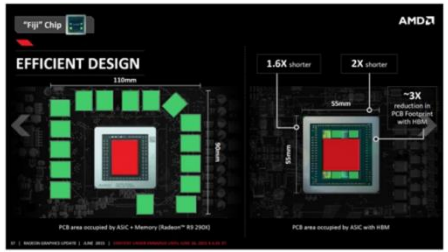
- Advanced silicon node cost avoidance
- Integrate heterogeneous die

Board Space

- Integrate multiple die on single package platform
- Reduce floor space of package platform (thin & small)







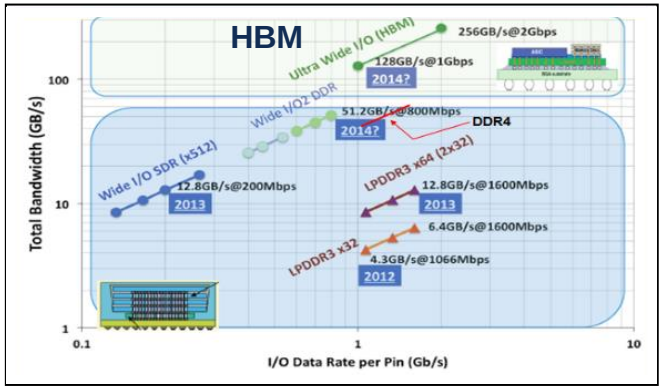
Multi Die System Packaging

Memory Bandwidth

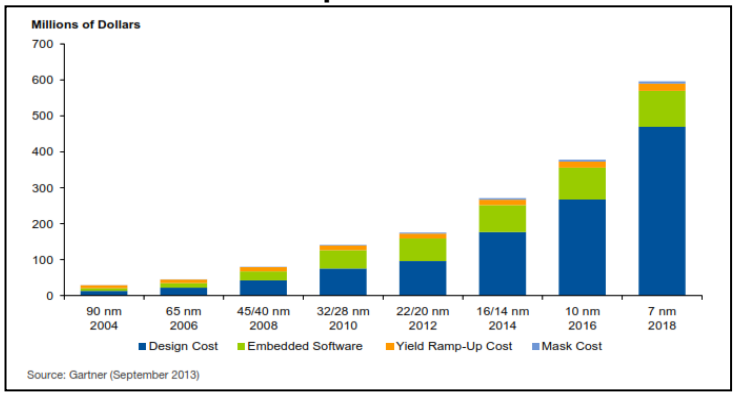
- Network Routers and Switches
- GPU: Raw processing performance
- Mobile: Display size, resolution
- **Power Efficiency**

Partitioning the Monolithic SoC

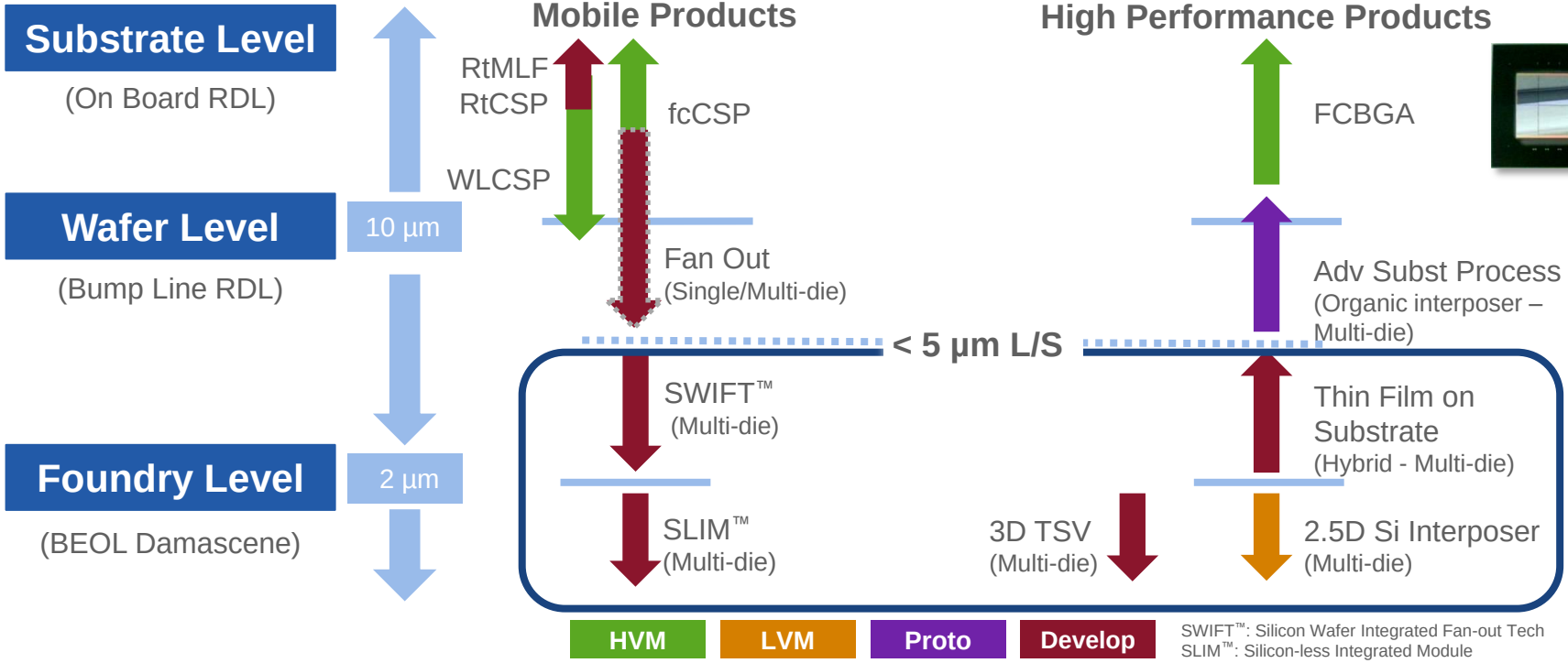
- Enables IP and IC re-use from lower cost nodes
- Lowest cost node for functional block (e.g. SERDES)
- Higher yield enabled by smaller die size
- Separating functions reduces # of layers per device



Development Costs



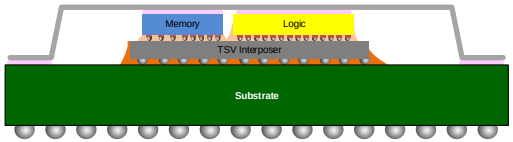
Amkor's Package Technology Integration Roadmap



Amkor's Multi-die Packages

2.5D FCBGA

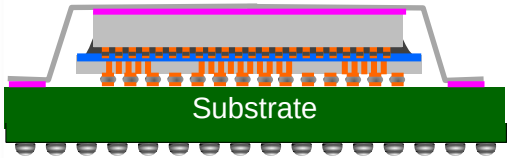
2.5D TSV Flip Chip BGA



- Homogenous & Heterogeneous die integration
- Multi-die, side by side
- <2um L/S D2D
- Bare die, Overmold, Lidded

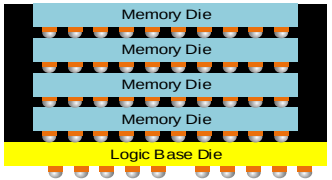
3D-TSV

3D TSV Flip Chip BGA



- Logic/Logic, and Logic/Memory Configurations
- High performance
- No Mold

3D-TSV DRAM

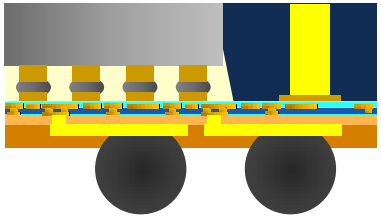


- DRAM stacking
- Molded
- Bare die & Exposed Die

Amkor's Multi-die Packages

SLIM™

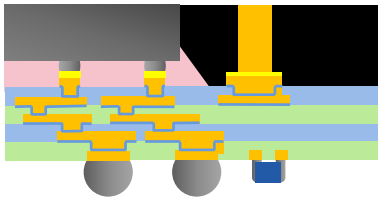
Silicon-Less Integrated Module



- Dies last
- BEOL same as 2.5D TSV
- Multi-die SOC die partition
- Foundry RDL < 2 µm L/S
- 3D POP memory compatible

SWIFT™

Silicon Wafer Integrated Fan-Out Technology



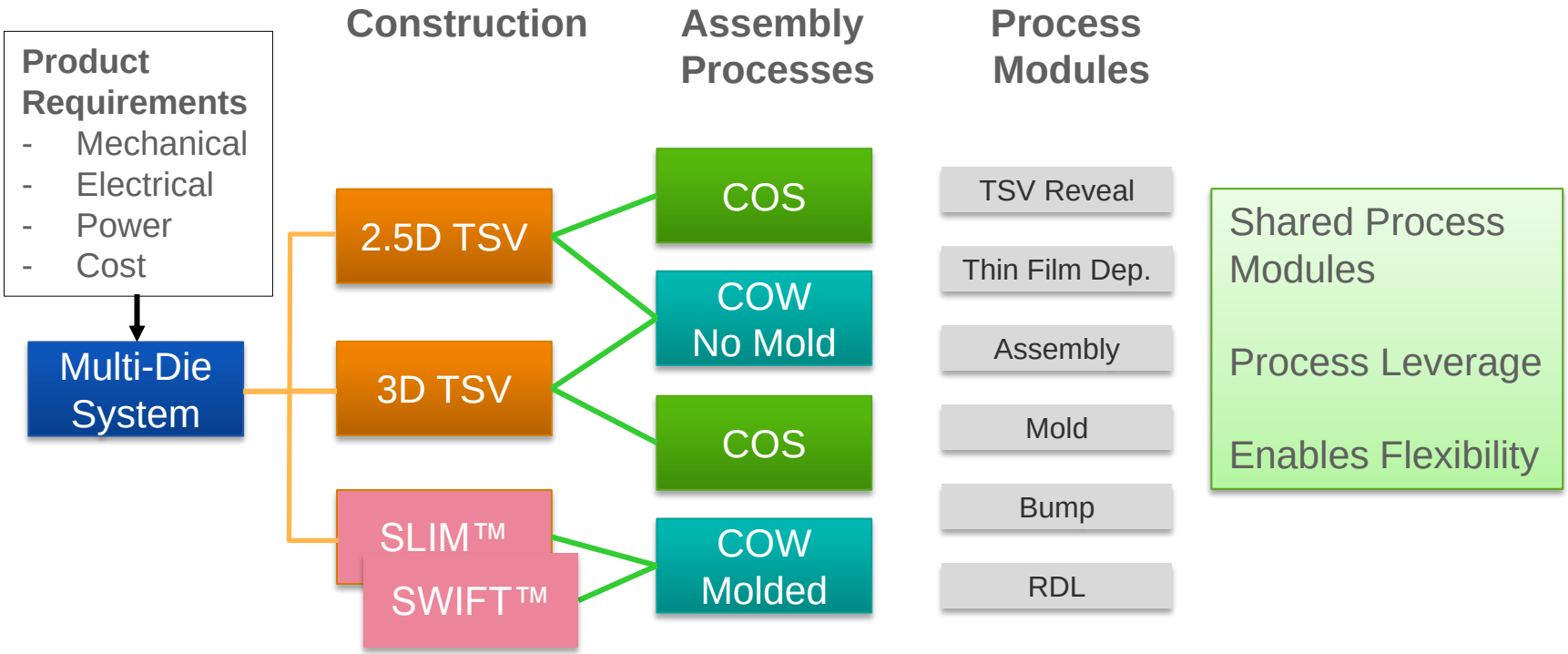
- Dies last
- Amkor multi-layer RDL
- Amkor RDL 2~5 µm L/S
- 3D POP memory compatible

Assembly Process Flexibility

- Multi-die Construction Versatility
  - 2.5D TSV (Logic + Logic, Logic + Memory, Logic + Memory + discreet IO die)
  - 3D TSV Logic + Memory
  - 3D TSV Logic + Logic
  - DRAM stacking
  - Other component types: Analog, MEMs, Sensors

- Key Factors
  - System Size (Interposer and Die sizes)-Trend is larger
  - Electrical Signaling and Power-Deliver-Network (PDN)
  - Device Power
  - Electrical Test and test points - Interim test or not
  - Cost Optimization

Package Construction and Processes



Multi-die Platform and Process Intersections

COS (Chip-on-Subst.)

- Lowest cost
- Strong leverage of FPGA assembly

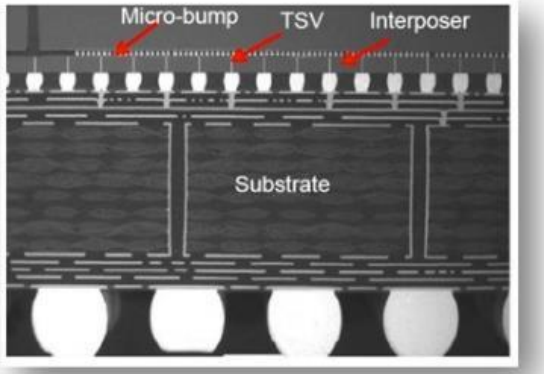
COW – No Mold

- Large die sizes
- Thin core substrates
- > Reticle size interposers

COW - Molded

- Enables SLIM™ and SWIFT™
- Required for 3D DRAM

Typical 2.5D TSV Product



Surface mount on board

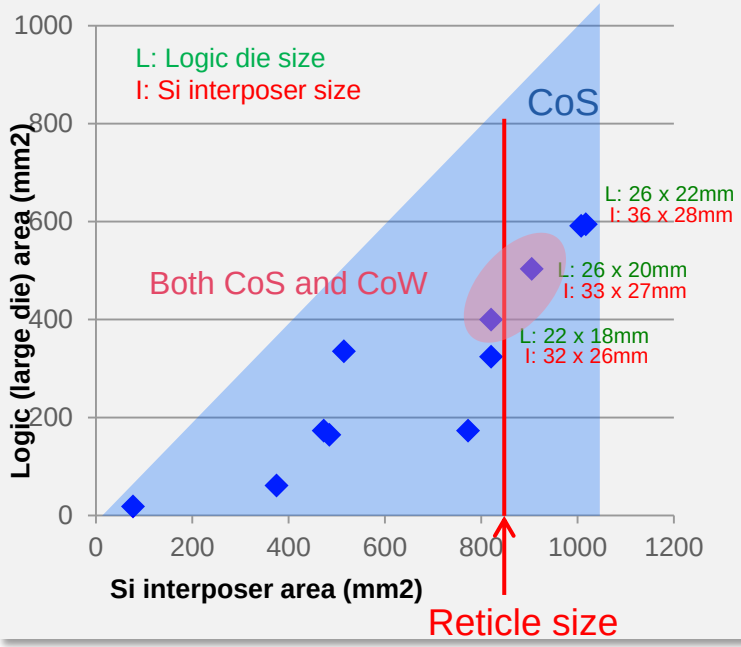
Multi-die Platform and Process Intersections

COS Process Flow (Chip-on-Subst.)

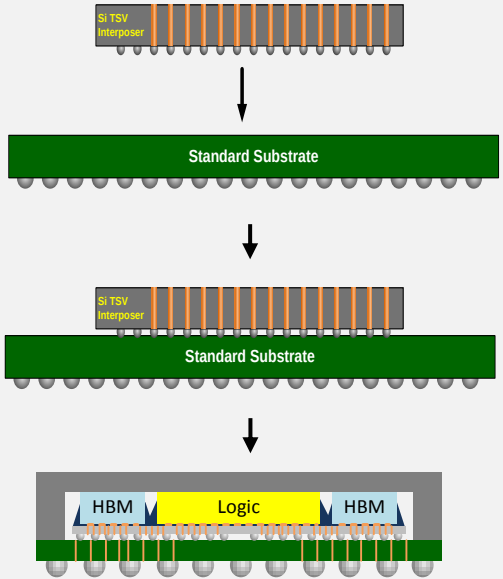
COW – No Mold

COW - Molded

- Proven 2.5D POR Process



2.5D TSV - COS



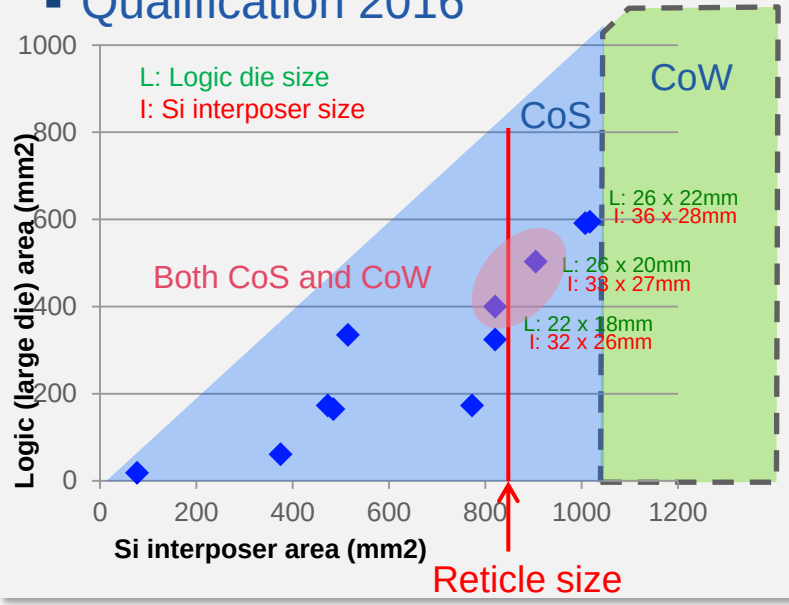
Multi-die Platform and Process Intersections

COS

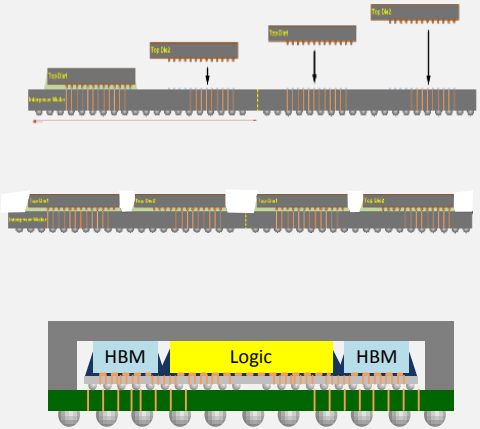
COW – No Mold

COW - Molded

- Larger interposers, larger die, thinner substrates
- Permits Interim test & mold-intolerant parts
- Qualification 2016



2.5D TSV - COW



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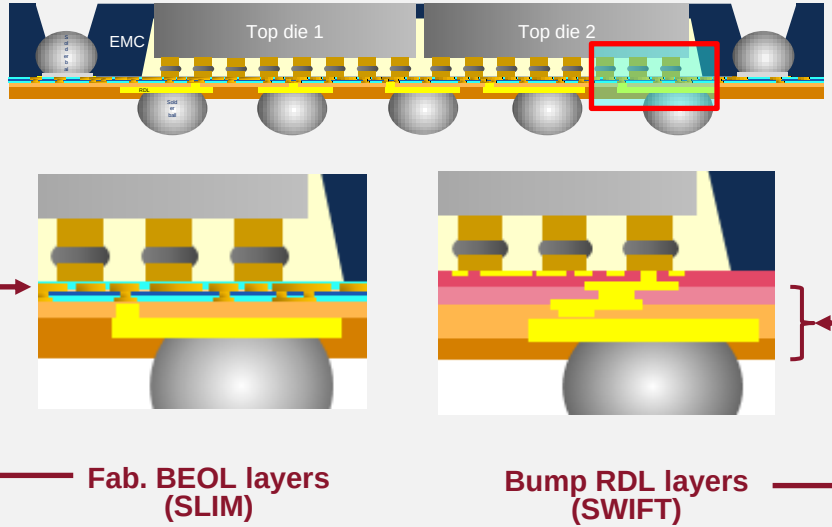
Multi-die Platform and Process Intersections

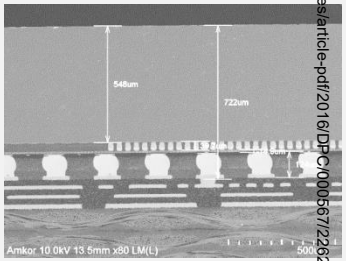
COS

COW – No Mold

COW – Mold Last

- Enables SLIM™ and SWIFT™
- Alternative for 2.5D/3D TSV





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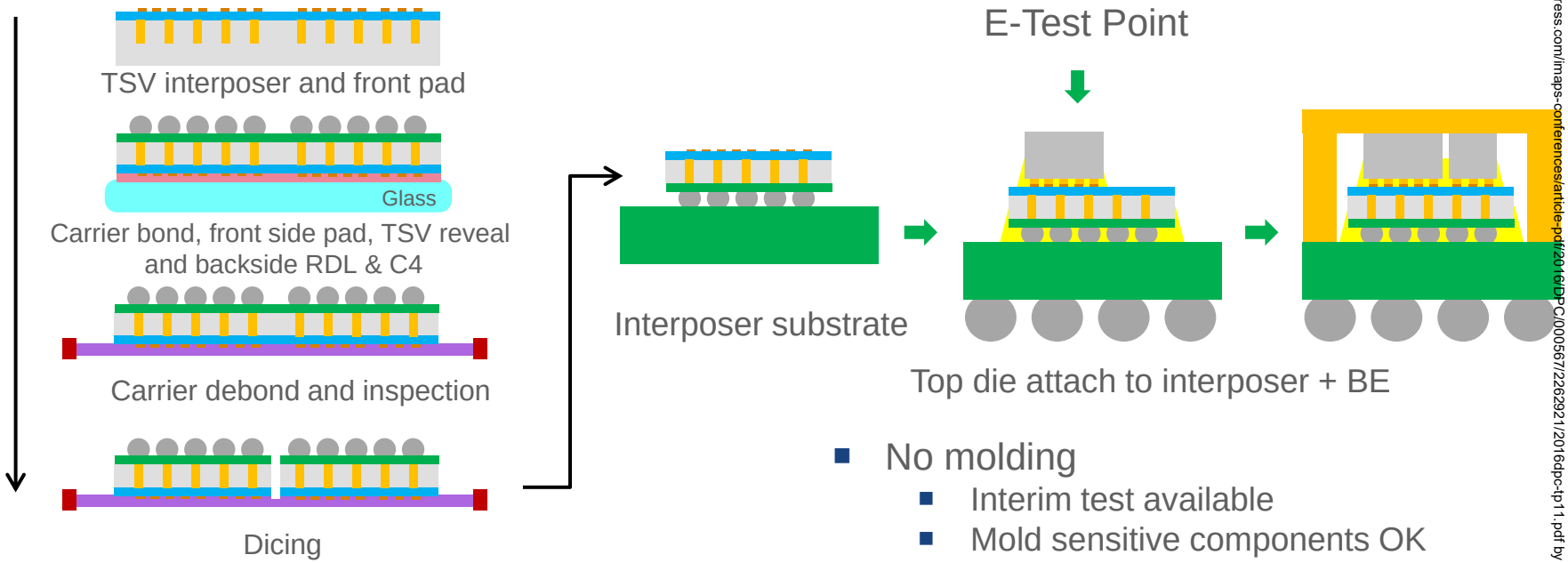
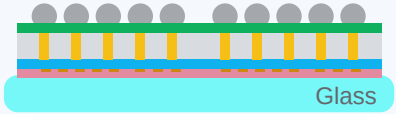
CoS Process Flow (POR)



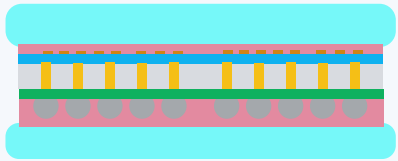
- No molding
  - Interim test available
  - Mold sensitive components OK
- Shared infrastructure with FCBGA

CoW Chip Last Process Flow

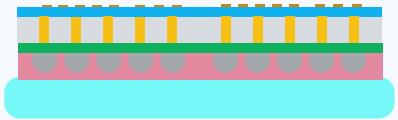
TSV interposer and front pad



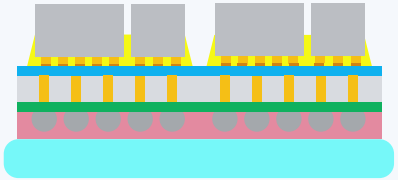
Carrier bond, TSV reveal, BS RDL & C4



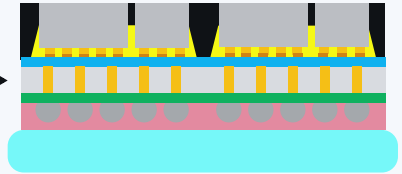
Re-bond to back side (=C4 side)



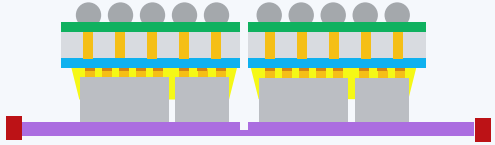
Front side carrier de-bond



CoW top die attach and underfill



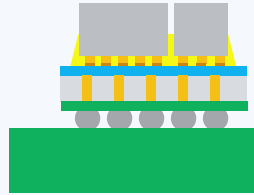
Wafer mold and mold side grind



Carrier de-bond and dicing

Non-mold CoW

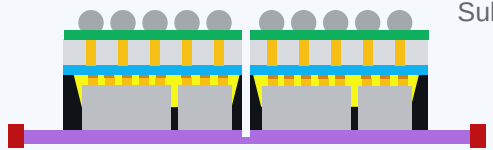
- Interim test flow available
- Interposer backside process first then top die attach



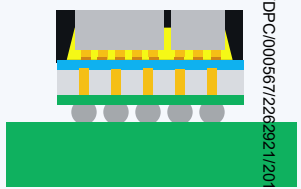
Sub-assembly to substrate

Mold last CoW

- Thinner interposers
- Interposer backside process first then top die attach



Carrier de-bond and dicing



Sub-assembly to substrate

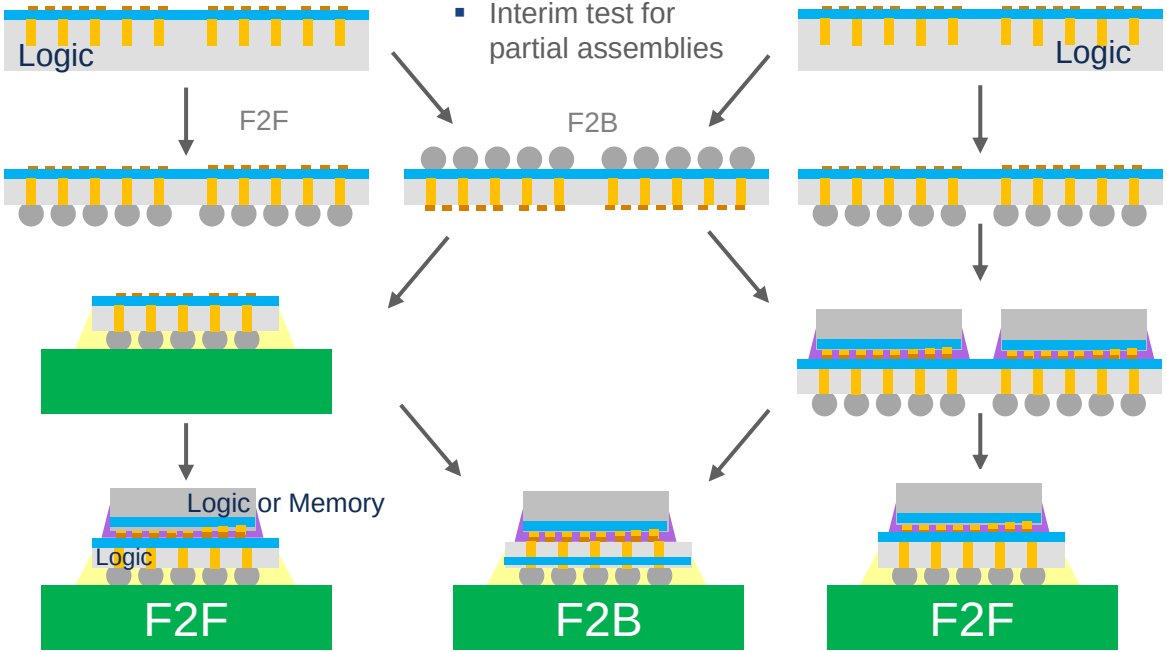
3D TSV Construction Options

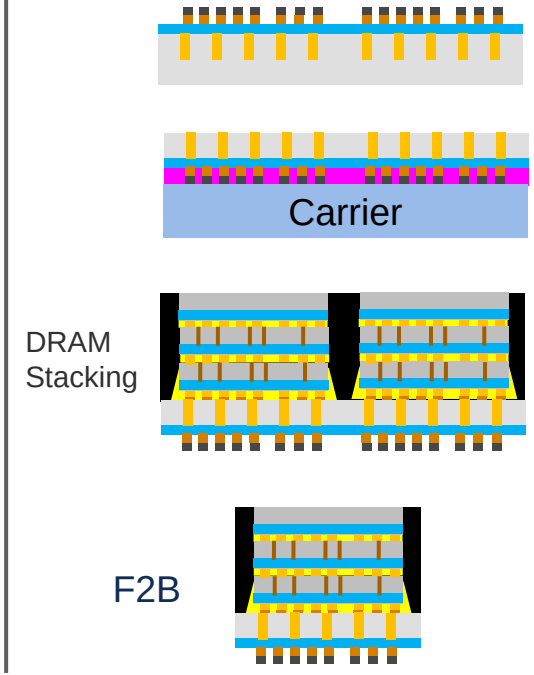
CoS Chip Last
POR for 2.5D

- Face to face or face to back stacking
- Interim test for partial assemblies

CoW Chip Last

CoW Chip Last (Molded)





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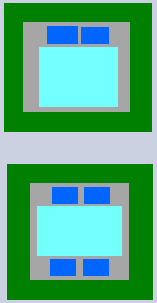
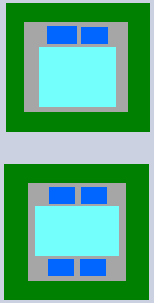
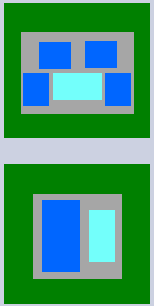
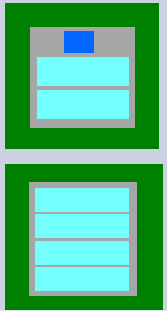
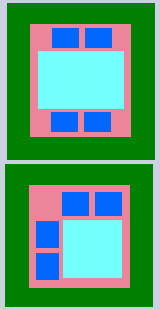
Production Readiness

Amkor's TSV Production Readiness

- MEOL: Wafer thin & back side processing
  - 300 mm TSV line installed, qualified, and production-ready
  - Yields ~ 98% (die level) with Cpk > 1.3
  - SPC control
- Assembly
  - Volume production at K4 facility
  - 2.5D TSV Yields ~98%
  - Leverage existing HVM assembly assets
  - Expertise, flexibility & scale
- Amkor Qualifications
  - 3D = 3 products @ L3-260, TCB-1000, HTS-1000, uHAST 264H
  - 2.5D = 4 products @ L4-260, TCB-1000, HTS-1000, uHAST 264H

2.5D Product Experience/TV Floor Plan

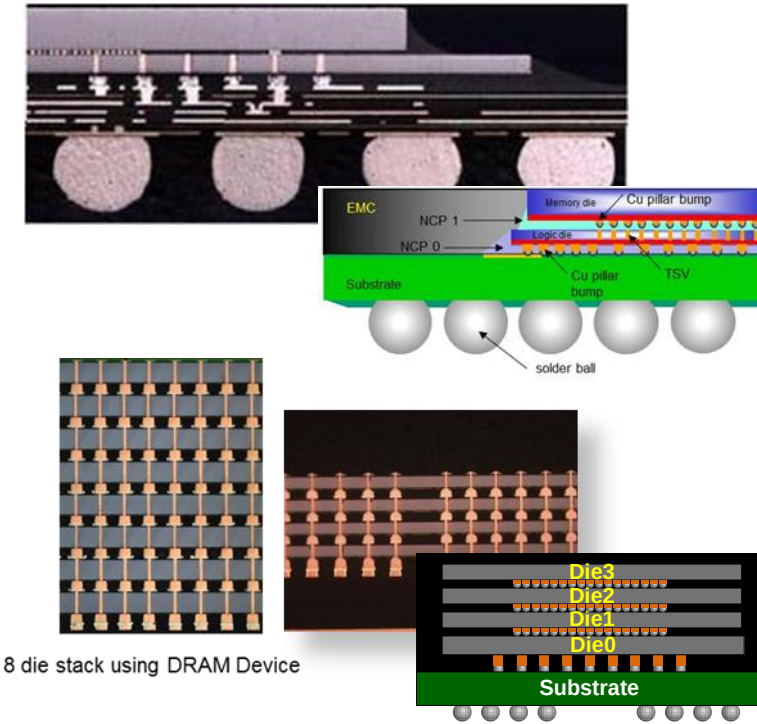
Applications	Platform	Graphics/HPC/ Network	Network/Server	FPGA	Network/Server
Interposer	Si	Si	Si	Si	Organic
Logic	40/28 nm	28 nm	28 nm	28 nm	40/45 nm
Memory/ small logic	DRAM	HBM (x2/x4)	RLDRAM (x1/x4)	SerDes	HBM / TV
Status	Qualified	Qualified	Completed Reliability/ Functional Demonstration	Demonstrated/ LVM 2013	Under Development
Floor plan					

2.5D MCM TSV Product Qualification Data

	Product 1					Product 2		Product 3			Product 4		
Package type	2.5D TSV FCBGA					2.5D TSV FCBGA		2.5D TSV FCBGA			2.5D TSV FCBGA		
Package dimensions	45 x 45 mm					55 x 55 mm		50 x 50 mm			25 x 25 mm		
Interposer size	26 x 32 mm					28 x 36 mm		26 x 32 mm			21.5 x 22.0 mm		
Logic die size	19.5 x 26.0 mm					22 x 26 mm		18 x 18 mm			5.0 x 12.7 mm		
Memory size	5.48 x 7.29 mm					5.48 x 7.29 mm		9 x 9 mm			10.9 x 16.0 mm		
Memory type	4 placements					4 placements		2 placements			1 placement		
Moisture Sensitivity Level	MSL4	90/90	90/90	90/90	30/30	MSL4	225/225	MSL4	50/50	50/50	MSL3	20/20	90/90
Highly Accelerated Stress Test	130°C/85% 96 hrs	45/45	45/45	45/45	n/a	110°C/85% 264 hrs	419/419	130°C/85% 96 hrs	25/25	25/25	130°C/85% 96 hrs	n/a	45/45
Temperature Cycling Test	T/C-B 1000x	45/45	45/45	45/45	30/30	T/C-G 1200x	440/440	T/C-B 1000x	25/25	25/25	T/C-B 1000x	20/20	25/25
	T/C-B 2000x	45/45	n/a	n/a	30/30	T/C-G 2000x	46/46	T/C-B 2000x	n/a	25/25	T/C-B 2000x	n/a	15/15
High Temperature Storage Test	150°C 1000 hrs	45/45	45/45	45/45	n/a	150°C 1000 hrs	248/248	150°C 1000 hrs	25/25	25/25	150°C 1000 hrs	n/a	15/15

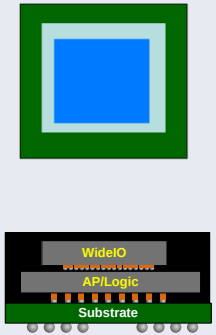
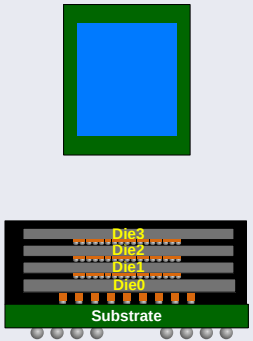
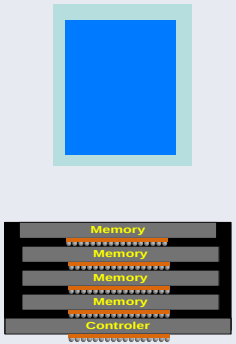
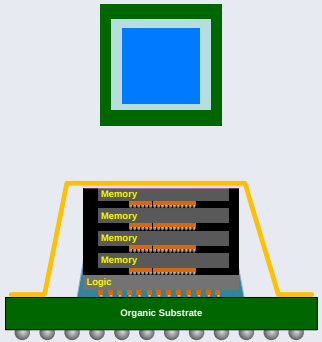
Amkor's 3D TSV Platform

- 3D – Tier-to-tier stacking
  - Wide variety of products assembled to date
    - Several years of development completed
    - 3D TSV assembly platform qualified at Amkor
    - TSV wafer finishing at Amkor
  - Logic + Memory on substrate assembly
    - TSV logic wafers from two foundry suppliers
    - Memory TSV wafers and cubes from three suppliers
  - Memory + Memory on substrate assembly
    - Over-molded final assembly
    - Exposed die and heat spreader options available



8 die stack using DRAM Device

3D Product Experience/TV Floor Plan

Applications	Platform	AP	DDR4-3DS	HBM	Logic + DRAM
Logic	28 nm	28 nm	n/a	2x-nm DRAM	28 nm
Memory	DRAM	Wide I/O	DDR4	HBM	Custom
Status	Qualified	Qualified	Passed Package Reliability/ Development Completed	Under Development	Under Development
Floor plan					

3D MCM TSV Product Qualification Data

	Product 1				Product 2				Product 3		
Package Type	3D TSV FCCSP				3D TSV FCCSP				3D TSV FCCSP		
Package Dimensions	14 x 14 mm				15 x 15 mm				14 x 14 mm		
Logic Die Size	8.5 x 8.5 mm				12 x 12 mm				6 x 6 mm		
Memory Size	8.6 x 9.2 mm				10 x 10 mm				8.6 x 9.2 mm		
Memory Type	Wide I/O				Wide I/O				Wide I/O		
Moisture Sensitivity Level	MSL3	90/90	90/90	120/120	MSL3	90/90	90/90	90/90	MSL3	90/90	90/90
Highly Accelerated Stress Test	130°C/85% 96 hrs	45/45	45/45	45/45	130°C/85% 96 hrs	45/45	45/45	45/45	130°C/85% 96 hrs	45/45	45/45
Temperature Cycling Test	T/C-B 1000x	45/45	45/45	45/45	T/C-G 1000x	45/45	45/45	45/45	T/C-B 1000x	45/45	45/45
	T/C-B 2000x	45/45	15/15	n/a	T/C-G 2000x	15/15	n/a	n/a	T/C-B 2000x	n/a	n/a
High Temperature Storage Test	150°C 1000 hrs	45/45	45/45	45/45	150°C 1000 hrs	45/45	25/25	45/45	150°C 1000 hrs	25/25	25/25

Thank You

