IMAPS 12th International Conference and Exhibition on Device Packaging

Advances in Aligned Wafer Bonding Enabled by High Vacuum Processing

Eric F. Pabo, Business Development Manager MEMS

www.EVGroup.com

Advances in Aligned Wafer Bonding Enabled by High Vacuum Processing

- Background and Motivation
- Vacuum Encapsulation
- Covalent Bonding Process
- Process Equipment
- Summary & Conclusions
- Questions & Answers

Advances in Aligned Wafer Bonding Enabled by High Vacuum Processing

Background and Motivation

Advances in Aligned Wafer Bonding Enabled by High Vacuum Processing

Background and Motivation

Requirements for Engineered Substrates Made by Wafer Bonding

- Capable Of Bonding Materials With Large CTE (Coefficient Of Thermal Expansion)
- Minimal Amorphous Zone Post Bond
- Electrically Conductive Interface
- Optically Transparent Interface

Background and Motivation

Applications for Engineered Substrates Made by Wafer Bonding

- Multi-junction Solar Cells
- Temperature Compensated SAW Filters
- High Performance LED Manufacturing
- Formation of Vertical Semiconductor Devices
- Layer Transfer (for example GaN)

Advances in Aligned Wafer Bonding Enabled by High Vacuum Processing

Background and Motivation

EVG

Requirements for High Vacuum Encapsulation by Wafer Bonding

- Effective Bake-Out Process
- Dual Temperature Bake-Out
- Getter Activation
- Alignment in Vacuum
- Formation of Hermetic Seal

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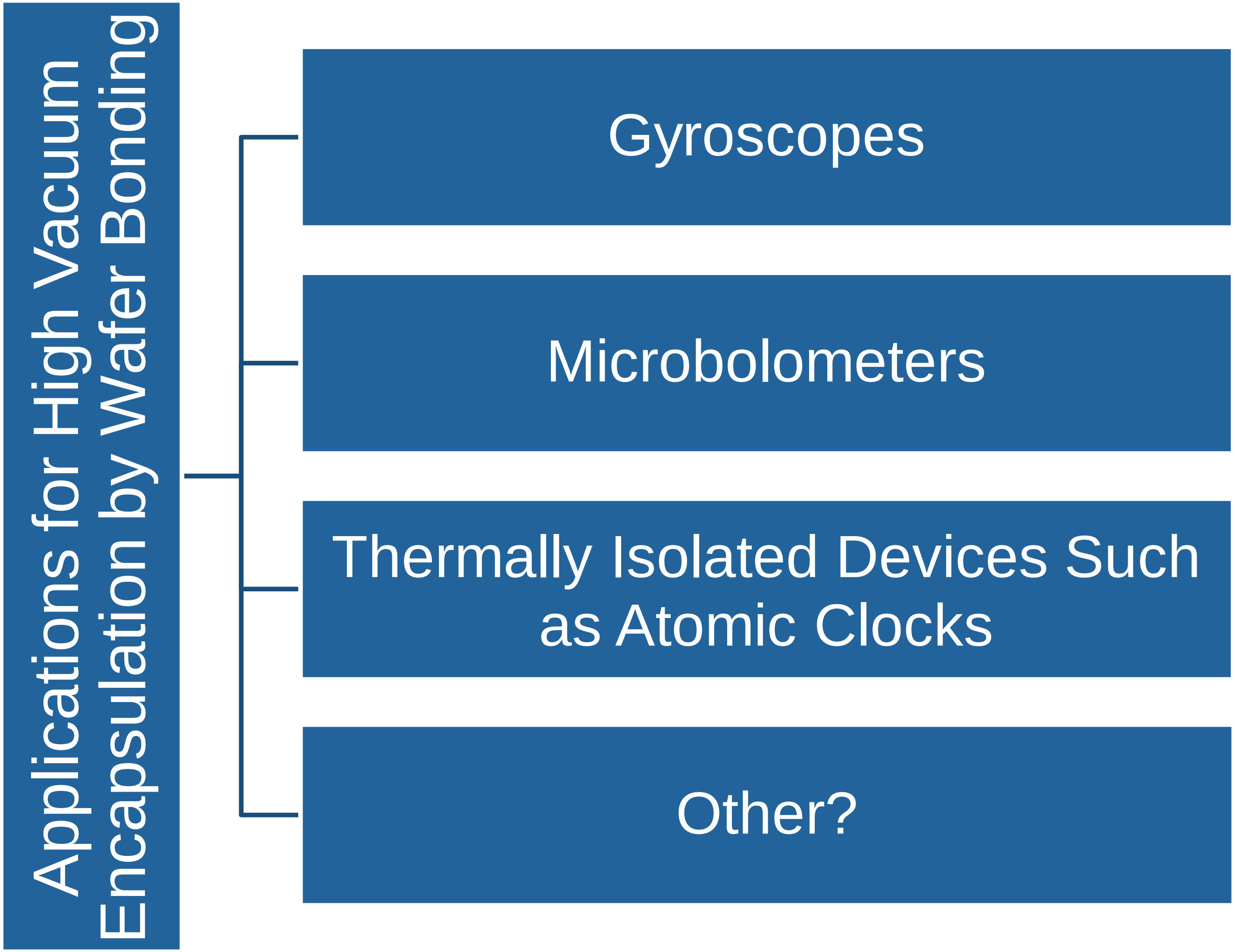
Background and Motivation



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Vacuum Encapsulation

Vacuum Encapsulation – Process Variables

- **Incoming Substrates Variables**
  - Size
  - Thickness
  - Bulk Material
  - Surface Material and Oxide Thickness
  - Surface Roughness
  - Cavities
  - Adsorbed Moisture
- **Bake-Out Variables**
  - Time
  - Temperature
  - Vacuum Level
- **Handling Process Variables**
  - Vacuum Level
- **Optical Alignment**
  - Alignment
- **Incoming Variables for Bonding Process**
  - Adsorbed moisture level
  - Surface Roughness
  - Oxide Thickness
  - Amorphous Layer Thickness
- **Bonding Process Variables**
  - Temperature
  - Applied Force / Pressure on Interface
  - Vacuum Level in Bond Chamber
  - Time
- **Bonding Process Output Variables**
  - Alignement
  - Voids
  - Strength
  - Getter Effectiveness
  - Hermeticity of Bond Line
  - Vacuum Level in Cavity
  - Stress Level / Bow and Warp

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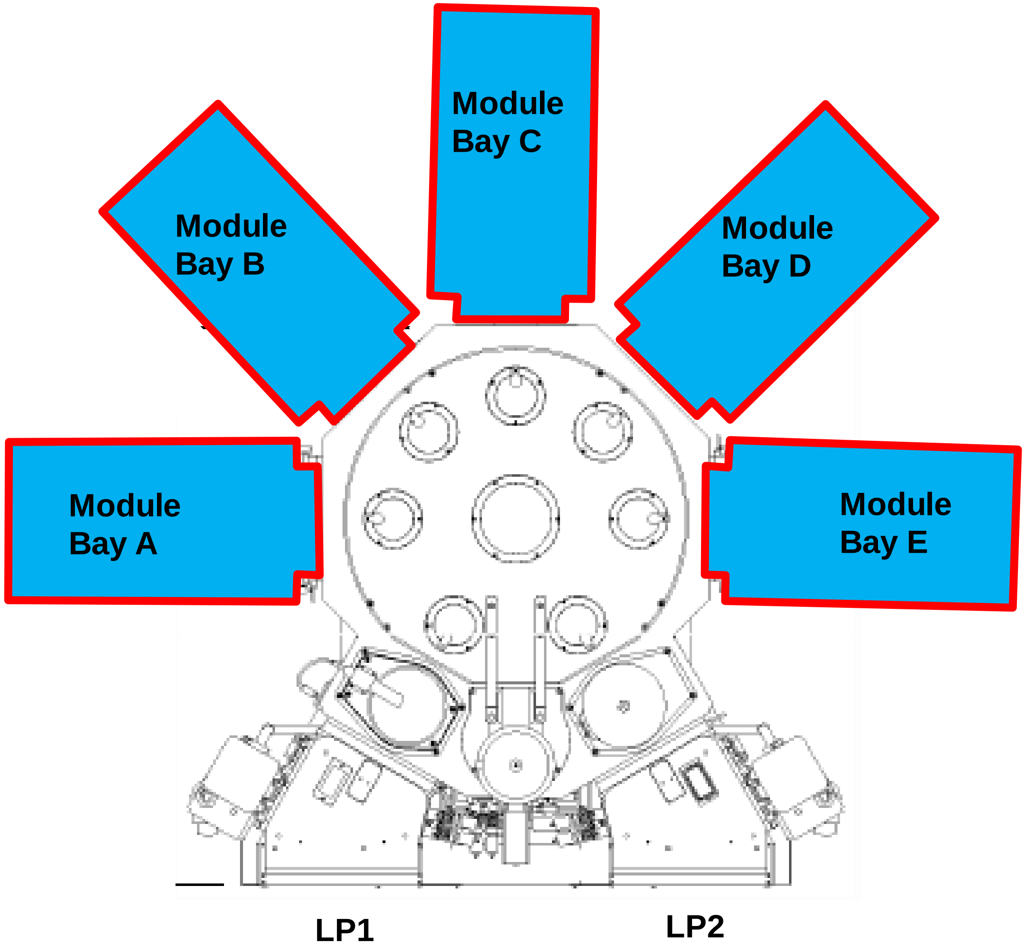
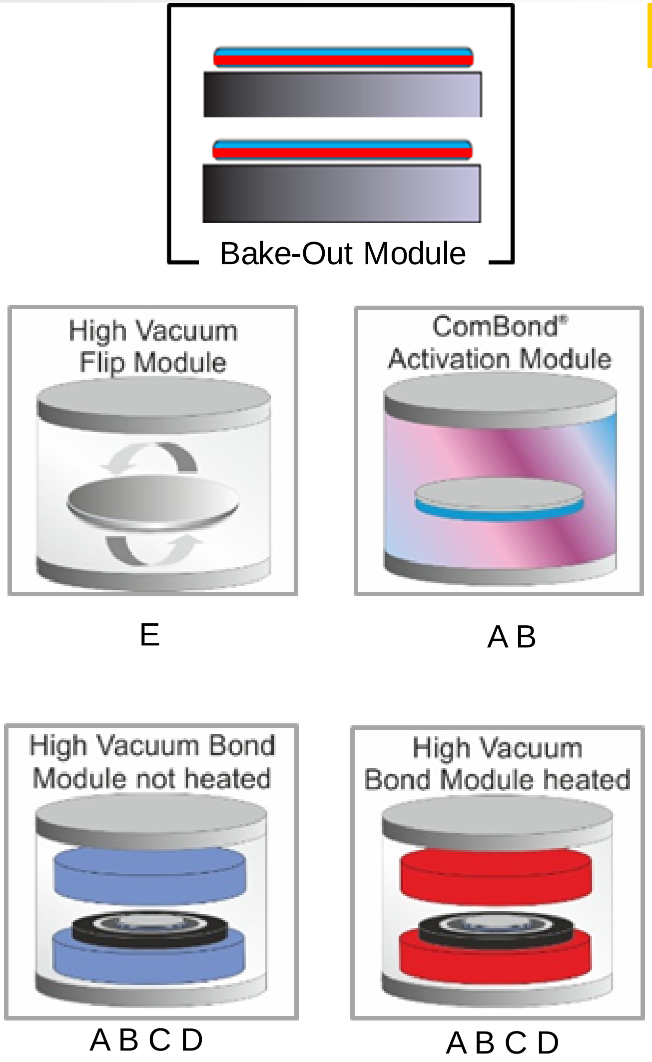
High Vacuum Wafer Bonding Cluster Tool





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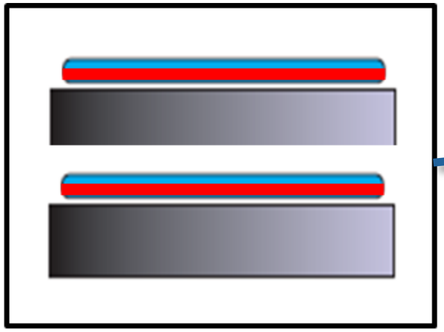
Optimized Bake-Out

- Wafers are baked out prior to aligning and clamping.
  - Open faced
  - Wafers stay in vacuum until bonding is completed



Conceptual drawing of bake out module

  - Much larger spacing then when clamped
    - Typical clamp thickness is 100 – 200 µm
    - Stacked bake out module will can have spacing of 10 – 20 mm
  - This increased temperature and increased spacing improves the desorption of water molecules from the surface of the wafer(s)

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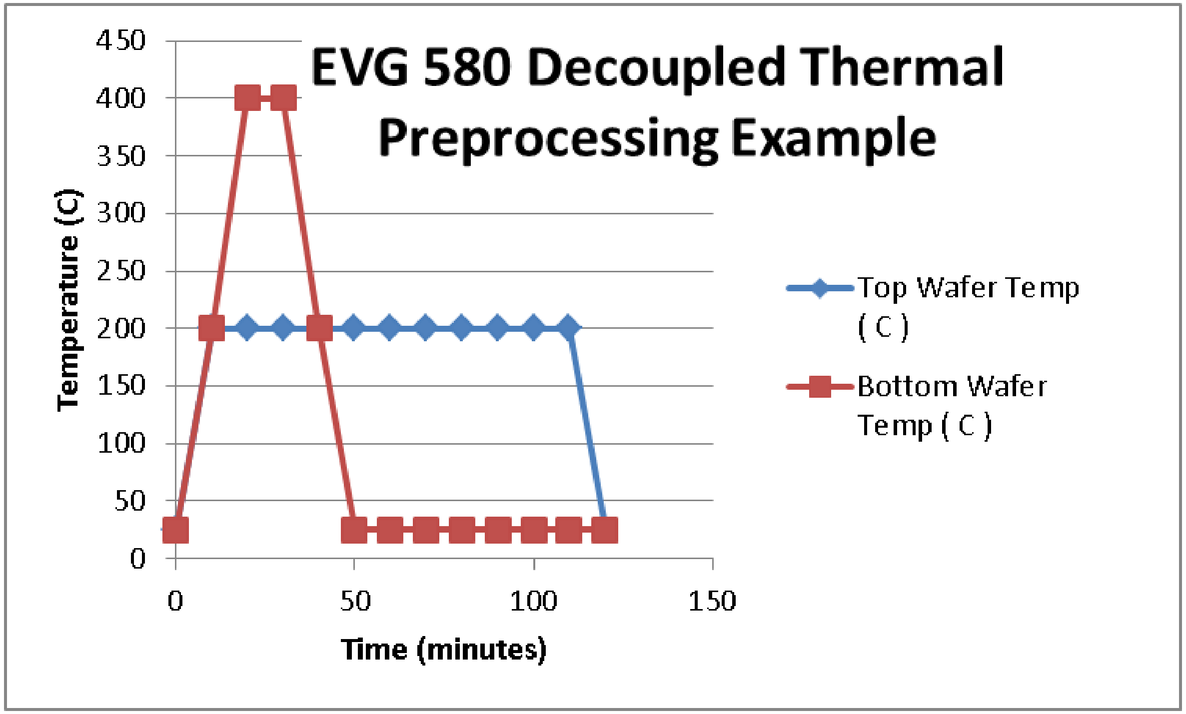
Separated Top and Bottom Wafer Pre-Processing

- Improved Getter Activation due to Separate Preprocessing of Top and Bottom Wafer.
  - Getter wafer can be activated at a high temperature
  - Other wafer can be baked out at lower temperature if required.



High Vacuum Wafer Bonding Cluster Tool

- Because of the cluster tool configuration, custom preprocessing modules can be developed and added without redesigning the tool
- Examples:
  - Reducing atmosphere; such as forming gas
  - Sputtering of a surface
  - Special customer requirements

Advances in Aligned Wafer Bonding Enabled by High Vacuum Processing

Covalent Bonding at Low Temperature

Covalent Bonding at Low Temperature – Process Variables

- **Incoming Substrates Variables**
  - Size
  - Thickness
  - Bulk Material
  - Surface Material and Oxide Thickness
  - Surface Roughness
- **Surface Treatment Process Variable**
  - Proprietary
- **Surface Treatment Output Variables**
  - Surface Roughness
  - Oxide thickness
  - Amorphous Layer Thickness
- **Handling Process Variables**
  - Vacuum Level
- **Incoming Variables for Bonding Process**
  - Surface Roughness
  - Oxide Thickness
  - Amorphous Layer Thickness
- **Bonding Process Variables**
  - Temperature
  - Applied Force / Pressure on Interface
  - Vacuum Level in Bond Chamber
  - Time
- **Bonding Process Output Variables**
  - Voids
  - Strength
  - Amorphous Layer Thickness
  - Oxide Present in Interface
  - Electrical Characteristics
  - Stress Level / Bow and Warp

Covalent Bonding at Low Temperature

- ***Why does ComBond® require high vacuum?***
  - → If an oxide-free interface is required, it is not enough to remove the oxide. Re-deposition of oxide needs to be prevented, as well.

Base Pressure [mbar]	Vacuum Classification	Comment	Time to form 1 monolayer [s]
1000	Rough Vacuum	Atmosphere	4.10E-08
100	Rough Vacuum		4.10E-07
10	Rough Vacuum		4.10E-06
1	Rough Vacuum		4.10E-05
0.1	Rough Vacuum	EVG®810LT process pressure level	4.10E-04
0.01	Rough Vacuum		0.004
0.001	Rough / Medium Vacuum	EVG®810LT base pressure level	0.041
1.00E-04	Medium Vacuum		0.41
1.00E-05	Medium Vacuum	EVG®580 ComBond® process pressure level	4.10
1.00E-06	Medium / High Vacuum		41.05
1.00E-07	High Vacuum		410.45
1.00E-08	**High Vacuum**	**EVG®580 ComBond® base pressure level**	**4104.54**
1.00E-09	High / Ultra High Vacuum		4.10E+04
1.00E-10	Ultra High Vacuum		4.10E+05

Immediate reoxidation

Enough time left to contact wafers before reoxidation occurs.

Assumptions:
- Each H_2O molecule from background contamination that hits the Si surface will stick.
- H_2O partial pressure is 10 % of base pressure.

Covalent Bonding at Low Temperature

Challenges

- Very stringent surface roughness requirements
- Entire process must be done under high vacuum

Benefits

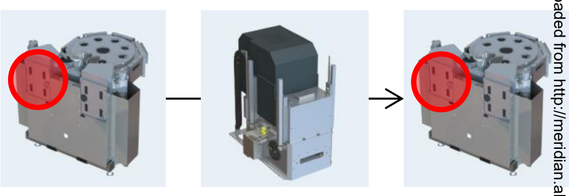
- High strength
- Covalent Bonds can be formed at room temperature
- Suitable for heterogenous integration of materials with different CTEs

Process Results

Si – Si Wafer Bonding

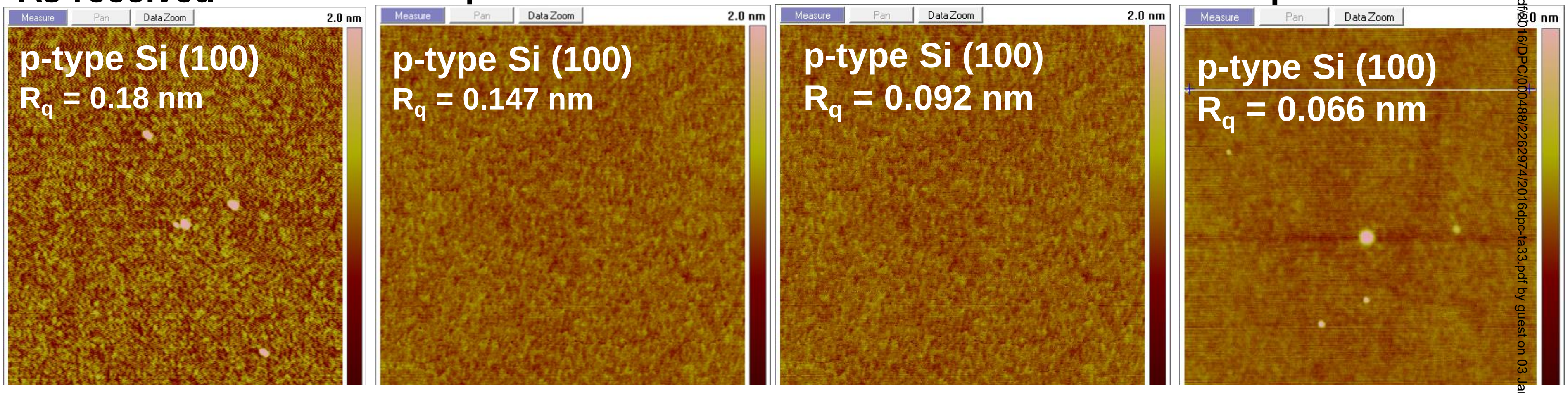
Pre-Bonding Surface Characterization: Topography

AFM Measurements



Low microroughness profiles are preserved during activation.

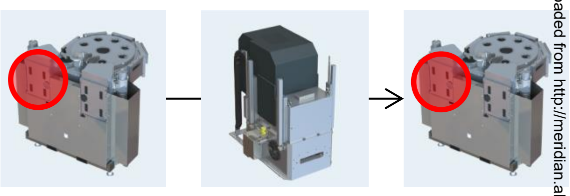
As received | **Recipe 1** | **Recipe 2** | **Recipe 3**



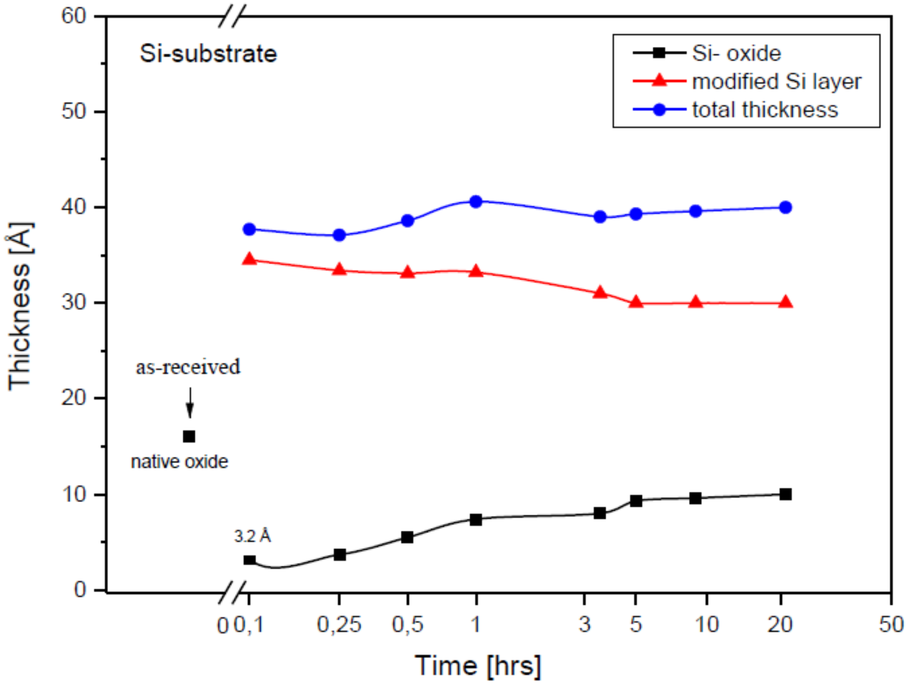
R_q < 0.5 nm for all samples / recipes

Pre-Bonding Surface Characterization: Chemical / Structural

Ellispometry (ambient air)

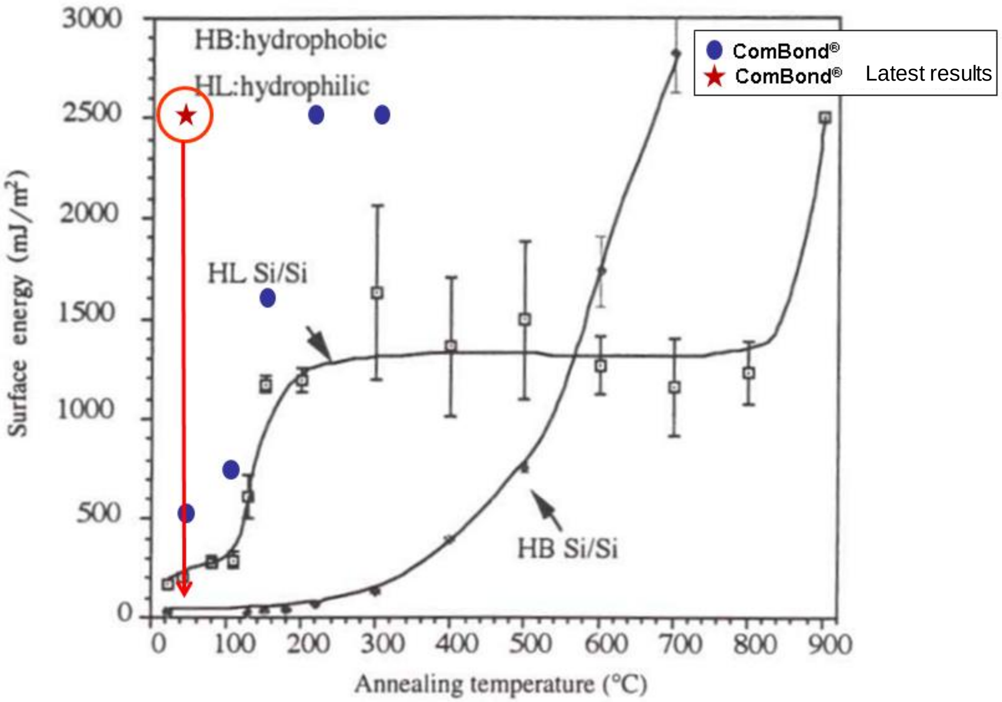


Native oxide was reduced to < 3.2 Å.



Bonding Trials

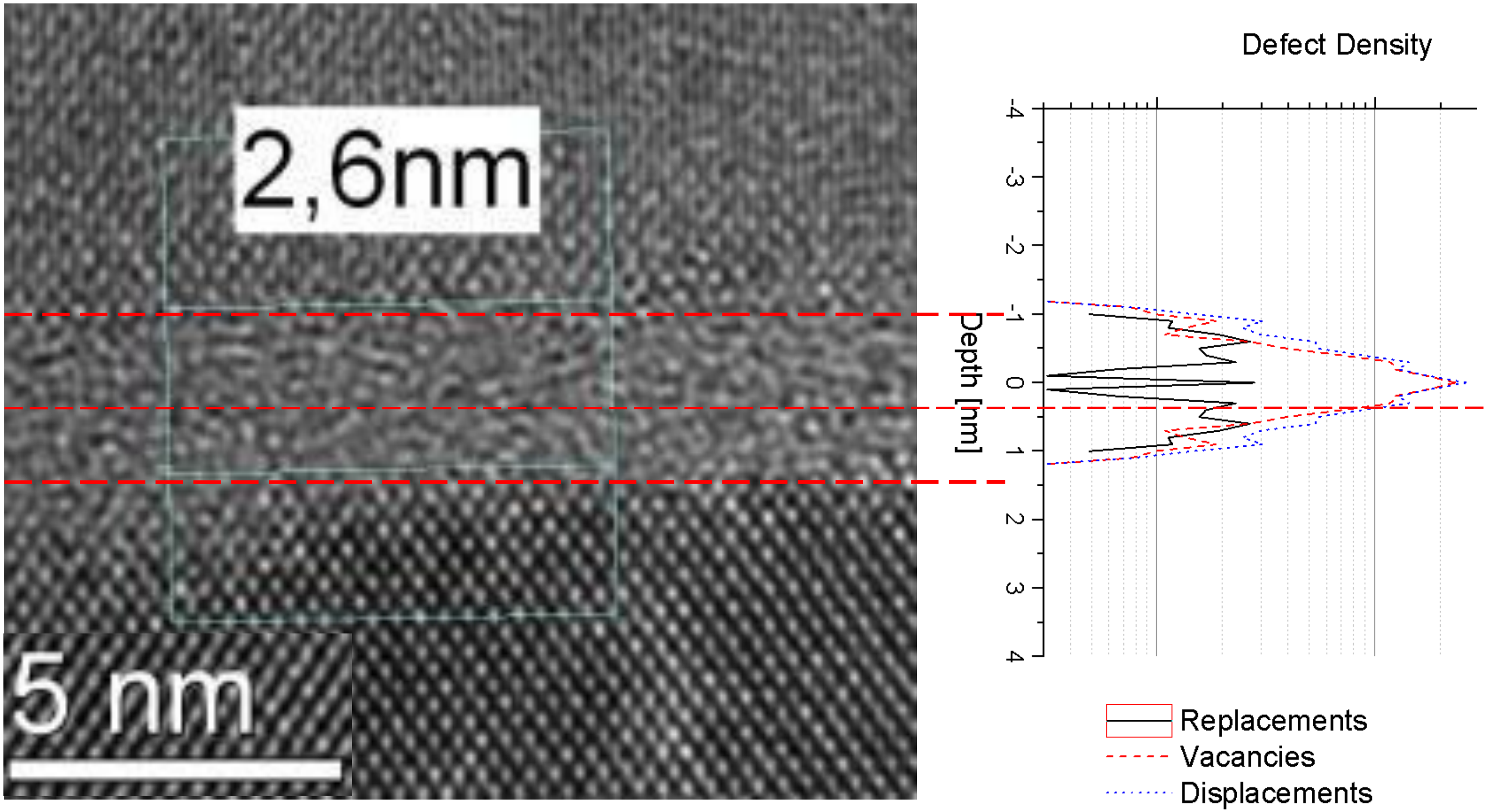
Overview



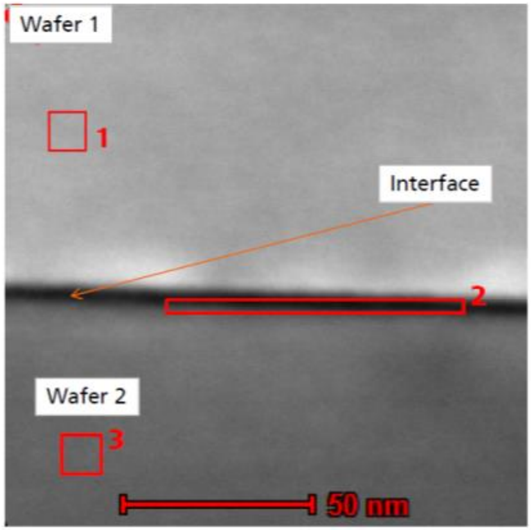
Q.-Y. Tong and U. Gösele, in *Semiconductor Wafer Bonding: Science and Technology,* p. 118, John Wiley And Sons, Inc., New York (1999).

Reproducibly achieved bond strength ≈ bulk fracture strength **without any thermal treatment** before, during or after processing.

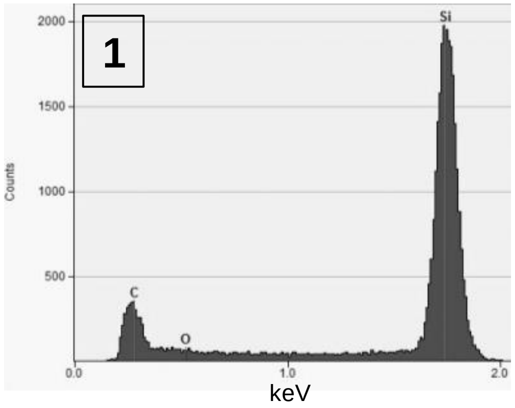
HR-TEM Measurements
sample #1- medium energy

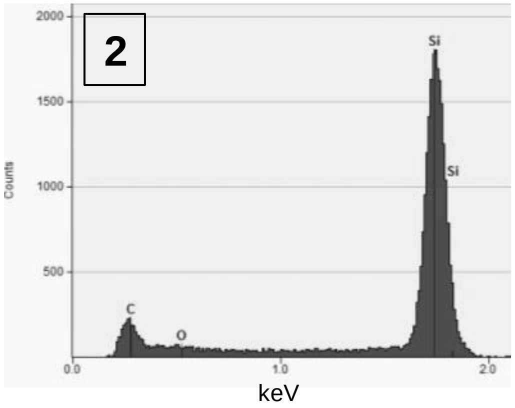


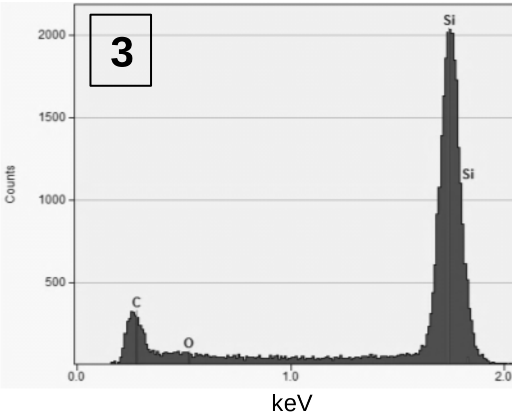
EDXS Measurements



- EDXS was performed on 3 rectangular areas.
- Spectra show the interface is most likely not composed of SiO_x.
- O and C signals have nearly the same peak intensity, regardless at which position the spectra were taken.
- This indicates O and C contamination is due rather to sample preparation.

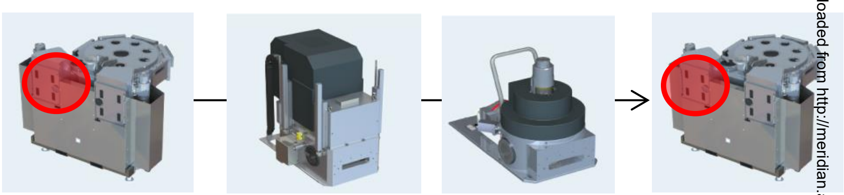


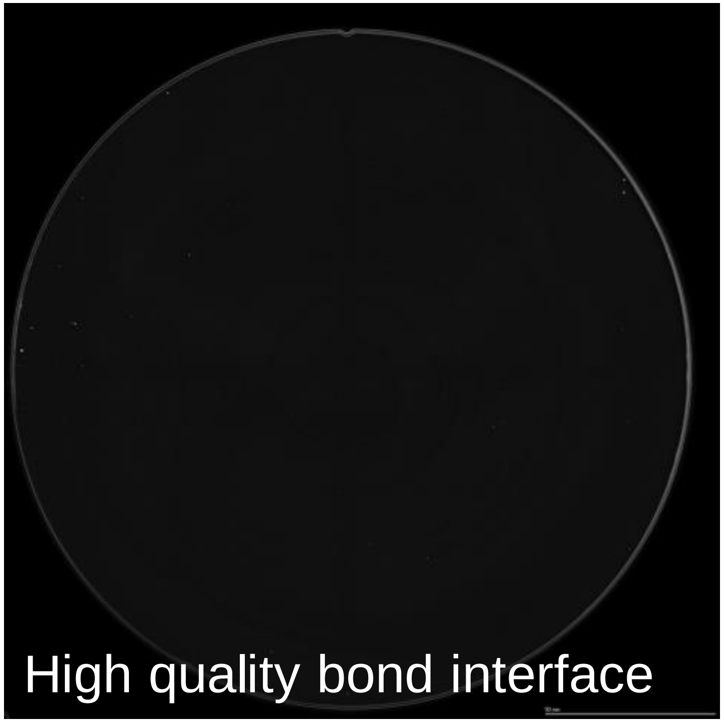


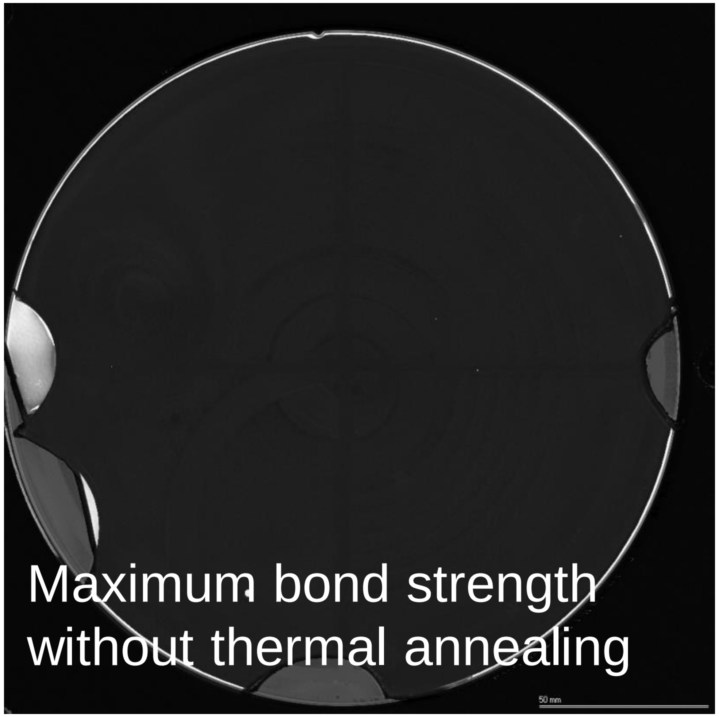


Bonding Interface Characterization: Uniformity

C-SAM / Maszara Test

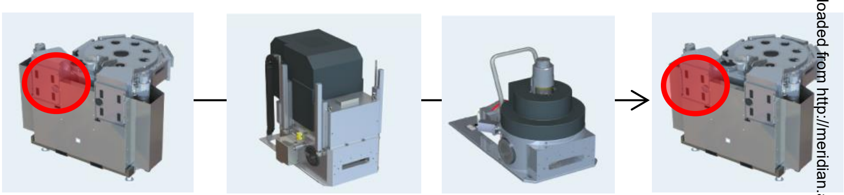




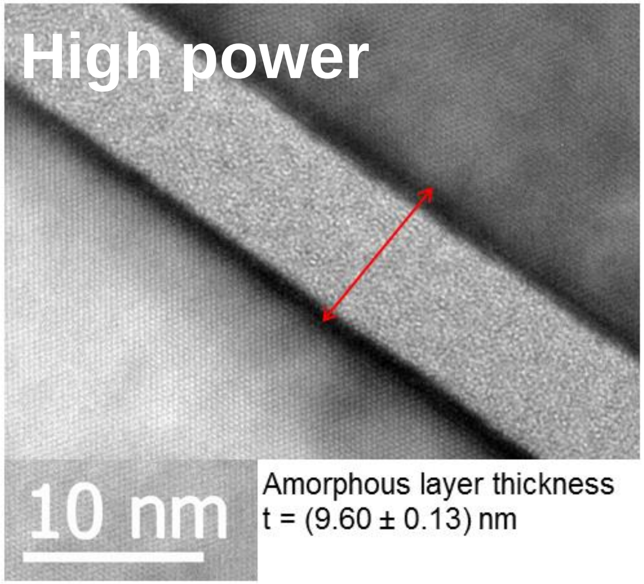


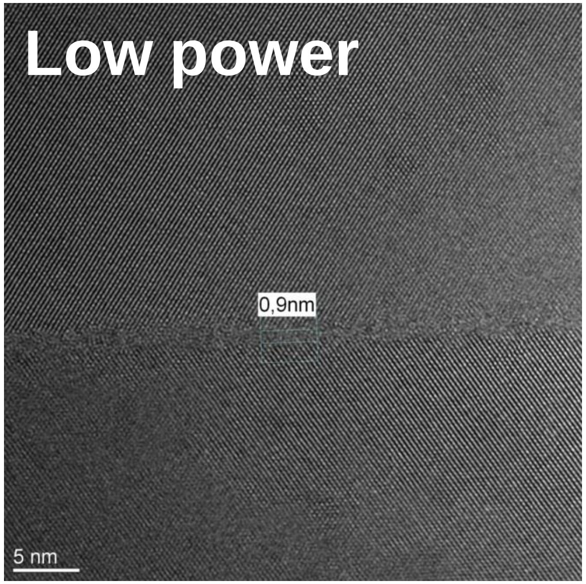
Bonding Interface Characterization: Structural

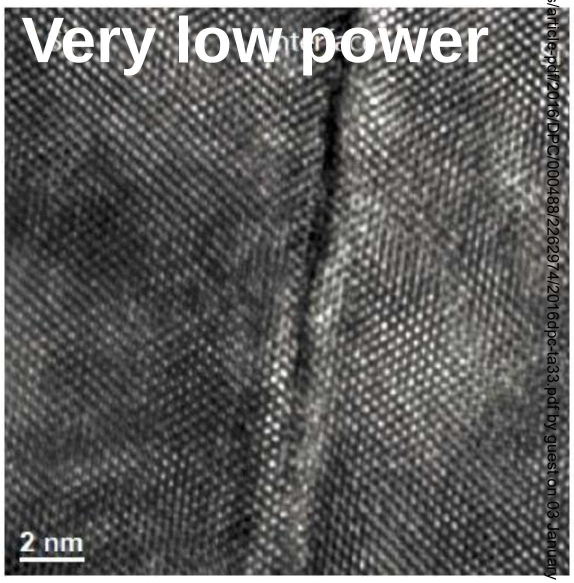
HR-TEM



Influence of activation power on amorphous layer thickness in a nutshell:

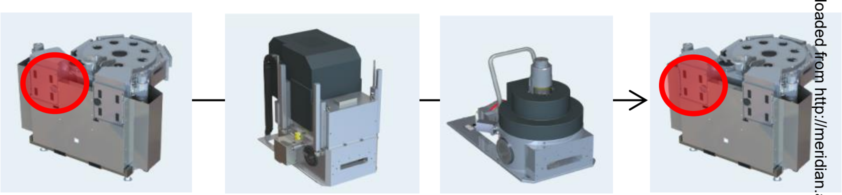




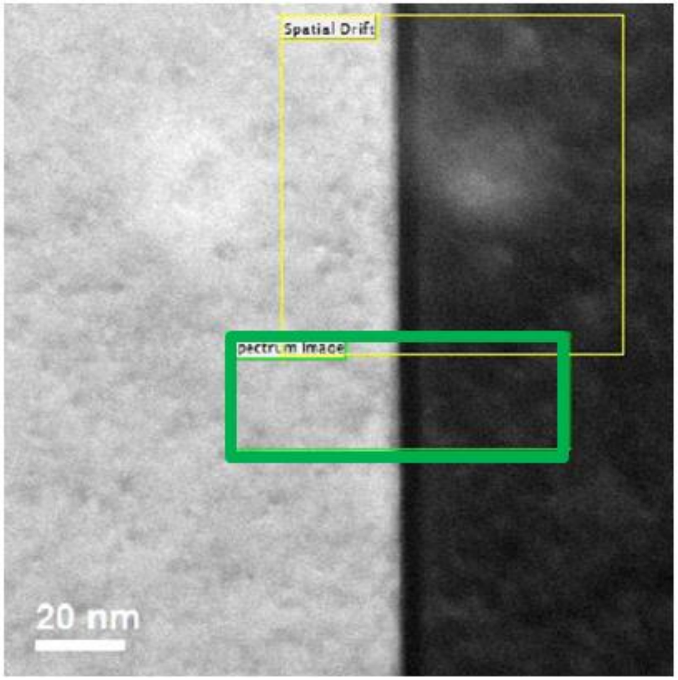


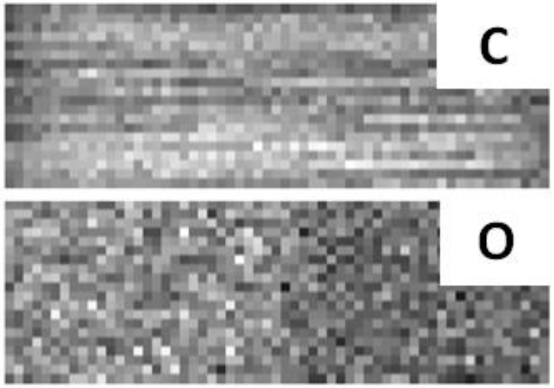
Bonding Interface Characterization: Chemical

EDXS



EDX measurement in the interface region (green rectangle) of a Si-Si wafer bond. Neither O nor C could be detected.





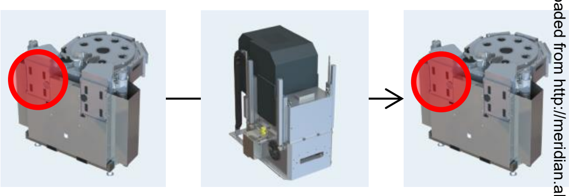
Process Results

GaAs – Si Wafer Bonding

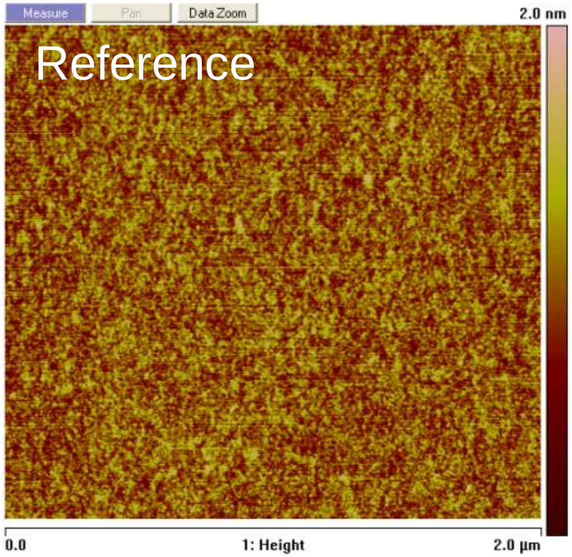
GaAs – Si Wafer Bonding

Pre-Bonding Surface Characterization: Topography

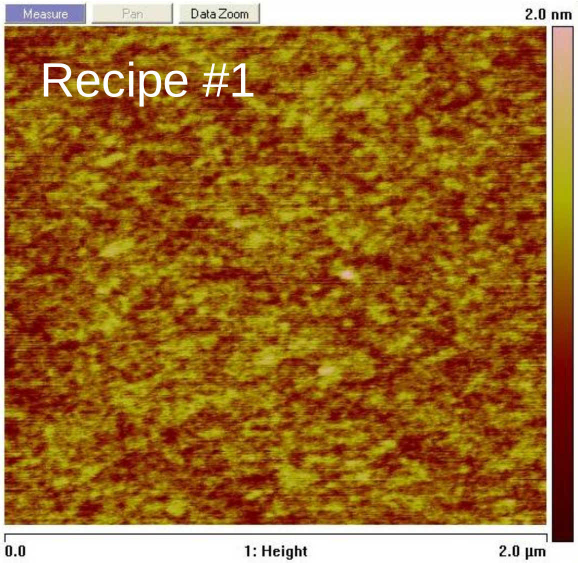
AFM Measurements



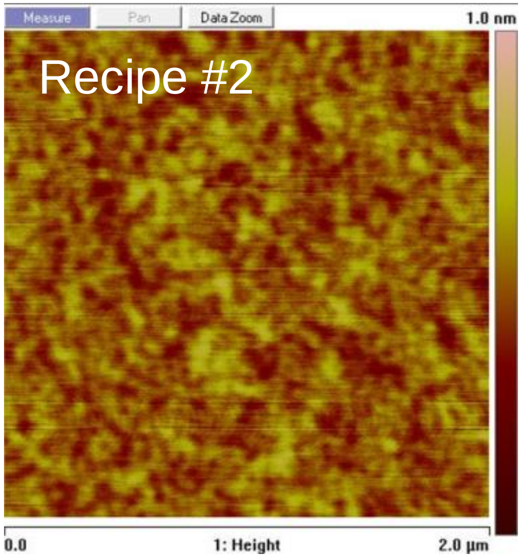
2 different surface activation recipes were considered. Both retained low microroughness profiles.



R_q = 0.237 nm



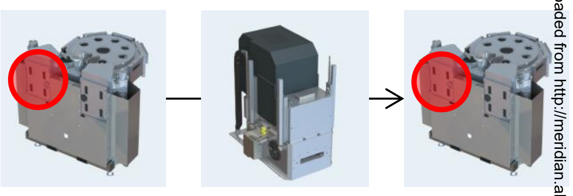
R_q = 0.199 nm



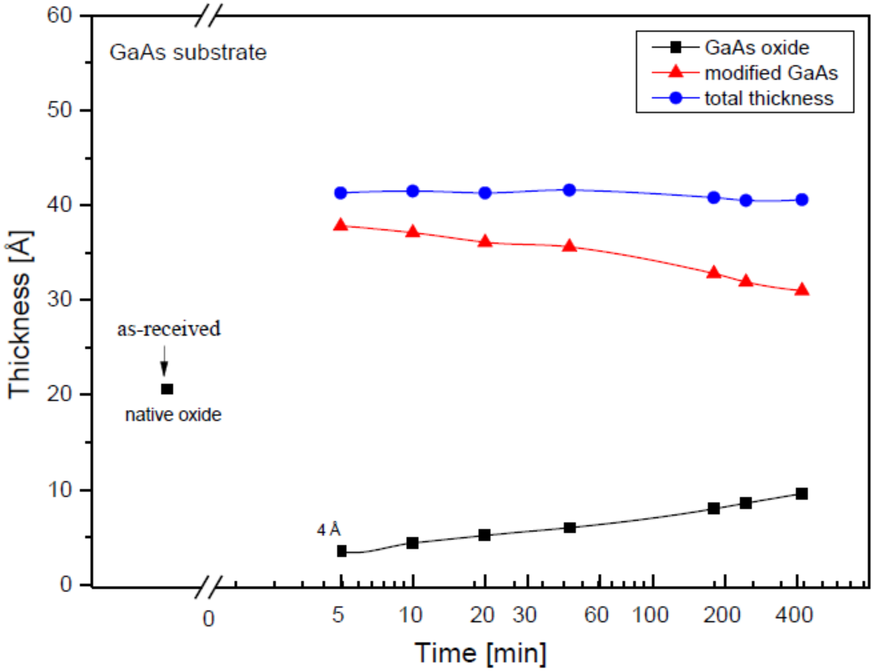
R_q = 0.093 nm

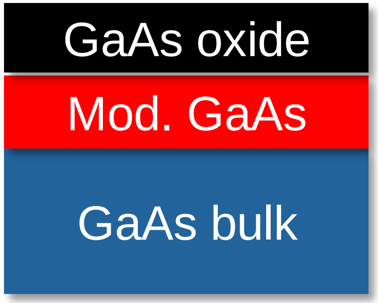
Pre-Bonding Surface Characterization: Chemical / Structural

Ellipsometry (ambient air)



Native oxide was reduced to < 4Å.

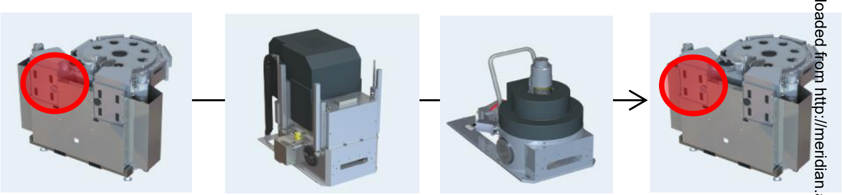




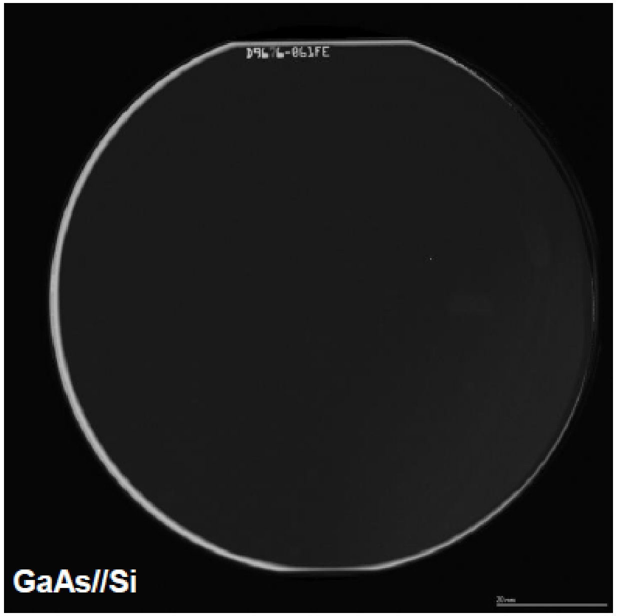
GaAs – Si Wafer Bonding

Bonding Interface Characterization: Uniformity

C-SAM / Maszara Test



High quality bond interface

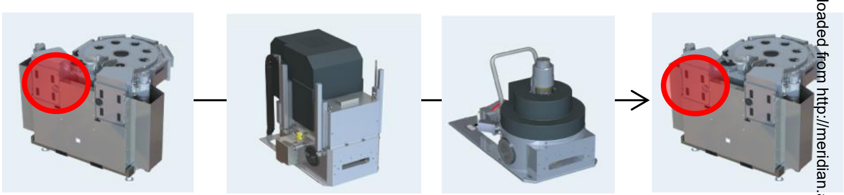


RT

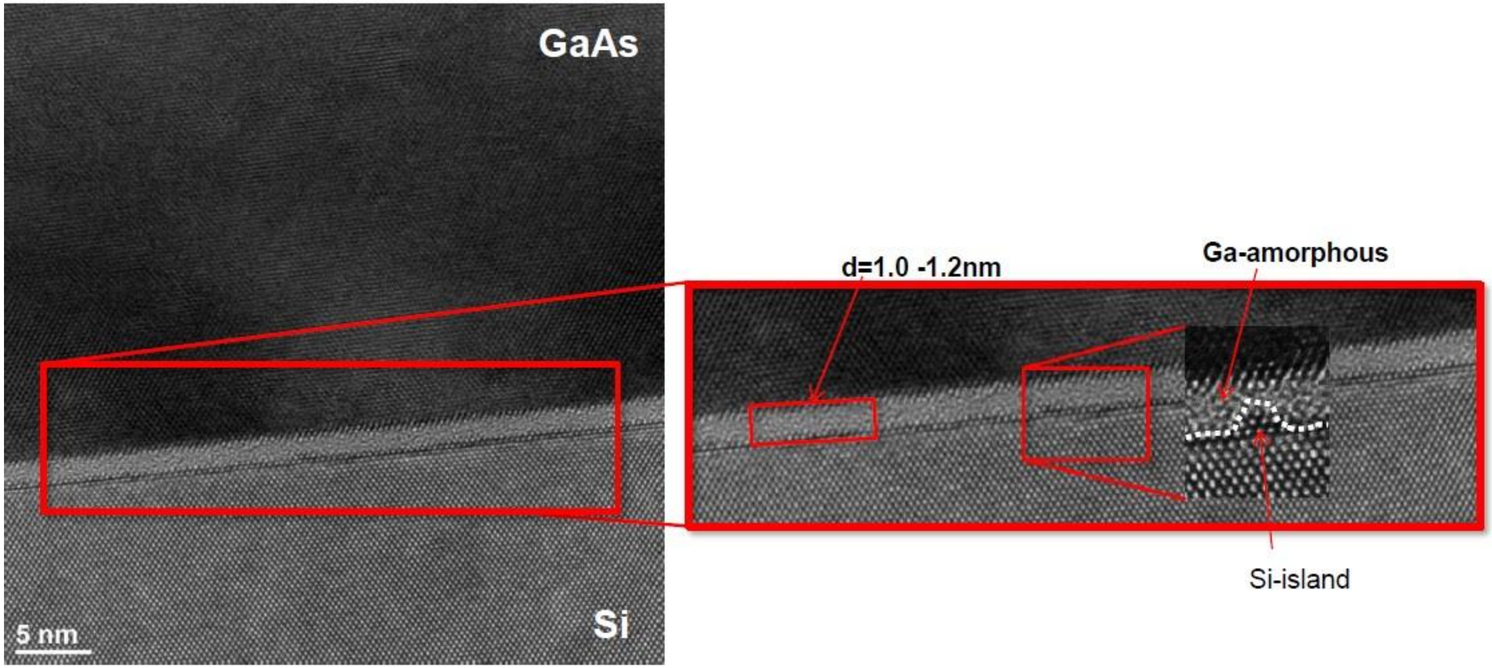
Maximum bond strength

Bonding Interface Characterization: Structural

HR-TEM

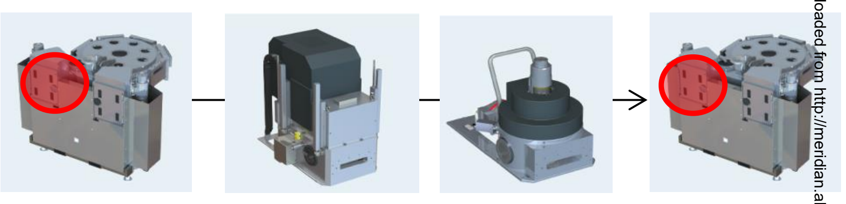


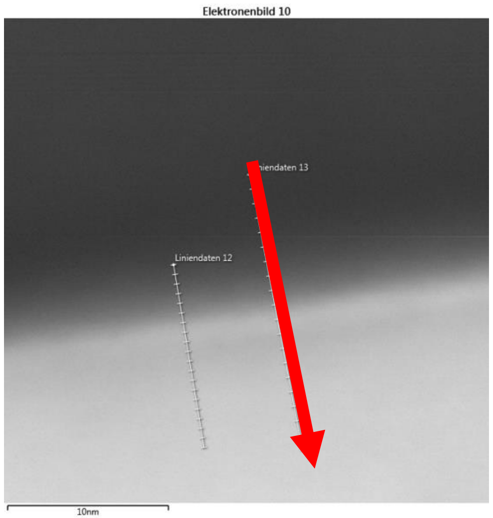
Very thin amorphous layer with d ≈ 1.2 nm

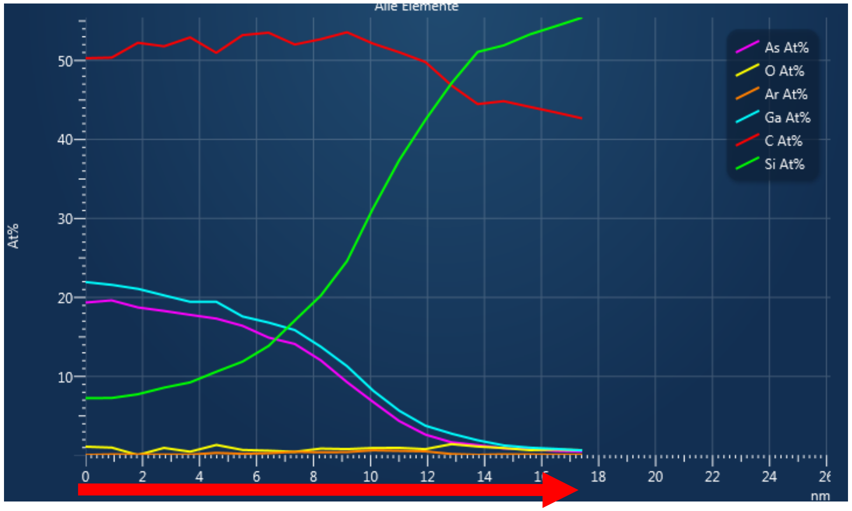


Bonding Interface Characterization: Chemical

EDXS







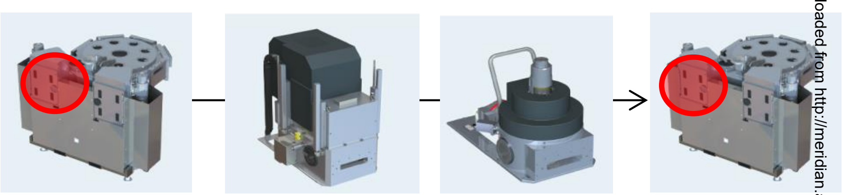
EDXS spectrum across the GaAs-Si bond interface.

O and C signals are residuals of SEM sample preparation.

No native oxide in the interface.

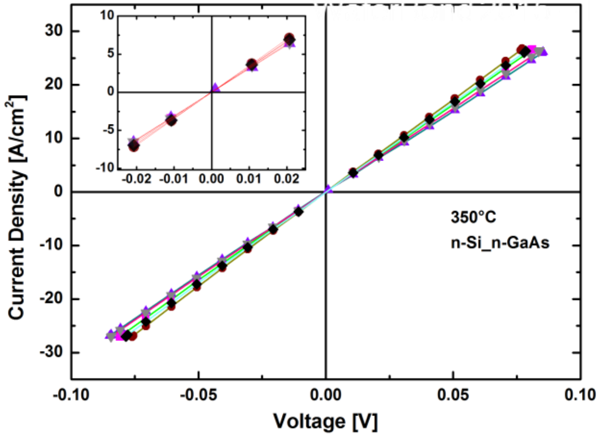
Bonding Interface Characterization: Electrical

I-V



In cooperation with Fraunhofer ISE

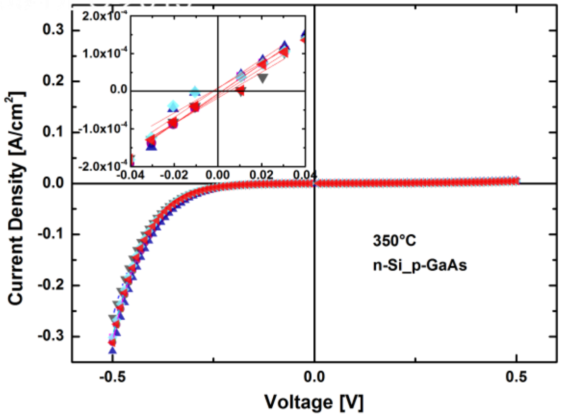
Si(n)-GaAs(n) wafer bond



→ 3 mΩ.cm^2 (mean) after RTA at 350°C

Suitable for concentrator PV

Si(n)-GaAs(p) wafer bond



→ Diode behaviour without tunneling

Process Results

GaAs – InP Wafer Bonding

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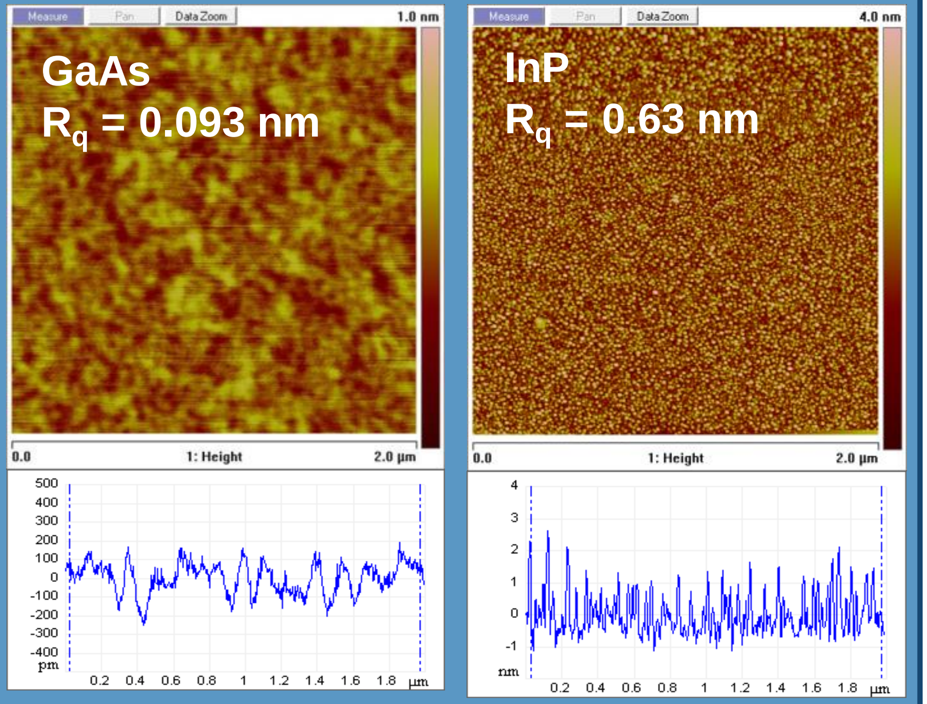
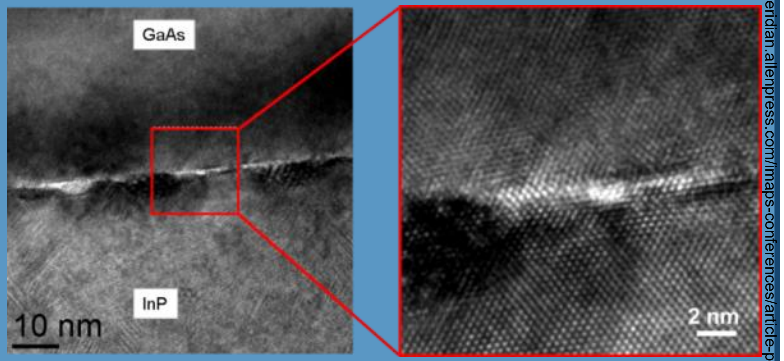
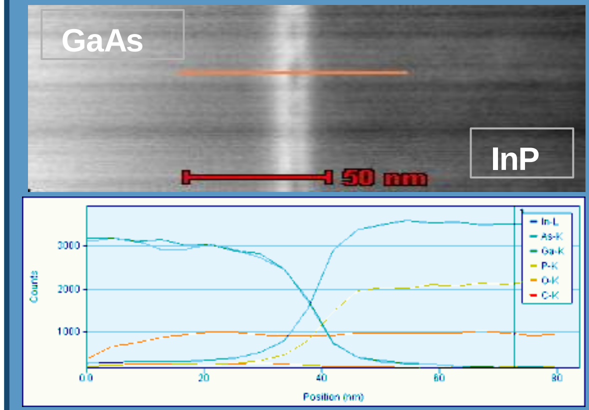
AFM Measurements



TEM Measurements



EDX Measurements

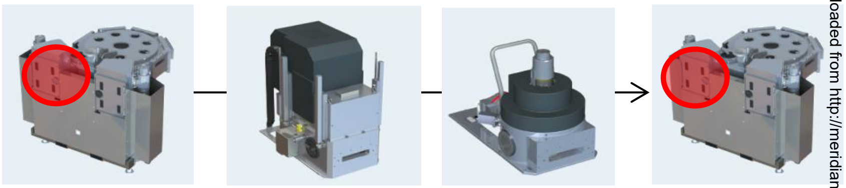


Process Results

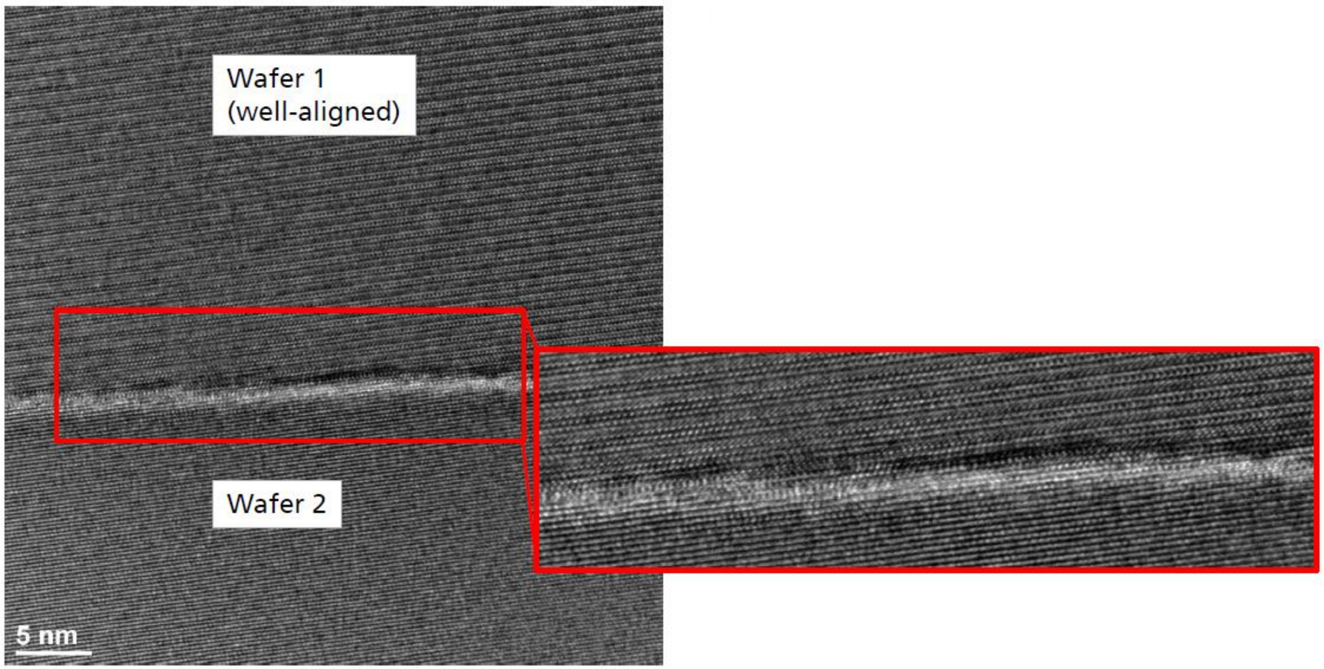
SiC – SiC Wafer Bonding

Bonding Interface Characterization: Structural

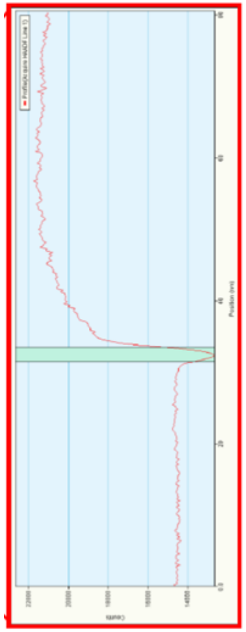
HR-TEM



Very thin amorphous layer with d < 2 nm



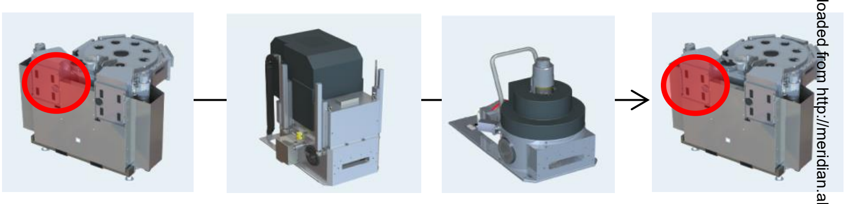
$d \approx (1{,}8\text{-}2{,}0)$ nm



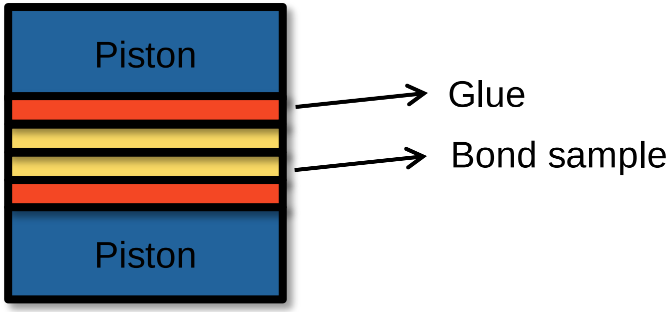
GaAs – InP Wafer Bonding

Bonding Interface Characterization: Structural

Pull Test



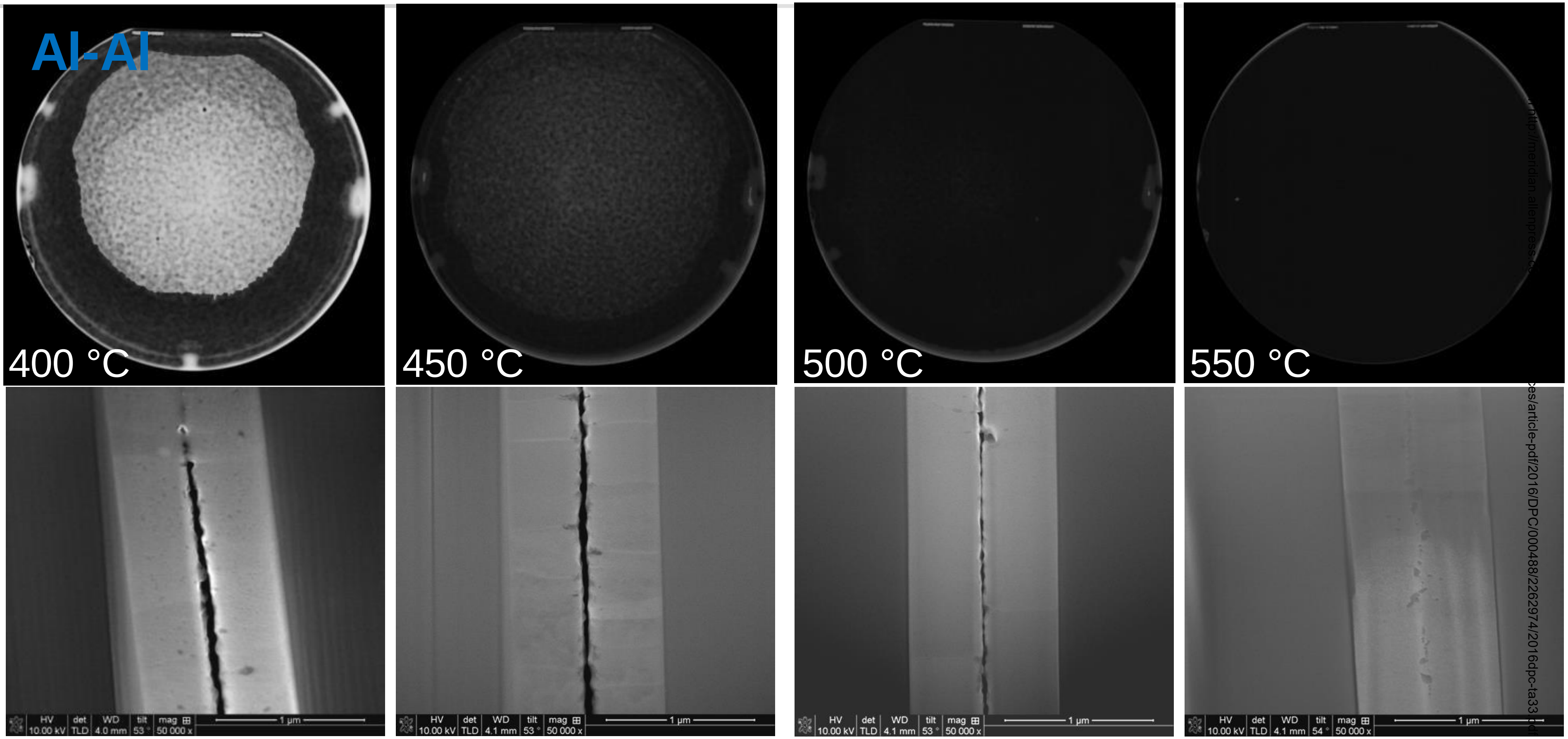
- Pull tests were performed on 16x16 mm² samples after thermal annealing.
- Tensile strength for all tested samples was **20 Mpa** (upper limit of measurment range)



Process Results

Al-Al Wafer Bonding

Al-Al Wafer Bonding



Top row: SAM image   Bottom row: SEM image

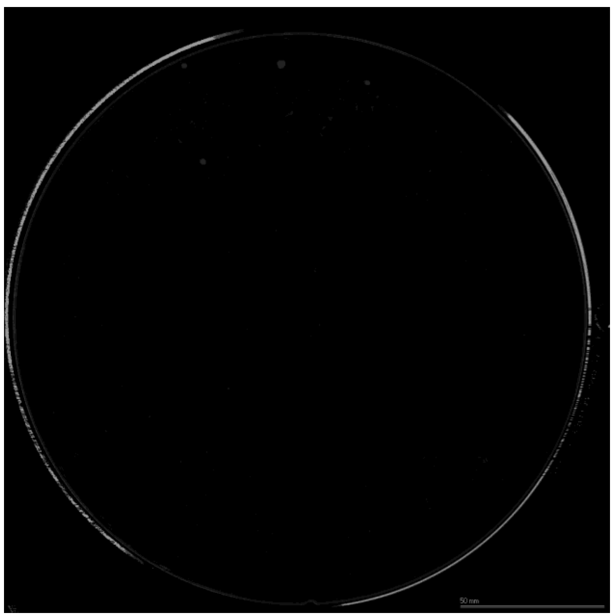
Left to Right: increasing temperature 400 °C – 550 °C, Δ = 50 °C, 60 kN

→ decreasing SAM signal with increasing bond temperature

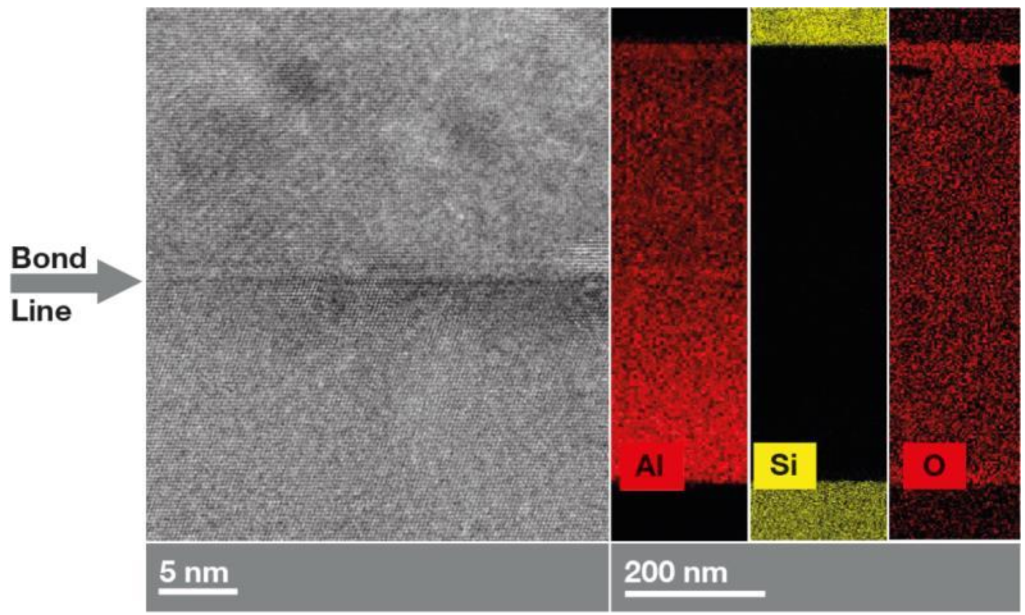
→ increasing bond interface quality with rising bond temperature

Al-Al Wafer Bonding

- Customer C
  - 200 mm; full-sheet
  - T = 150 °C
  - t = 1 hour
  - F = 60 kN



High bonding strength



No O_2 concentration difference between the bulk and the interface

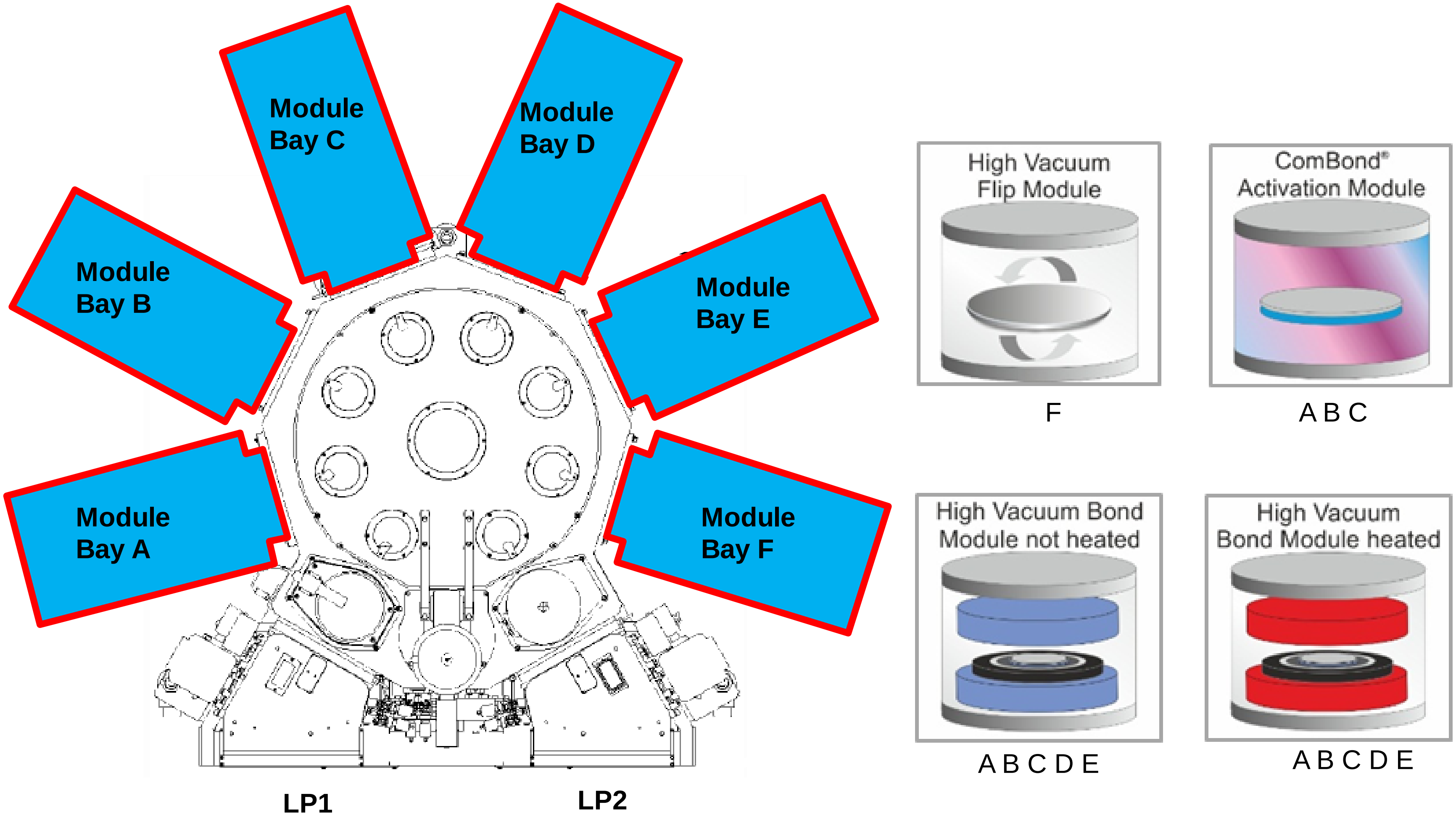
Advances in Aligned Wafer Bonding Enabled by High Vacuum Processing

Process Equipment

Process Equipment

IMAPS 12th International Conference and Exhibition on Device Packaging

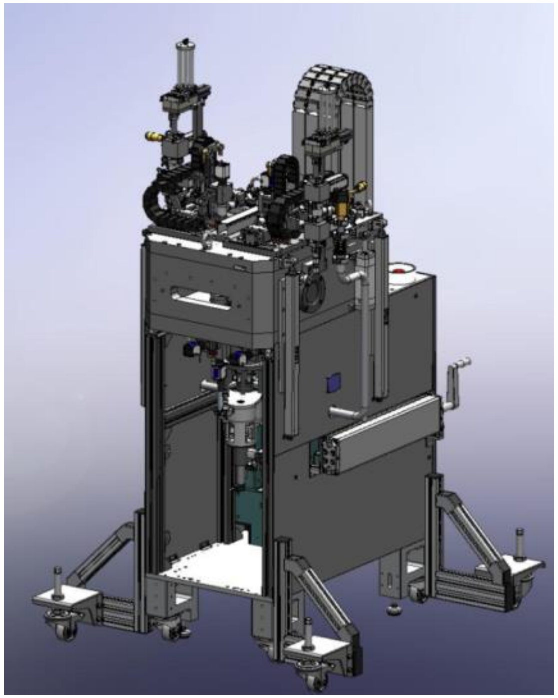
Process Equipment



Process Equipment

- VAM (Vacuum Alignment Module
- Electrostatic chucks
- Face to face (F2F) and front to back (F2B) alignment
- Force up to 10 kN
- Enhanced vacuum level of < 9 x 10^{-8} mbar
- Clamp mechanism to fix aligned wafer pair
- Process chamber bake out function

Vacuum Align Module VAM	Technical Data
F2F alignment F2B alignment	< 1 µm < 1 µm
Piston force	Up to 10 kN
Throughput	12 wph
Wafer Substrate	150 mm - 200 mm F2B 150 mm - 200 mm F2F
Wafer stack height	< 10 mm



Advances in Aligned Wafer Bonding Enabled by High Vacuum Processing

Summary & Conclusions

Summary & Conclusions

- High vacuum wafer bonding with all processing and handling done in vacuum environment can have the following advantages
  - Vacuum encapsulation
    - High vacuum level
    - Different preprocessing for top and bottom wafer
  - Covalent bonding
    - Room to low temperature bonding thereby enabling bonding of materials with CTE mismatch
    - Oxide free interface
    - Minimized amorphous zone

Orcas in a line – Resurrection Bay, Alaska

Thank you!

Questions?

Eric F. Pabo – Business Development Manager MEMS

EVG®580 High Vacuum and ComBond® Overview

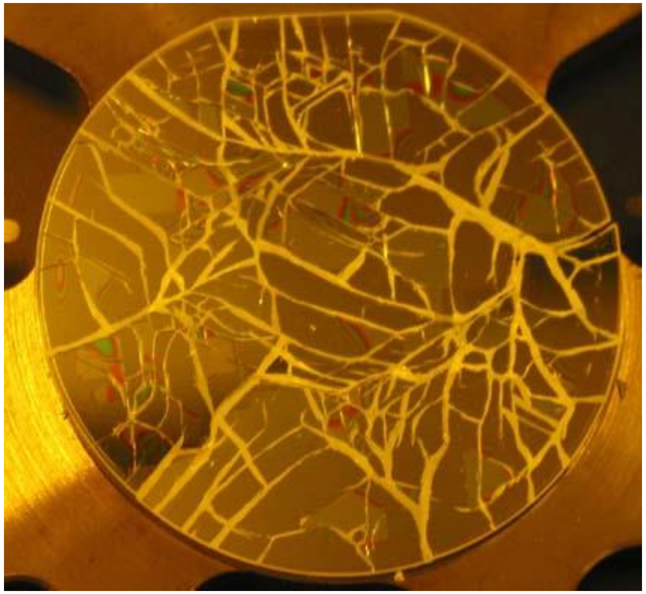
	Current Bonding Systems (e.g. Gemini®)	EVG®580 ComBond®
Vacuum specification	~5 x 10^{-6} mbar (in the bond chamber)	~1.3 x 10^{-7} mbar
Time for base pressure evacuation	95 minutes	5 minutes
Handling between process modules	Ambient pressure	Under Vacuum (~1.3 x10^{-7} mbar)
Pressure sequence on process modules	Ambient pressure – vacuum – ambient pressure	Constant vacuum level

EVG®580 High Vacuum and ComBond® Overview

- Wafers enter and exit EVG®580 through a load lock system
  - System is kept pumped down at all times except during maintenance resulting in a lower base vacuum
  - Substrates are kept under vacuum at all times inside of the EVG®580

Si/$LiNbO_3$

- Cleaning
- Annealing: 200°C/1 hour



- Cleaning
- Plasma activation (O_2)
- Temperature: 100°C/2 hours