Modeling and Design of High Temperature Silicon Carbide DMOSFET Based Medium Power DC-DC Converter

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Abstract:

Silicon Carbide (SiC) is a promising new material for high power high temperature electronics applications. SiC Schottky diodes are already finding wide acceptance in designing high efficiency power electronic systems. We present TCAD and Verilog-A based modeling of SiC DMOSFET, and the design and analysis of a medium power DC-DC converter designed using SiC power DMOSFETs and SiC Schottky diodes. The system is designed as a 300W boost converter with a 12V input and 24V/36V outputs. The SiC power converter is compared to another designed with commercially available Silicon power devices to evaluate power dissipation in the DMOSFETs, transient response of the system and its conversion efficiency. SiC DMOSFETs are characterized at high temperature by developing temperature dependent TCAD and Verilog-A models for the device. Detailed TCAD modeling allows probing inside the device for understanding the physical processes of transport, whereas Verilog-A modeling allows us to define the complex relationship of interface traps and surface physics that is typical to SiC DMOSFETs in a compact analytical format that is suitable for inclusion in commercially available circuit simulators.

Keywords: TCAD, Verilog-A, SiC DMOSFET, DC-DC converter

I. Introduction:

Design of efficient Silicon Carbide based power systems requires a thorough knowledge of the physics of operation of SiC power devices, their thermal behavior, and calibrated compact models that can be included in industry standard simulation tools such as SPICE and MATLAB Simulink. Unique aspects of 4H-SiC based devices such as interface trap states, incomplete ionization, transition region, surface roughness and Coulomb scattering mobility need to be understood and incorporated in the device models to carry out accurate modeling and simulation. In this paper address some aspects of modeling and simulation of SiC devices and circuits using a multi-tiered approach. We first link experiment to physics based TCAD models. We then use those models to create behavioral models for SiC devices. Finally these models are used in circuit and system simulations.

In Section II, we briefly discuss the physics of the operation of SiC devices by demonstrating a custom 2D drift-diffusion based TCAD simulator for SiC MOS devices. We then describe a fast and accurate thermal modeling method that can be used to create temperature maps for SiC devices, packages and modules in Section III. Section IV discusses the behavioral Verilog-A models for DC and transient operation of SiC DMOSFETs. We demonstrate a 300W SiC DMOSFET based DC-DC converter and its advantages over a Silicon DMOSFET based converter in Section V. Finally the conclusions from this work are presented in Section VI.

II. SiC DMOSFET TCAD Modeling:

Drift-diffusion based distributed device modeling can provide significant insights into the operation of Silicon Carbide power devices. We have further developed distributed device

models that take into account the complex physical characteristics of SiC DMOSFETs. The device models mainly deal with the physics of the interface traps, the channel mobility and the off-state breakdown characteristics of these devices [1, 2, 3].

$$\vec{\nabla}\cdot\left(\varepsilon\,\vec{\nabla}\phi\right)=-q\left(-n+p+N_D^+-N_A^-\right) \quad (1)$$

$$\frac{\partial n}{\partial t}=\frac{1}{q}\vec{\nabla}\cdot\vec{J}_n-R_n+G_n \quad (2)$$

$$\frac{\partial p}{\partial t}=-\frac{1}{q}\vec{\nabla}\cdot\vec{J}_p-R_p+G_p \quad (3)$$

$$\vec{J}_n=-qn\mu_n\vec{\nabla}\phi+qD_n\vec{\nabla}n \quad (4)$$

$$\vec{J}_p=-qp\mu_p\vec{\nabla}\phi-qD_p\vec{\nabla}p \quad (5)$$

Drift-diffusion based device modeling involves solving the coupled differential equations comprising of the Poisson equation, and electron and hole current continuity equations in conjunction with the electron anqd hole current equations. These equations (Eq. (1) to Eq. (5)) are solved for a DMOSFET for steady state and time-dependent operations. We also incorporate the physics of carrier scattering and charge transport inside the device to capture the exact behavior of the semiconductor device. The physics of electron/hole scattering is incorporated as part of the mobility model. The mobility model for SiC devices includes the bulk phonon scattering, ionized impurity scattering, surface phonon scattering, surface roughness scattering, Coulomb scattering from interface traps, and the scattering in the transition layer.

a) Mobility: The main scattering mechanisms in a 4H-SiC MOSFET channel are the Coulomb scattering from interface trapped charge, surface roughness scattering and the mobility degradation due to the Si-C-O transition layer [1, 2, 3, 4].

b) Interface traps: Traps at the SiC-SiO_2 interface in SiC MOS structures cause significant reduction in the channel current by reducing the total mobile charge concentration [1, 2]. Interface traps not only cause the surface mobilities and mobile charge concentration to reduce, they also lead to higher sub-threshold slopes. Figure 1 shows the extracted interface trap density of states profile for a 20A 4H-SiC DMOSFET.

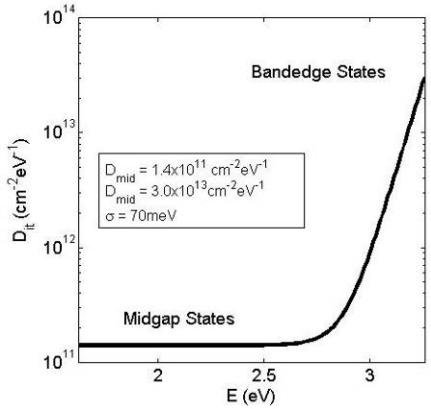

Fig. 1. Extracted interface trap density of states for a 20A 1200V 4H-SiC DMOSFET.

c) Impact ionization: Impact ionization caused by high energy electrons and holes at large electric fields leads to breakdown of the SiC DMOSFETs. Several models that relate the rate of impact ionization to the electric field and/or electron/hole energies exist in the literature [5, 6]. We have employed these models to simulate the breakdown characteristics of 1200V SiC DMOSFETs.

d) Device Modeling Findings: We have modeled the physics of a 20A 1200V SiC DMOSFET using an in-house drift-diffusion device simulator. The source and drain of the DMOSFET are doped to the $10^{20}cm^{-3}$ levels whereas the drift region is doped to the mid $10^{15}cm^{-3}$ levels. The oxide thickness of the DMOSFET is approximately 70nm.

Figure 2 shows the I_D-V_G characteristics of the DMOSFET. The sub-threshold slope for this device is 285mV/decade at 150^oC which is an indication of the presence of large number of interface traps. This can significantly affect the turn-on and switching losses of the SiC DMOSFET.

Figure 3 shows the simulated breakdown characteristics of the device. Our simulations indicated that the impact ionization has a very strong dependence on electric field in the device. The impact ionization is initiated close to the p-well drift region boundary where the electric field intensity is the highest. For the device under test, breakdown voltage was evaluated to be approximately 1600V. Further, the SiC DMOSFET exhibited excellent leakage characteristics until breakdown. This simulation indicated that these SiC DMOSFETs would

serve very well for operation at bus voltages of 300V which are present in hybrid electric vehicles.

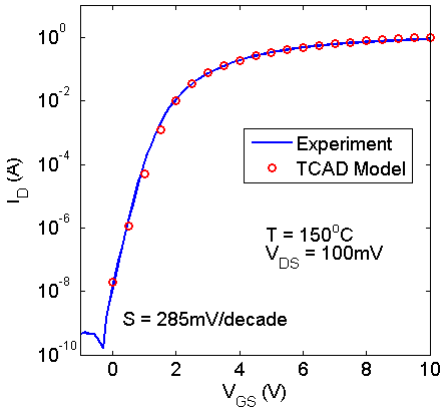

Fig. 2: I_D-V_G characteristics of a 20A SiC DMOSFET operating at 150°C. The subthreshold slope is 285mV/decade due to the large number of interface traps.

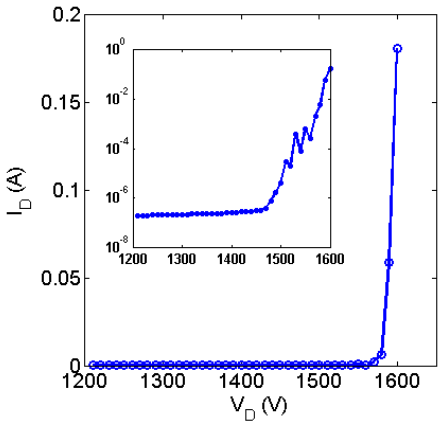

Fig. 3: Simulated breakdown characteristics at gate bias of 0V of the SiC DMOSFET under test.

e) SiC Mixed Mode TCAD Modeling: The DMOSFET in a DC-DC converter circuit has an inductive load. Modeling the switching behavior of the DMOSFET under this inductive load is essential to understand the limitations imposed on switching frequency, interface trap dynamics, reverse recovery, etc. We carried out mixed-mode simulation of a 4H-SiC DMOSFET operating as a switch with inductive and resistive loads with a goal to eventually building a complete 4H-SiC DMOSFET mixed-mode simulator for investigating complex power converter circuits. Mixed-mode simulation of this circuit involves solving Kirchoff's laws along with the semiconductor Drift-Diffusion equations self-consistently. Details of this work have been published elsewhere [7].

III. SiC Thermal Modeling:

A detailed consideration of the coupled thermal-electrical effects at power chip and module levels is crucial for the performance prediction of power devices as well as systems. For medium and high power applications, this can be equivalent to tens to hundreds of Watts contributing to Joule heating, effectively turning the power module into a heater unit, and therefore resulting in appreciable temperature rise in critical components. This temperature increase also adversely affects the overall electrical performance. The temperature rise in power devices and circuits can also lead to a catastrophic failure once a critical temperature is reached beyond which the negative feedback between the electrical and thermal dynamics turns into a positive feedback, causing a thermal runaway and irreversible damage to power module components.

To determine self-heating at the chip and power module levels, we have developed detailed distributed thermal simulators that are based on differential and lumped versions of the heat-flow equation, respectively written below.

$$C\frac{\partial T}{\partial t} = \nabla\cdot\left(\kappa\nabla T\right) + H \qquad (6)$$

$$C^{th}_{i,j,k}\frac{\left(T^{t}_{i,j,k} - T^{t-1}_{i,j,k}\right)}{\Delta t} + \frac{\left(T^{t}_{i,j,k} - T^{t-1}_{i\pm1,j,k}\right)}{R^{th}_{i\pm\frac{1}{2},j,k}} + \frac{\left(T^{t}_{i,j,k} - T^{t-1}_{i,j\pm1,k}\right)}{R^{th}_{i,j\pm\frac{1}{2},k}} + \frac{\left(T^{t}_{i,j,k} - T^{t-1}_{i,j,k\pm1}\right)}{R^{th}_{i,j,k\pm\frac{1}{2}}} = H^{t}_{i,j,k}\left(T^{t-1}_{i,j,k}\right) \qquad (7)$$

Here i, j and k represent x, y and z directions; C is the heat capacity; κ is the thermal diffusion constant; T is the temperature; H represents the heat generated; C^{th} and R^{th} are the thermal capacitance and resistance; lastly, t is time. At the DMOSFET's unit cell level, we solve the differential heat-flow equation, and couple it to semiconductor performance equations. At the entire chip level, we use the lumped thermal network to solve for the temperature variations on the chip surface. Finally, at the package and module levels, we

combine the thermal network that is used to describe the power device with those used for the package and power module. At each level, we provide a feedback to the electrical performance of the power devices, and iterate between the electrical and thermal levels until a self-consistent solution is obtained. [8, 9]

a) Thermal Model Findings*:* Figure 4 shows the calculated temperature map for a power module that has 4 power devices, which operate in parallel to boost the current and power output. Each power device consumes an average power of 25 W, has an area of approximately 6 mm^2, and contains approximately 1600 unit cells. The power module is cooled by a liquid coolant at 100 ºC. As the coolant flows over the module, it slightly heats up, resulting in temperature variation along the flow direction.

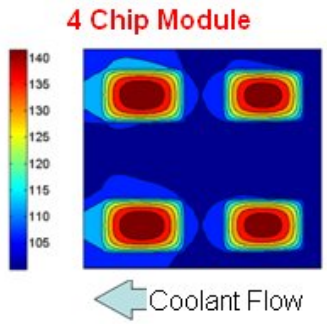

Fig. 4: Temperature map of a power module that includes 4 power devices. The power module is cooled using a liquid coolant that is at 100 ºC. The colorbar shows the temperature scale in ºC.

As an input to the thermal simulator, we calculated the heat generated by an individual power device using the device modeling described in Section II. The heat generated increases with temperature, peaks at approximately 150 ºC, and then starts rolling off as the temperature-dependent bulk mobility starts dominating the SiC DMOSFET performance. The temperature within a unit cell of the power device is effectively the intersection of the heat generated versus temperature line and the thermal load line whose slope is determined by the equivalent thermal resistance between that cell and the ambient.

Figure 5 shows the thermal maps as calculated for a 20A 1200V 4H-SiC DMOSFET packaged in a TO247 package attached to an aluminum heat sink. The power versus temperature characteristics was first calculated by carrying out mixed-mode simulation of a boost converter circuit. This information was then used to evaluate the heat generated inside the DMOSFET. A network of thermal resistors was then constructed using information about the thermal conductivity of the die, the package and the heat sink. The ambient temperature was assumed to be 100°C. The figure shows that using the aluminum heat-sink with multiple fins and the TO247 package, for the power dissipated in the DMOSFET during a DC-DC conversion, the maximum temperature is seen at the center of the die. Heat dissipates very quickly on the heat-sink and therefore we cannot see a large temperature gradient. The maximum temperature on the DMOSFET die was approximately 75°C higher than the ambient.

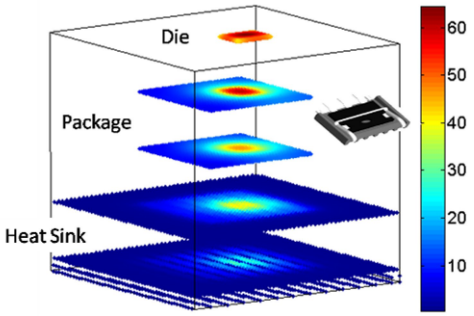

Fig. 5: Calculated temperature map of a 20A 4H-SiC DMOSFET in a TO247 package mounted on a heat-sink. The colorbar shows the temperature ***above*** the ambient. For the medium power switching application, the peak die temperature is approximately 75°C above the ambient.

IV. SiC DMOSFET Verilog-A Modeling:

While distributed device and mixed-signal modeling gives valuable insight in to the physics of the operation of SiC devices, this modeling technique is not entirely suitable for complex circuit simulation. We have therefore taken initial steps into transferring the physics of the SiC DMOSFET operation into a behavioral Verilog-A based analytical equations model. This behavioral description of the terminal characteristics of SiC DMOSFETs not only allows us to include device physics, but also

allows the calculation of heat and temperature of the DMOSFETs during circuit operation.

a) DC IV Model: We have initiated the development of physics based Verilog-A model for 4H-SiC DMOSFETs. Using the standard Verilog-A description of the industry standard BSIM3 equation set, we modified the threshold voltage, mobility and drain resistance models to account for the behavior of the SiC DMOSFET. The threshold voltage model is modified to include the effect of interface trap occupation as a function of gate voltage:

$$V_{th}(T) = V_{th}^{0}(T) + \frac{q}{Cox} N_{it}(V_G) \qquad (8)$$

Here $V_{th}^{0}(T)$ is the standard BSIM model for temperature dependent threshold voltage. As a simplified model, we have used the logarithm of the gate bias to represent the change in the surface potential, and thereby the changes in interface trap occupation, as a function of gate voltage.

$$N_{it}(V_G) = \mathrm{NIT0} + \mathrm{NIT1} \cdot \log(V_G) \qquad (9)$$

Further, the channel mobility has been modified to reflect the surface mobility in SiC MOS devices. Finally, the drift region of the DMOSFET is modeled using a fixed value for the drain resistance.

Figure 6 shows the simulated room temperature J_D-V_D curve using the compact Verilog-A model for a 20A SiC DMOSFET and its comparison to experiment. (The current is scaled by the width of the device.) Excellent match to experiment in the linear region of operation has been achieved with the simplified

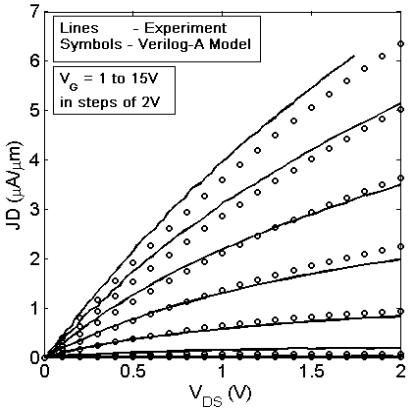

Fig. 6: Measured and Verilog-A simulated J_D-V_D curves for a 20A 4H-SiC DMOSFET at 27°C.

trap occupation and mobility models described above. Further, Fig. 7 shows the I_D-V_D characteristics of the device at 150°C. The measured and simulated curves match reasonably well, thereby validating the model.

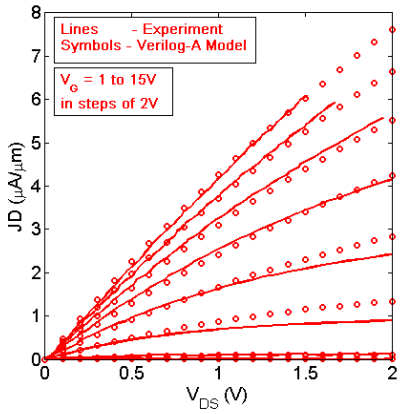

Fig. 7: Measured and Verilog-A simulated J_D-V_D curves for a 20A 4H-SiC DMOSFET at 150°C.

b) Gate-Drain Capacitance Model: In order to build a complete model to account for transient behavior of 4H-SiC DMOSFETs, it is essential to characterize the different capacitances in the device. During switching, the JFET and drift regions of the DMOSFET undergo a rapid transition from neutral to depletion. This gives rise to a gate-drain capacitance that changes with drain bias. Typically this capacitance is modeled using the "Switch Capacitor" model [10, 11]. Using drift-diffusion simulation, this drain bias dependent gate-drain capacitance (C_{GD}) can be extracted. In the quasi-static case, this capacitance can be approximated by calculating the change in total charge in the entire drain region (JFET+drift+drain) when a small change in the gate bias is applied. Keeping the drain voltage at different levels during this calculation gives the bias dependent gate-drain capacitance.

Further, for accurate transient simulations using the behavioral Verilog-A model, this capacitance needs to be included in the Verilog-A model. Care must be given to ensure that there are no abrupt transitions in the C_{GD} versus V_{DS} curve to avoid convergence errors during transient simulation.

Figure 8 shows the gate-drain capacitance of the 20A 1200V 4H-SiC DMOSFET as extracted from 2D device

simulation, and the equivalent model as implemented in Verilog-A.

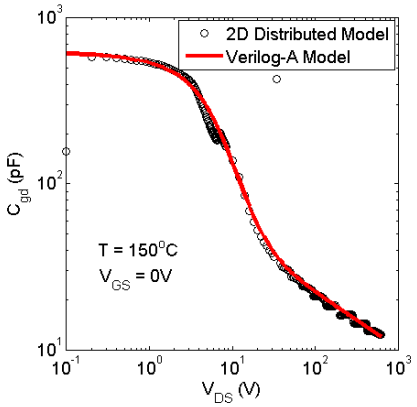

Fig. 8: Gate-drain capacitance of a 20A 1200V 4H-SiC DMOSFET as a function of drain bias modeled using 2D drift-diffusion and behavioral Verilog-A compact models.

c) Boost Converter Simulations: Using the complete Verilog-A model for the 20A 1200V 4H-SiC DMOSFET, transient simulations of a DC-DC boost converter have been carried out. The circuit comprises of the 20A 1200V 4H-SiC DMOSFET and commercial SiC Schottky diodes along with passive components. The load is a 5Ω resistance.

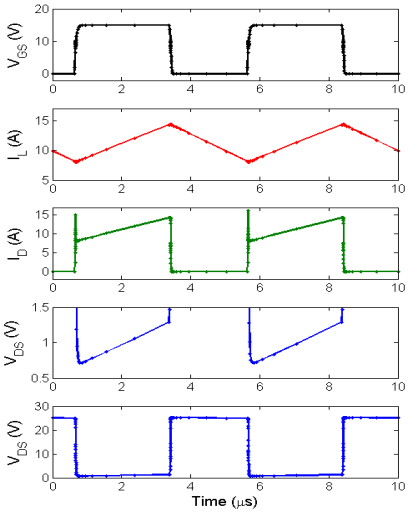

Fig. 9: Simulated 12V/24V SiC DMOSFET based boost converter using Verilog-A model for the DMOSFET.

Figure 9 shows the simulated waveforms for a 12V/24V boost converter simulation with a 4.7μH inductor and 5Ω load. The boost converter operates in the continuous conduction mode at 200 kHz. During the ON state of the DMOSFET, the inductor current (I_L) of 7.5A-15A flows through the DMOSFET (I_D). Correspondingly the drain voltage of the DMOSFET (V_{DS}) rises from approximately 0.75V to 1.3V. This causes a small amount of ON state conduction loss in the device. During the off state the DMOSFET blocks 24V with negligible leakage current. The maximum power dissipated during the switching cycle is during the turn-ON and turn-OFF periods.

Figure 10 shows the simulated waveforms for the power dissipated in the DMOSFET for various DC-DC conversions (12V/18V, 12V/24V and 12V/33V). The load is kept constant at 5Ω. The average power dissipated in the DMOSFET increases with output voltage as 8.62W at Vout=24V and 59.87W at Vout=33V. The large increase in dissipated power for the Vout=33V case is due to the excessive current (>20A) passing through the DMOSFET during this DC-DC conversion. The simulated energy required for switching the DMOSFET for the 12V/24V and 12V/33V conversions is 7.74μJ and 37.22μJ respectively. The power transfer efficiency was calculated to be approximately 93% for the 12V/24V conversion. This simulation does not consider the effects of package and other stray inductance on the operation of the circuit.

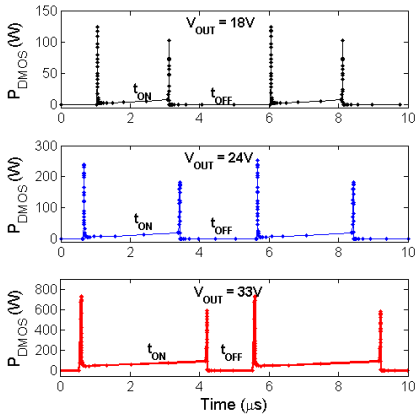

Fig. 10: Simulated power dissipation in the DC-DC converter circuit for different boost operations. Maximum power is dissipated during the turn-ON and turn-OFF parts of the switching cycle.

V. SiC DC-DC Converter:

A 300W DC-DC boost converter was designed and built using 4H-SiC DMOSFETs and Schottky diodes. Figure 11 shows the DC-DC converters designed using the 20A 1200V 4H-SiC DMOSFETs. The SiC DMOSFETs and SiC Schottky diodes were obtained from Cree Inc. Another converter was built using Si DMOSFETs and SiC Schottky diodes to compare the power conversion efficiencies.

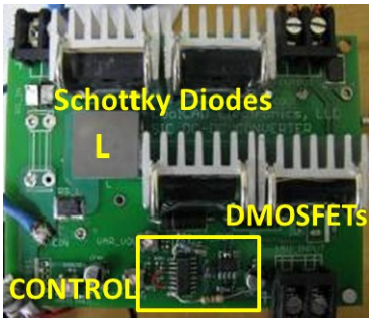

Fig. 11: Top view of a 300W SiC DMOSFET based DC-DC converter. The input and output capacitors are underneath the PCB.

The STP26NM60N 600V 20A Silicon DMOSFETs were used for building the Silicon DC-DC converter. Even though our voltage operating range was limited to 50V output voltage, the high voltage Silicon DMOSFETs were chosen to be close in breakdown voltage to the high voltage (1200V) SiC DMOSFET.

a) SiC DC-DC Converter Findings: The DC and transient characteristics of the DC-DC converters were measured in order to quantify the performance of the power DMOSFETs. The input and output capacitors are chosen to be 1500μF, while the inductor is a 4.7μH inductor with a rated saturation current of 40A. The input voltage to the power converter is through a 12V 1200W power supply. The output voltage can be regulated using a feedback mechanism between 15V and 40V. The test results shown next are for load resistances from 5Ω to 10Ω.

Figure 12 shows the power conversion efficiency of the two power converters – one with Silicon DMOSFETs and other with SiC DMOSFETs, as a function of the output power. The SiC power converter outperforms the Silicon power converter for all the output power levels. This is in spite of the fact that the SiC DMOSFETs used are rated at twice the blocking voltage of the Silicon DMOSFETs. This clearly suggests the strength and effectiveness of SiC technology versus Silicon for power electronics applications.

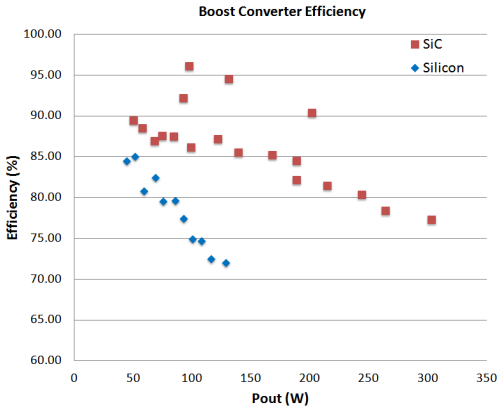

Fig. 12. Measured efficiency of the Si and SiC boost converters vs. output power. SiC boost converter works significantly better than its Silicon counterpart, even though the voltage rating of the SiC DMOSFET is twice that of the Silicon device.

Figure 13 shows the switching characteristics of the DC-DC converter during a 12V/24V conversion. There is some oscillation during the turn-off of the DMOSFET caused due to stray inductances.

Figure 14 shows the turn-off behavior of the SiC DMOSFETs during the DC-DC conversion. The turn-off of the device gives rise to significant oscillations due to the parasitic inductances that exist in the path of the

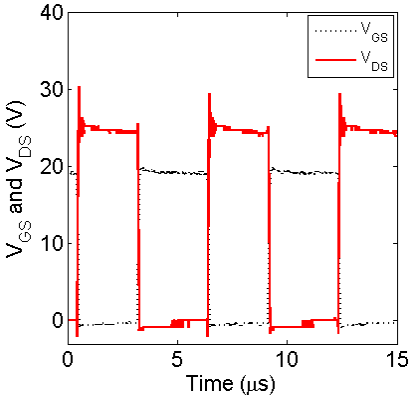

Fig. 13: Measured V_{GS} and V_{DS} of the 20A 1200V SiC DMOSFETs while working as a 12V to 24V DC-DC converter.

DMOSFET drain current. These inductances are due to the bond wires, package leads, solder joints, and the PCB traces. We have tried to minimize this inductance by using wide and short PCB traces on the drain nodes of the DMOSFETs. These oscillations on the drain of the DMOSFETs cause the highest power dissipation in the DMOSFETs, and thereby significantly reduce the efficiency of the system.

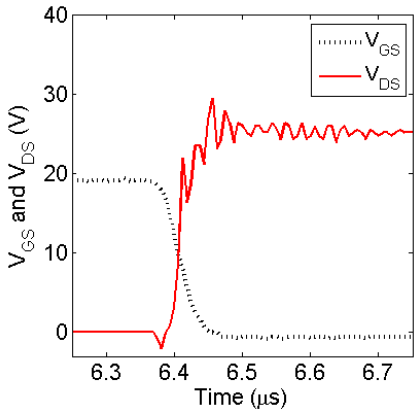

Fig. 14: Measured turn off of the SiC DMOSFETs. Oscillations at the drain terminal are a result of the stray inductances.

VI. Conclusion:

Modeling, simulation and design methodologies for Silicon Carbide DMOSFET based DC-DC converter are presented. Physics based TCAD modeling has shown that the interface traps and surface roughness limit the operation of SiC DMOSFETs. Further, fast thermal calculations for the DMOSFET die, package and power module has suggested that the rise in temperature at the die during DC-DC convertor operation is significant and can affect performance of the system. Verilog-A behavioral language has been used to incorporate the detailed physics of transport in 4H-SiC DMOSFETs into a format suitable for circuit and system simulation. The use of Verilog-A models has given good agreement with DC IV characteristics of the device, and has also enabled simulation of the transient behavior of the DMOSFET in a DC-DC converter application. Finally, a 300W SiC DMOSFET based DC-DC converter has been built and compared to another Silicon DMOSFET based one. The SiC DMOSFET based converter has shown higher conversion efficiency and lower switching losses at all power levels.

Acknowledgement

This work was supported in part by the National Science Foundation under SBIR Award #0912683.

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