Reliability Assessment of Passives for 300C using HALT

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Abstract

Highly accelerated life testing (HALT) is used to quickly assess the reliability of passive components for geothermal applications operating at 300°C ambient temperature. The HALT methodology uses combined stresses to accelerate the failure of capacitors and resistors. This paper describes the test methodology, special fixture designed, and results on capacitors and resistors. Life models for the components are presented. A process to modify component terminations is presented to make them appropriate for 300°C.

Keywords: High Temperature, Capacitor, Resistors

Introduction

The work reported in this document is part of a Department of Energy funded project to develop a sensor system for use in a geothermal well operating at 300°C. There are other needs for high temperature electronics in deep oil and gas drilling, well monitoring, instrumentation for jet engines and power generation equipment. Advances in SiC devices have enabled higher temperature electronics. Passive components to interconnect with the active devices are necessary for useful applications. Packaging and materials often limit passive components from high temperature applications. In addition, some high temperature components are limited by the availability of test fixtures to qualify them. This paper will present results on life testing of capacitors with two dielectrics and thick film resistors and the fixture developed to test them. This paper is not intended to be a comprehensive study of all capacitor and resistor types but does present results on promising components that would be useful in a high temperature circuit.

Capacitor technologies for high temperature

Capacitors are needed for filtering (0.1 uf) and timing (100pF) purposes. Capacitors come in a variety of dielectrics and packaging but few are suitable for 300°C applications. The parameters of interest include capacitance, temperature coefficient of capacitance (TCC), breakdown voltage, and DC losses (leakage resistance or insulation resistance). AC loss values are important at higher frequencies and are not the focus of this study. Table 1 lists temperature coefficient trends for three dielectrics showing potential for 300°C presented in Kirschman [1] by various sources. Surface mount ceramic Class I dielectric capacitors have low TCC and are the focus of this study.

Table 1 Property trends from RT to 300°C for capacitor dielectrics

Parameter of Interest	Ceramic (Class I)	Ceramic (Class II)	Glass
Capacitance	Low/med K	High K	Low K
TCC	+5%	-60 to 75%	+10%

Two dielectrics were selected for testing at 300°C: a SiSc based dielectric, and a calcium zirconate ($CaZrO_3$) dielectric. All samples are reated at 50V, the SiSc dielectric samples and the $CaZrO_3$ dielectic have a capacitance of 0.1 uF. All packaging is surface mount to be easily compatible with thick film substrate assembly. The SiSc dielectric is specified for operation at 300°C. High temperature performance and reliability is reported by Alberta [2] using HALT testing but no failures were reported. As

reported, there is a strong increase in capacitance from room temperature to 250°C followed by a decrease in capacitance. The packaging 0.1 uF is a 1209 case size and has a gold thick film termination, which makes it compatible with assembly processes for high temperature applications. The $CaZrO_3$ capacitors are a Class I, COG dielectric and have base metal electrodes (BME) composed of nickel with a copper end termination. The termination is plated with a nickel barrier layer and tin finish that needs to be replaced due to its temperature limitation. This capacitor dielectric has shown capability for 200°C applications [3].

Capacitor packaging and re-plating

Capacitor packaging can be a limitation for use at 300°C. Capacitor encapsulation and leads may limit reliable use at high temperature. Surface mount ceramic capacitors have high temperature potential but in most cases the termination material available has been a limit. Lead-free components are often supplied with silver palladium (AgPd) or tin plating over nickel terminations. The AgPd termination poses the risk of failure due to silver migration (accelerated by temperature) and tin plated leads are limited by the melting point of tin (232°C). AgPd migration may, possibly, be mitigated by encapsulation of the material, low voltage applications, or alloy with another element that can tie up the Ag. In order to facilitate testing of tin plated terminations, a process was established to prepare tin plated components for high temperature by chemically stripping the tin finish and re-plating with immersion gold. The immersion gold is intended to preserve the solderability of the nickel surface until soldering using a high temperature solder. Nickel will diffuse through the gold at the use temperature and form a limiting oxide.

The $CaZrO_3$ capacitors targeted for testing have a termination of tin over a nickel barrier layer.

Figure 1 shows the thickness of Sn is ~10um.

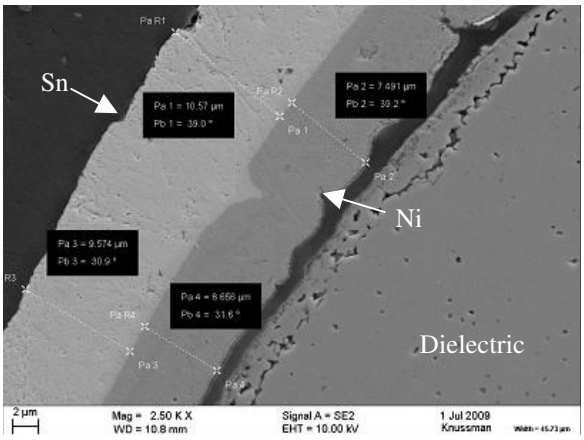


Figure 1 $CaZrO_3$ capacitor termination section.

Two tin stripper chemistries were tested: Brite Solder Stripper #3 (nitric acid, fluoroboric acid) and Magnum NPS-220 (nitric acid, sulfamic acid, fluoroboric acid). The gold finish was made using Shipley EL-221 immersion gold. Two groups of tests were carried out to understand the needed etching and plating times for the Solder Stripper #3 and immersion Au. The first test group had a fixed etch time of 90 seconds followed by 5min, 10 min and 30 min plating of immersion Au. The 90 seconds etching time was calculated from the etch rate provided by the specification sheet with a 50% margin.

Figure 2 shows a region in the cross-section of a sample after 90 seconds of stripping followed by 30 minutes of Au plating. An EDS analysis of three spots within the sample is shown in Figure 3. Spectrum 1 is taken in the immersion Au layer, spectrum 2 is the nickel-tin (Ni-Sn) intermetallic compound (IMC) layer that remains after stripping, and spectrum 3 is in the nickel barrier layer. Figure 4 shows an area of delamination between the immersion Au and Ni-Sn IMC layer.

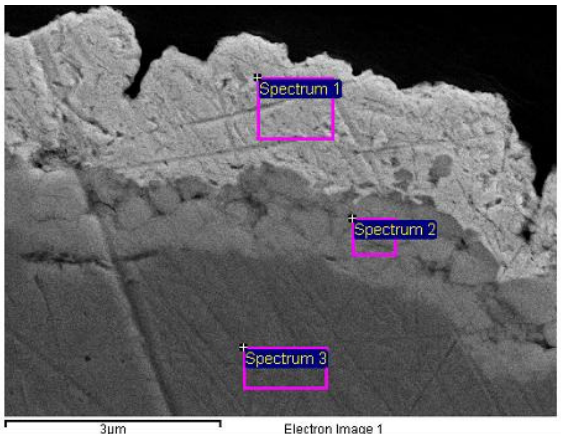


Figure 2 $CaZrO_3$ capacitor cross-section Region 1

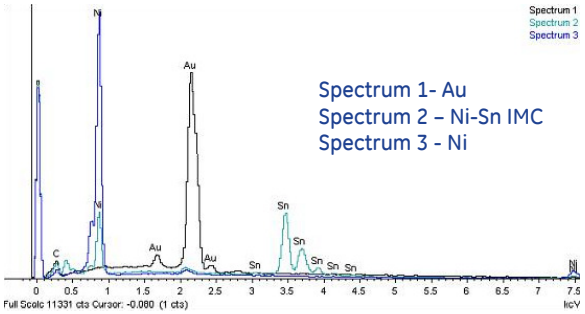


Figure 3 EDS of Region 1

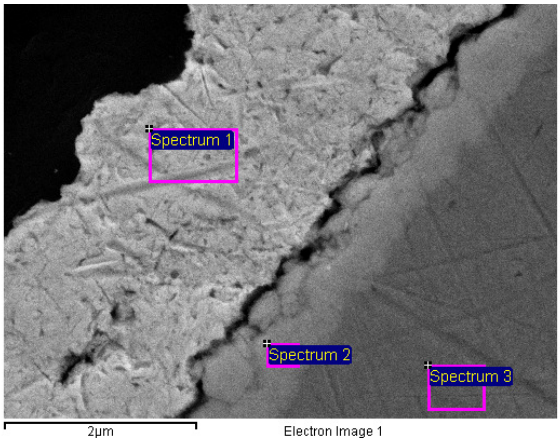


Figure 4 $CaZrO_3$ capacitor cross-section Region 2

A second group was run in order to determine an etch time needed to remove the Ni-Sn IMC layer. Test group 2 used the same solution (Brite Company Stripper #3) but varied the etch time from 1 minute to 8 minutes. The IMC thickness was measured in the range of 300-1000 nm regardless of the etch time as seen in Figure 5. The etchant was not able to reduce the IMC thickness any further.

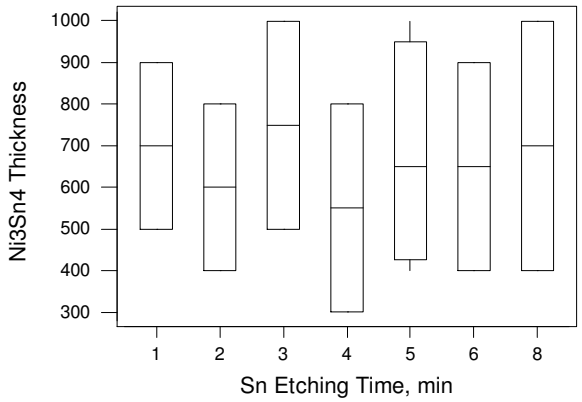


Figure 5 Group 2 Ni-Sn IMC thickness (nm) at varied Sn stripping times

Magnum NPS-220 solution was evaluated to etch the Sn finish and evaluate its capability to reduce the Ni-Sn IMC layer and improve the adhesion of electroless plated Au. Etching time from 2 minutes to 10 minutes was studied. At 2 minutes etch time under agitation, there is a uniform layer of Ni-Sn IMC remaining with a thickness of 200-500nm and apparent separation of immersion Au layer. At 5 minutes etch time, there are fewer regions where Ni-Sn is present and the immersion Au adhesion is improved. After 10 minutes etch time nearly the entire Ni-Sn IMC layer is removed and immersion Au adhesion is maintained. Figure 6 shows section views of the layers of interest.

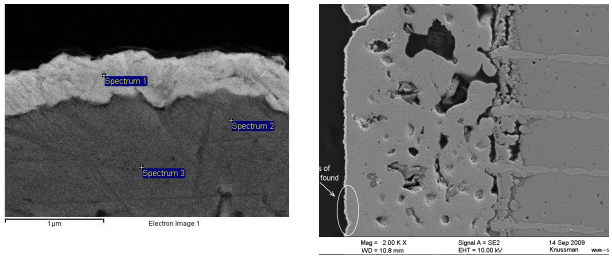


Figure 6 NPS220 Sn etching and adhesion of Au plating

Capacitor reliability testing

The acceleration model for capacitors takes the form of Equation 1[4], which has the Erlang form and where t is time, V is voltage, T is temperature (K), k is Boltzman's constant, n is the voltage exponent (typically around 3[5,6]), E_a is activation energy varies but typically around 1[6], and the subscripts refer to test conditions 1 and 2.

Equation 1

$$\frac{t_1}{t_2} = \left(\frac{V_2}{V_1}\right)^n \exp\frac{E_a}{k}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)$$

An understanding of Ea provides information on the failure mechanisms and reliability at other temperatures. Equation 1 shows that time acceleration may be achieved by voltage and temperature. Acceleration by voltage and temperature has material limits that may change the failure mode. An assumption made in acceleration models is that the failure modes are constant. This assumption is detected by constant distribution shape parameters or slope of the distribution.

Reliability characterization of capacitors using Highly Accelerated Life Testing (HALT) has been performed at conventional temperatures. Paulsen [5]

tested 50V rated 0.1 uF Kemet ceramic capacitors at voltages of 250V, 325V, 400V, 500V, and 600V and temperatures of 155C, 165C, and 175C. The failure distributions shared a common slope. Confer [6] tested 50V rate 0.1 uF 1206 Murata Erie ceramic capacitors at 8 times rated voltage, 400V and at 125, 135, 140, and 150C. 180 samples were tested. Munikoti [7] tested 20 vendor lots of 50V rated COG, X7R and Z5U capacitors at 400V and 140C and found correlation with a standard 100V, 125C, 1000 hour test.

The purpose of the test design is to create a failure model based on a failure definition of 100 µamps leakage current. Temperatures of 300°C and 350°C were selected. Munikoti [7] recommends measuring dielectric breakdown voltage and that it is desired to have a breakdown voltage greater than 2x the maximum test voltage. Leakage current measurements were made at 300°C and 350°C conditions of the dielectrics as shown in Figure 7. Both capacitor dielectrics have leakage currents less than an order of magnitude of the failure criteria at >16 times their rated voltage. Acceleration voltages of 100 (2x), 200 (4x), and 290V (5.8x) were selected to balance the need for time acceleration, equipment limitations, and stay close to the use voltage (15-25V). Using typical voltage exponents, very high acceleration factors would be given with these levels.

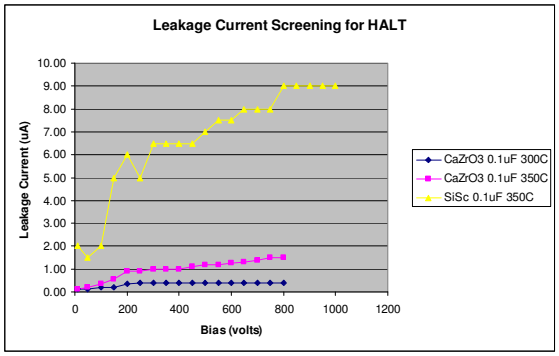


Figure 7 Leakage current screen test

A special fixture design was made to survive these temperatures, provide a voltage bias and monitoring during the testing. The fixture for testing the capacitors in situ is shown in Figure 9 and a section view of the fixture is shown in Figure 10. The fixture provides capacity for up to 30 samples. Bias to the samples is provided using spring loaded shoulder bolts within the sample cavity. The fixture housing is made of Macor to provide high temperature (up to 1.25E8 ohm-cm @350C) insulation resistance. The fixture base is nickel-plated (50-150 µinch) copper and is used as the electrical ground. Electrical connection to the shoulder bolts and base is provided using Tyco/AMP StratoTherm ring tongue terminals (#321896). The terminal is crimped to 20 AWG nickel plated copper strand wire (10/0.010) insulated with glass reinforced mica tape. The samples are loaded into each hole with one termination in contact with the base (ground) and the other end against a spring-loaded stainless steel #10-32 socket head shoulder bolt connected to the positive supply. The springs are made of 304 stainless steel. The spring load provides 1-2 lbs of normal force to the termination to reduce contact resistance. The springs may be selected according to the length of the capacitor being tested. Macor spacers are used to support the capacitors to prevent skew of its position and to prevent an electrical short if the capacitor fractures. The spacers are half cylinders cut to a length just short of the capacitor length. The environmental ovens used for this test are Thermolyne 6000 furnaces. A 1 inch diameter access hole is located at the top of the furnace that can accommodate up to 70 wires. The test circuit is taken from Mil-Prf-123 and is shown in Figure 11.

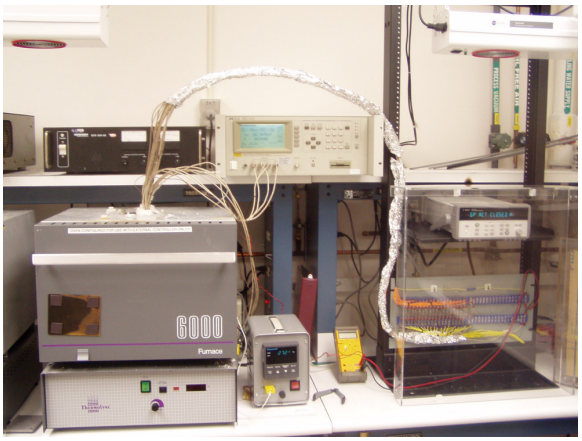


Figure 8 HALT test facility

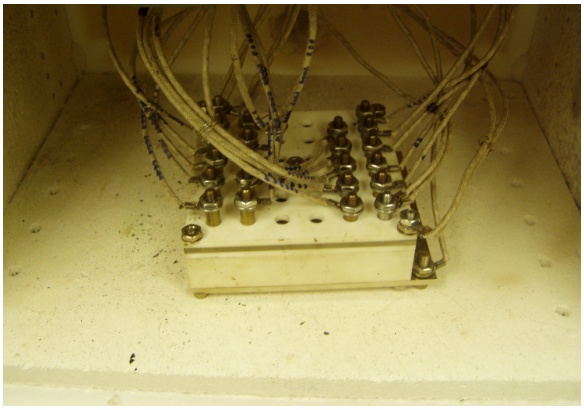


Figure 9 High temperature HALT test fixture

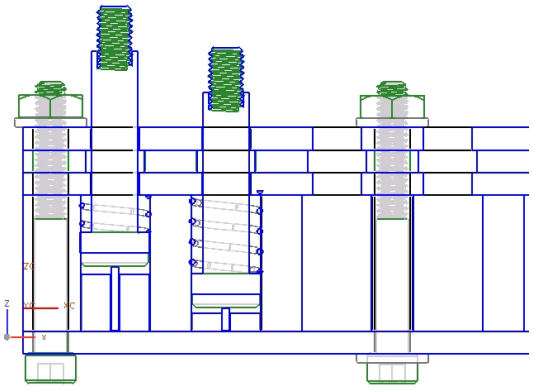
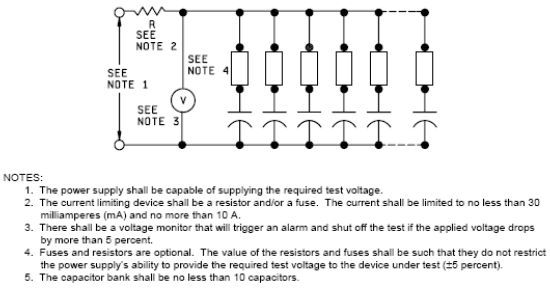


Figure 10 High temperature HALT fixture section view (tall and short samples)



NOTES:
1. The power supply shall be capable of supplying the required test voltage.
2. The current limiting device shall be a resistor and/or a fuse. The current shall be limited to no less than 30 milliamperes (mA) and no more than 10 A.
3. There shall be a voltage monitor that will trigger an alarm and shut off the test if the applied voltage drops by more than 5 percent.
4. Fuses and resistors are optional. The value of the resistors and fuses shall be such that they do not restrict the power supply's ability to provide the required test voltage to the device under test (±5 percent).
5. The capacitor bank shall be no less than 10 capacitors.

Figure 11 MIL-PRF-123D 4.6.6.2.1 figure 4 test circuit

Results

The capacitance change from room temperature to 350°C was taken in the fixture for each capacitor. The SiSc capacitor shows strong temperature dependence on the order of 15% nF/°C. The CaZrO3 BME capacitor had little temperature dependence on the order of 0.48% nF/°C.

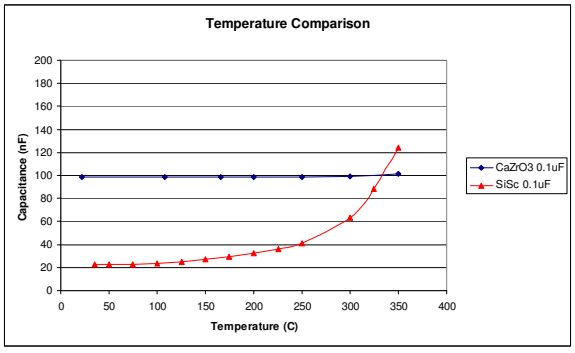


Figure 12 Capacitance over temperature

During the life testing a sample capacitor was connected in the fixture with a 4 wire connection and 1 meter long cables to make capacitance measurements during the test. The capacitance was measure periodically during the HALT test runs at a fixed temperature. Figure 13 shows a plot of the sampled data points for each capacitor. Both capacitors show stability at 300°C. The ScSi capacitor was halted after 2500 hours with –3.3% change in capacitance. The $CaZrO_3$ capacitor has accumulated >4000 hours with –3.0% change in capacitance.

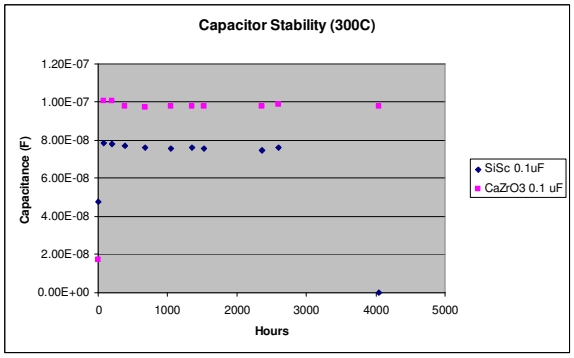


Figure 13 Capacitance stability at 300°C

Highly Accelerated Life Testing (HALT) was conducted on the SiSc and $CaZrO_3$ 0.1uF capacitors. Ten samples were tested at each voltage and temperature condition that is listed in Table 2. The SiSc 0.1 uF capacitors were run at 100V, 200V, and 290V at 300°C and 350°C. This capacitor was also run at 50V and 350°C but was not run at 50V 300C. The $CaZrO_3$ capacitors were run at 100V, 200V, and 290V only at 300°C. A 50V 300°C test condition has not shown enough failures at this time to report. Plans are to continue testing this capacitor at the same voltage bias at 350°C to complete the failure model parameters.

Table 2 HALT test sample and condition summary

Sample	#	Bias	Temperature
SiSc 0.1 uF	10	50V (350C only), 100V, 200V, 290V	300°C 350°C
$CaZrO_3$ 0.1uF	10	50V, 100V, 200V, 290V	300°C 350°C (planned)

Distribution plots are shown in Figure 14 for the SiSc 0.1 uF group using lognormal distributions. The shape parameters for the test conditions do not all representing the same failure modes. The shape parameter for the highest stress condition (290V,

350C) is significantly different than the other conditions indicating a different failure model.

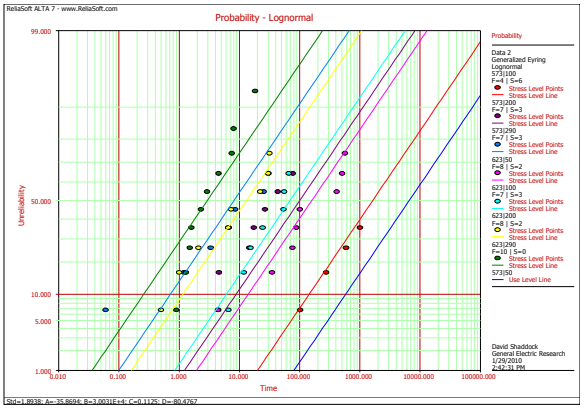


Figure 14 SiSc 0.1 uF capacitor HALT (100V, 200V,290V; 300°C, 350°C)

Distribution plots for the $CaZrO_3$ capacitors is shown n Figure 15 for the test conditions completed. It can be seen that the highest stress condition has a different failure mode than the lower stress conditions. This may indicate an upper bound for this capacitor voltage that may be used at this temperature.

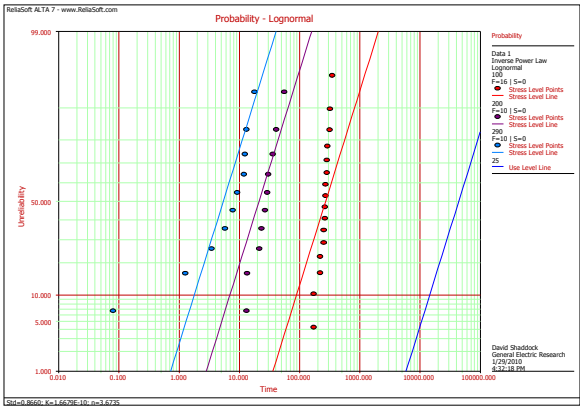


Figure 15 $CaZrO_3$ 0.1 uF capacitor HALT (100V, 200V; 300°C)

The acceleration model parameters of Equation 1 were solved for the SiSc capacitors data and an inverse power law model for the $CaZrO_3$ capacitors since they have been tested at only one temperature at the time of this report. Equation 1 reduces to the inverse power law for only one temperature. In both cases, the highest stress condition was not included in the analysis. The calculated model parameters for the two dielectrics are shown in Table 3.

Table 3 Calculated model parameters and mean life prediction (lower 90% confidence interval)

Group	n	Ea	Mean: 300°C, 25V
SiSc 0.1 uF	1.85	3.5	48454 hrs
$CaZrO_3$	3.67	NA	17254 hrs

The voltage exponent is comparable to typical industry standard values for the $CaZrO_3$ and lower for the SiSc. Activation energy for the SiSc is higher than typically found in typical capacitor dielectrics indicating robustness to temperature.

The two models and modelling parameters are used to predict the mean life at 300C and 25V bias. The lower confidence interval of the mean life for each dielectric is listed in Table 3. All of the conditions listed are more than sufficient to meet a 1000 hours. Continued refinement of the model for the $CaZrO_3$ dielectric will be made using the additional test condition at 350°C.

Resistor Technology for High Temperature

Electron scattering causes resistance to electrical current from thermally generated lattice vibrations, point and line defects, and impurity atoms. Mattheisens's rule states that resistivity is the sum of lattice vibrations, ρ_L and impurity defects, ρ_I. The lattice vibrations are a function of temperature, T.

$$\rho = \rho_L(T) + \rho_I$$

The resistivity due to lattice vibrations is a function of temperature and may be represented by $\rho_L = \rho_{L0}\left(1+\alpha_0(T-T_0)\right)$, where α_0 is the temperature coefficient of resistance.

The amount of noise on a circuit depends on the conduction mechanism but increases in temperature. Johnson noise voltage, e_n, and current, i_n, are defined by

$$e_n = \sqrt{4kTR\Delta f}\ ,\quad i_n = \sqrt{\frac{4kT\Delta f}{R}}$$, where Δf is the bandwidth, R is resistance, T is absolute temperature, k Boltzmann's constant. Wirewound and Metal film resisters have the lowest noise. The HTL testing reported by Naefe [8]] shows testing of a Dale chassis mount resistor having some s capability to survive 300°C.

Thin film resistors provide precision values and low temperature coefficients. Thin film resistors are produced by depositing the resistive material onto a substrate using thin film deposition processes such as sputtering, evaporation, reactive sputtering or chemical vapor deposition. The films are oxidized to produce a layer that seals the metal from corrosion and drift. Thin film resistors have better resolution, stability, high frequency performance, smaller size and TCR values than thick film resistors [9]. Nickel chrome resistors are subject to interdiffusion and oxidation at 400-500C.[10].

Thick film QPL resistors (MIL-PRF-55342) are low cost and available with high temperature compatible terminations such as gold and platinum gold. Ruthenium oxide has high oxidation resistance and can be run up to 1000C without any degradation in performance [9]. They also have good stability, low TCR, and low noise. Surface mount discrete thick film resistors provide miniaturization and the ability for the resistive material to be deposited directly onto a ceramic, tested and trimmed at that level in high volume. As for capacitors, packaging may be a limitation to high temperature applications. The package must be compatible with assembly methods for interconnection. Termination materials such as tin or AgPd pose risks at high temperature as discussed earlier.

Resistor Reliability Testing

Reliability models for resistors contain temperature and humidity as factors. Humidity is not a concern at the temperature of interest. Temperature is also affected by the applied power through Joule heating.

Coleman [11] presented a model based on the percentage change in resistance ($\frac{\Delta R}{R}$) as a sum of failure mechanisms that are a function of time (t) and temperature (T).

$$\frac{\Delta R}{R} = \sum \alpha_i t^{n_i} \exp\left(\frac{-E_i}{kT}\right)$$ where α is a pre-exponent constant characteristic of the failure mechanism, E is the activation energy, n is the time dependence. Activation energies reported by Coleman [11] vary from 0.13 to 0.38eV and power exponent from 1/5 to ½ depending on the thick film material.

Results

Samples of QPL thick film resistors (1kΩ, 1%) were tested for temperature sensitivity and change in resistance at 350°C at rated voltage (0.25W).

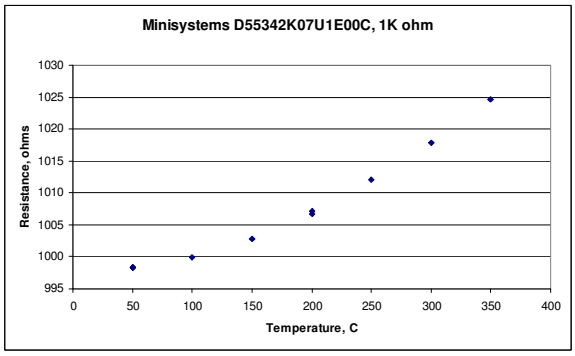


Figure 16 Thick film resistance over temperature

The resister temperature response shows a change in resistance of 7.8% from 50 to 300°C. A plot of the resistance change up to 2800 hours is shown in Figure 17 along with reference lines indicating +/- 2% change in resistance. Five out of ten resistors have exceeded this criteria but it is too few to make a reasonable distribution plot. It is expected that more failures will be reported at the time of the HiTEC 2010 conference. The first failure occurred at 1083 hours and is shown in Figure 17 as the grey line. A power outage occurred that took the bias power off line a few times causing gaps in the data. The grey sample did not come back on line due to a system monitor that would take the sample out of circuit when a voltage threshold is detected. The monitoring program was changed to keep the resistors in circuit to allow for other failure thresholds to be made and allow a degradation analysis.

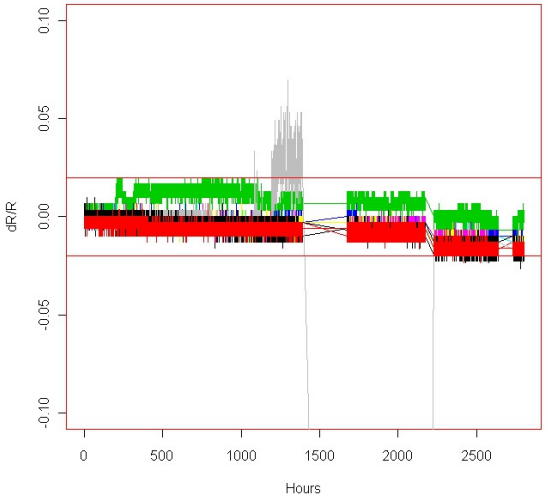


Figure 17 Thick film resistor change in resistance at 350°C (2800 hrs)

Conclusion

A test fixture was developed that allows for reliability testing of passive surface mount components at high temperature while under bias. The fixture was used to measure capacitors and resistors at high temperature with a voltage bias. A process was developed to strip tin from tin plated components and re-plate them with immersion Au to make them more compatible with high temperature assembly methods. SiSc capacitors were tested at 300° and 350°C with accelerated voltages. The voltage exponent (1.85) and activation energy (3.5 eV) was calculated. The projected life using the acceleration model is in excess of 1000 hours. $CaZrO_3$ capacitors are in process of similar testing. Results of 300°C testing at accelerated voltages are reported with predicted life in excess of 1000 hours. The voltage exponent was calculated to be 3.67, which is much higher than typical capacitors reported. Testing of a thick film QPL resistor is in progress and measurements of the temperature response and degradation of the resistors at the time of this writing is reported. The resistor has a first failure at 1083 hours at the failure criteria of +/-2%. Further work is planned to test the $CaZrO_3$ capacitors at a second temperature level to determine activation energy. Further testing of the thick film resistors at a a second temperature and of wire wound surface mount resistors is planned.

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