Development of a SiC SSPC Module with Advanced High Temperature Packaging

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Abstract

Development of a multi-chip power module (MCPM) is reported that uses advanced metal-matrix composite aluminum packaging to manage high thermally induced stresses in devices that incur 350°C transients. The MCPM uses parallel SiC devices to control 120A DC nominal, 1200A fault in a 270V DC system. Electrical system modeling is presented to characterize electrical fault transients that induce electrical and thermal stresses in the semiconductors and packaging. The characterization of the advanced aluminum-based packaging system, which uses composites, such as AlSiC, and direct bonded aluminum (DBA), is discussed to manage the thermal stresses and transient heat flow.

Key words: SSPC, SiC, High Temperature

I. Introduction

In the commercial and military aircraft industry, new designs are moving toward More Electric Aircrafts (MEAs) [1][2][3], and the Solid-State Power Controller (SSPC) is one of the key components in the onboard system superseding conventional mechanical, pneumatic and hydraulic systems [4]. Having faster fault current interruption capability (a few microseconds) and reduced weight, the SSPC can provide reduced weight, size and overall operating expense of aircrafts and enables system flexibility [5].

The 270V DC level was introduced to supersede the conventional 28V DC level for military applications (230V AC for civil applications), and hence, reduce the current rating, as well as the size and weight of the wires [6]. Presently, typical commercial SSPC products on the market are all under 30A. These devices are used to connect load to the secondary distribution bus, while interrupters on the primary bus are conventional mechanical, pneumatic and hydraulic devices capable of much higher current rating requirements. A 50A SSPC prototype is reported in [7] and a proposed 100A SSPC model is simulated in [5] to determine the required number of silicon die, for transient operation, but packaging issues are not included. The research reported here describes the design of a 120A nominal, 1200A fault, SiC SSPC module for a 270V DC airborne system, with applications as a fault current interrupter in the primary bus.

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II. Electrical Function of an SSPC

Current Trip Algorithm

The SSPC trip-current profile follows an i^2t curve depicted in Fig. 1. When the i^2t data sampled from the system is below the curve, the SSPC remains closed, and opens instantly at levels above the curve to protect the wires, loads, or itself. In practical applications, this curve is presented as a band with upper and lower limits. A permitted variation range is left between two limits to avoid frequent actions under unstable currents.

Within an application, such as the power system in an airframe, an equivalent system wiring resistance, R, can be defined. The total thermal energy absorbed by the wiring is $E = i^2Rt$. A more sophisticated model would define R as temperature dependent to account for wire heating from multiple over-current excursions. An $R(T)$ bends the straight slope in the i^2t curve of Fig. 1.

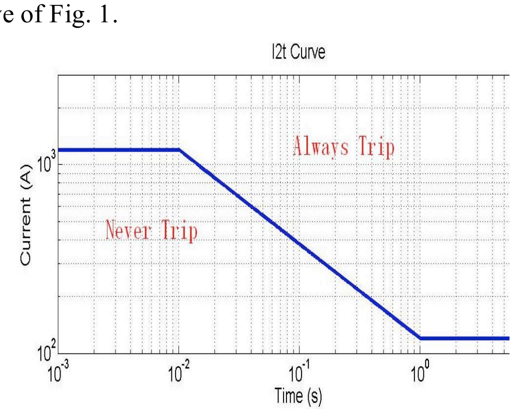

Figure 1. i^2t Curve

Following a conservative design approach by assuming an adiabatic wire environment, e.g. ignoring heat loss into the wire insulation, an i^2t constant can be defined for a particular system, which equates heat generated in a current carrying component (i^2Rt) to heat absorbed by the component (product of mass, specific heat and temperature rise). A well accepted adiabatic temperature rise formula given in standards, etc. [8][9] can be used to determine a design requirement for the SSPC module. The equation is:

$$i^2 t = K^2 S^2 \ln\left(\frac{T_2 + \beta}{T_1 + \beta}\right) \quad (1)$$

where

I = short-circuit current (RMS over duration), A;

t = duration of short circuit, s;

K = constant depending upon the conductor material, $As^{0.5}/mm^2$;

S = cross-sectional area of the conductor, mm^2;

T_2 = final temperature of conductor, °C;

T_1 = initial temperature of conductor, °C;

β = reciprocal of temperature coefficient of resistance(α) for conductor material at 0°C, °C.

$$K^2 = \frac{C\,(\beta + 20)}{\rho_{20}} \quad (2)$$

where C = volumetric specific heat of the conductor at *20°C, J/°C* mm^3; ρ_{20} = resistivity of conductor metal at *20°C, Ωmm*. The value of K and β is *226* and *234.5* respectively for copper, and *148* and *228* for aluminum. The adiabatic method is sufficiently accurate for a majority of practical cases and any error provides a conservative evaluation [8].

Parameters in Eq. (1) are defined by the system except T_1, the initial temperature resulting from abnormal conditions. For example, if the time between two overload-faults disallows adequate cooling of wires, a different initial temperature for the second fault would be used. A similar case results from an extreme flight environment. The higher initial temperature induces a lower i^2t constant, and thus, shorter fault current duration. Often thermal sensors are required on the wires or inside cables to provide the initial temperature parameter.

Equivalent Constant for SSPC Design

Monitoring and control in the system determines when the SSPC activates (opens). This is an operational condition. A design condition requires that the SSPC be properly sized to accommodate the overload energy flow below the i^2t curve in Fig. 1, and, itself, not overheat forcing a premature trip. Since SSPC design is such as to minimize volume, weight and steady-state electrical loss, the SSPC must have sufficient thermal capacity not to overheat before the overheating of a system component, e.g. wiring. Hence, the i^2t constant calculated above also applies to the SSPC design, and of course with safety margin. The SSPC, itself, is a thermally limited system component and has its own i^2t energy profile.

III. Semiconductor Die Selection

Primary thermal generation sources within an SSPC are the semiconductors. During normal operation at nominal rated current, thermal generation is relatively small compared to overload requirements. The difference in design philosophy between the two states, however, is substantial. During normal steady-state operation the semiconductor die area, or die count, is determined by targeted module efficiency and follows traditional power module design approaches. For transient over current operation the die area is dependent primarily on the allowable peak junction temperature of the die and thermal capacity of die and packaging, and becomes the dominant design objective. For this SSPC design, nominal current is 120Adc with a 1200A trip, and the die area, respectively, is approximately 1:2 for a given required i^2t response.

The SSPC performance is primarily dependent on transient thermal capacity. Extending junction temperatures substantially increases the thermal capacity. As an estimate from Eq. 1, the approximate ratio difference of the aluminum structure operated at *350°C* versus *175°C* is *2.75* increase in capacity. One advantage of SiC is the higher temperature operation. In this development the pulsed capability of SiC to operate to *350°C* is used and the packaging is developed to operate longer term at *>450°C*.

The SiC MOSFET being considered is nominal 20A/1200V 4H-SiC SiC DMOS with 4mm×4mm dimensions and $12mm^2$ active area [10]. For this prototype the 20A die is selected for scaled development. After testing, the power module and die-count are scaled to accommodate single die approaching $56mm^2$. The die is compatible with aluminum-based packaging.

Special Concerns for SiC MOSFET

SiC MOSFETs bring in effective characteristics, such as lower on-resistance, higher junction temperature capability, etc., but have practical issues as well. To ensure safe operation of the SSPC, the power semiconductor device junction temperature must be monitored. Conventional Si-die SSPCs access junction temperature by sensing voltage across the on-resistance of the switch, and estimate the junction temperature through a preset voltage-temperature table. However, this cannot be applied to this early SiC development reported here:

1) The temperature-dependent $R_{DS(on)}$ variation in SiC MOSFETs is not as significant as conventional Si devices, hence using $R_{DS(on)}$ or V_{DS} of the SiC devices is challenging for this critical application. A study by CREE Inc. has demonstrated that the $R_{DS(on)}$ of SiC MOSFET only increases by *20%* from *25°C* to *150°C* while the contrast Si super junction MOSFET increases by *250%*[10].

2) This SSPC reported here operates at *350°C* maximum transient junction temperature and exceeds the upper limit manufacturers commit to in their data sheets. Again, sensing through $R_{DS(on)}$ in this early development is limited or impractical.

IV. SSPC Module Description

Due to the high current, high temperature operating characteristics, special requirements constrain material selection in the packaging. Long-term reliability is achieved by minimizing chemical degradation at interfaces and managing mechanical stresses. To minimize dissimilarity at material interfaces, the power module design should seek a mono-material approach. A proposed approach uses aluminum (Al) [11]. This includes Al metalized SiC MOSFET, Al interconnects (bonding wires and traces), and AlN layer for electrical insulation. The Al acts as an excellent stress relief during temperature cycling due to the low Young's Modulus, and also provides a common metallurgical bonding medium.

Figure 2. Metal matrix composite module, e.g. AlSiC, with Al-interconnect pads for active and passive components, and terminals. Aluminum on AlN on Al-composite.

The Al has a 2.5 times higher electrical resistance and a 40% lower thermal conductance than copper. Thus, a 2.5 times thicker conductor interconnect structure is required for equivalent power dissipation. The thermal conductor resistance is not a large absolute value in the module. During transient high current conduction, any resistive loss is included in the thermal capacity.

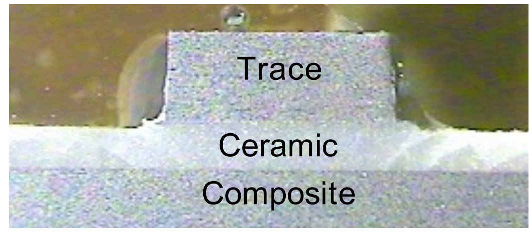

Figure 3. Trace of Al bonded to ceramic captured in metal composite, and showing strong bond lines.

An aluminum-based power module was designed using a cast process to place Al interconnects onto an AlN substrate captured into an Al metal matrix composite. A patterned module is shown in Fig. 2.

Ceramic/Metal-Matrix Interface

The capturing of ceramic in a metal matrix composite with inclusion of as cast interconnects provides an efficient mechanism of creating a 'metal-ceramic wiring board' for power electronic modules. Shown in Fig. 3 is a cross-section of the interconnect, substrate and metal matrix composite structure. The bond lines are clean and, from SEM analysis, well diffused into aluminum. A thin aluminum skin exists between the ceramic and composite structure (not visible in the figure).

V. Thermal Transient Characterization

Transient thermal performance

The focus of this research is to determine the number of parallel dies for a given i^2t energy constant. The die count is primarily dependent on the transient joule heating during overload and on die and module characteristics to rapidly spread heat, avoiding excessive die junction temperature. The thermal issues conflict with reducing size and weight of the SSPC. More dies spread the heat and reduce initial transient heat density in each die. However, more dies increase package size and total die costs. Reliability increases with less distributed thermal stress, but decreases with more die interconnections. Using larger dies directly increases reliability, particularly at higher transient thermal densities. The thermal conductance for 4H SiC is much higher than the surrounding Al system and provides substantial rapid heat spreading.

To maximize the power density and determine the

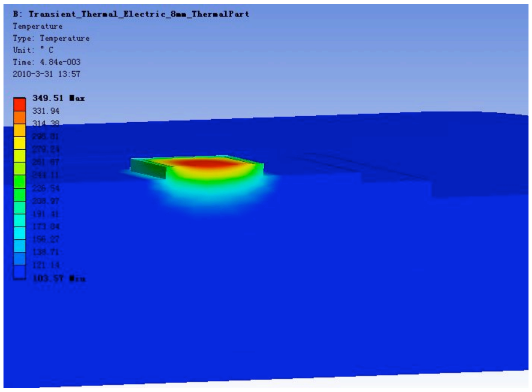

Figure 4. A transient thermal simulation showing a peak *350°C* top-side and *104°C* bottom-side profile at *4ms* for an 80A current drive.

required SiC die area, i.e. number of dies, a group of transient thermal simulations relating the maximum sustaining fault current to maximum allowed junction temperature were performed.

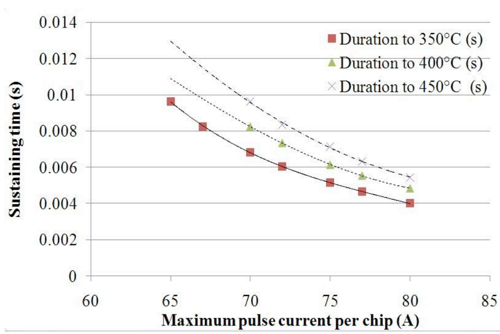

Figure 5. Pulse current per die vs. sustaining time before reaching the maximum junction temperature

Material parameters are listed in Table 1. The module was designed for attachment to a *105°C* cold, hence a *105°C* bottom thermal ground was used. For this design a maximum allowed junction temperature was set to *350°C*. The SiC die and packaging can operate to *450°C*, so a sufficient design margin is inherent in the design. A single-point simulation result is shown in Fig. 4.

With the peak die junction temperature set to *350°C, 400°C* and *450°C*, and module thermal ground set to *105°C*, successive transient heat loads were generated in the die by successively increasing a unit-step pulse current. The current value is representative of an over current trip value. The product of the $R_{ds\text{-}on}$ and peak current determines the heat load. Temperature variations of $R_{ds\text{-}on}$ at different current levels are included in the heat loading.

With thermal boundaries at fixed values and thermal loading as the independent variable, the variation of total sustainable time can be determined. The results of successive thermal loading along with added variations of peak allowed junction temperatures are plotted in Fig. 5 showing the maximum sustaining time an SSPC can be closed before tripping open. This sets the i^2t constant and defines the i^2t characteristic for the SSPC. For example, the sustaining time in Fig. 1 is *10ms* for a maximum pulse current of *1200A*.

Table 1. Material Parameters in Simulations

	4H SiC	Silver Glass	Pure Al	AlN	Base plate
Density (g/cm3)	3.21	7.52	2.7	3.3	2.4
Thermal Conductivity (W/mm*K)	0.49	0.2	0.25	0.29	X 0.23 Y 0.23 Z 0.12
Specific Heat (J/g*K)	0.69	0.31	0.23	0.74	0.852

Die Count (Chip Count) & Module Rating

According to Eq. (1), the i^2t constant for a specific cable can be determined, and then, curves in Fig. 5 can guide the SSPC designers to address the die-count. In this research the permissible allowable surge current per SiC die was determined to be *75A*. Hence, from Fig. 5 the maximum sustaining time was *5ms*. The peak transient trip current requirement of the SSPC was 1200A. The SSPC design would require 16 parallel die to achieve a 1200A trip current rating with a 5ms sustaining time.

VI. Prototype Module Development

Demonstration of research results of a *120A/270Vdc* SSPC design is scaled using only 4 of the 16 smaller SiC semiconductor devices. The approximate die area for the full SSPC requires approximately *200mm*^{2} active area (*16* parallel die at *12mm*^{2} each). SiC devices in development could drop the total number of die to four or less.

The prototype module reported here uses the physical structure shown in Fig. 2 to accommodate four SiC MOSFET die on a continuously connected aluminum pad for drain connections with an overlay for source/gate/terminal interconnections. The complete build-up of the module is not reported here, but only the determination of the optimum set of devices for scaled performance.

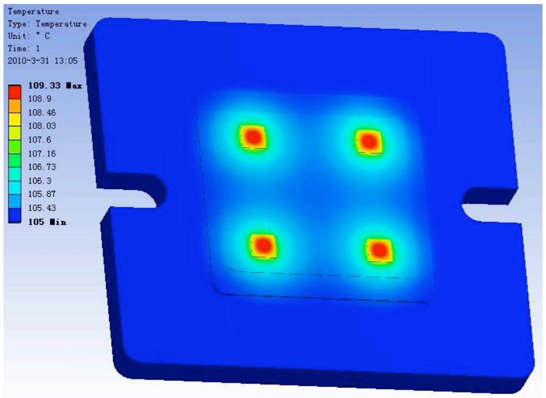

Figure 7. Temperature Distribution of a four-die power module at Steady State

Optimum Die Layout and Count Per Module

Excessive interaction of joule heating between multiple dies mounted on the same module substrate effectively increases the thermal impedance of the power module. However, excessive separation of die moves die closer to the module walls and, again causes a limitation on heat spreading effectively increasing the thermal impedance. By iteratively

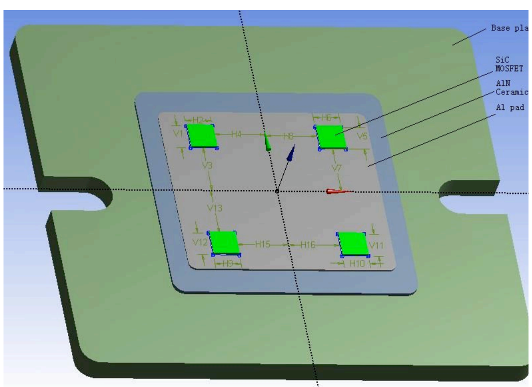

Figure 6. Optimization of die placement. The edge-to-edge separation is half the keep-out distance.

simulating the steady-state temperature distribution of a four-die power module as dies are symmetrically separated, an optimized die layout can be determined.

The spacing or die "keep-out" distance is the distance from the edge of each die to the x- or y-axis. For the symmetric layout in Fig. 6 the distance between any two dies is two times the keep-out distance of each die. Through simulation, a steady-state thermal distribution of four 4mm-square die is shown in Fig. 7. Both Figs. 6 and 7 are based on Fig. 2 with a continuous aluminum pad.

Results of iterative simulations with various keep-out distances are depicted in Fig. 8. The results show that when the keep-out reaches 8mm the power module will achieve the lowest thermal impedance, about 0.665°C/W per die, 0.166°C/W per module. According to the steady-state keep-out optimization, the prototype module best permits only four dies.

Characteristics of the Thermal Profile

The optimum location of die rather close to the edge of the aluminum pad should not be unexpected. The aluminum pad thickness is 380μm while the ceramic is 580μm embedded in a rather large composite. Since the thermal conductivity of all the materials, as seen in Table 1, are similar at 230 W/m*K to 290 W/m*K, the spreading is approximately uniform and continuous.

Also seen from Table 1, the composite base plate is anisotropic. The fast transient current response by

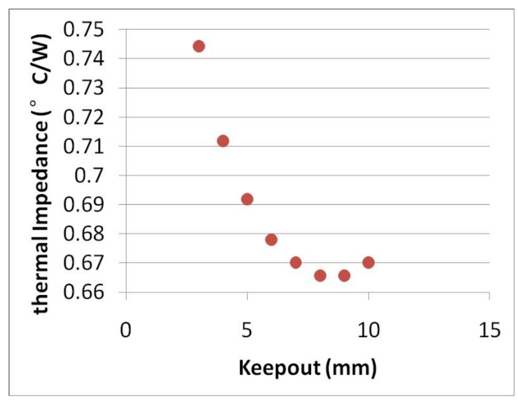

Figure 8. Thermal Impedance vs. Keep-out Distance

SiC devices creates a transient thermal loading of the die and upper part of the module. The mass and specific heat of the materials govern the thermal capacity. Integrating in other materials, such as copper, can provide thermal benefits, but at the expense of reliability as the system moves away from a mono-material approach.

VII. Conclusions

This paper reports on development of a 120A/270Vdc Solid-State Power Controller (SSPC) with a 1200A/5ms trip limit for application to DC aircraft electrical systems. The solid-state switches are SiC MOSFETs operated to a *350°C* transient junction temperature. Aluminum-based power module packaging is designed for 450°C, and in combination with the SiC devices provides approximately a 2.3 times thermal capability over silicon approaches. The aluminum-based multi-chip power module (MCPM) has cast Al interconnects onto AlN ceramic which is captured in an Al metal matrix composite, such as AlSiC. The high temperature, aluminum-based module approach provides reduced size and weight.

The 120A high current SSPC design brings up critical issues that have not been discussed previously, particularly in optimizing the number of parallel die per package. The optimum number is determined by performing transient thermal and steady state simulations. Also included is optimization of the die layout within the multi-chip power module.

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