Edge-Controlled Mechanical Failure of Si and SiC Semiconductor Chips†

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Abstract

Silicon (Si) and silicon carbide (SiC) semiconductor chips are subjected to thermal gradients during service, have coefficient of thermal expansion mismatches with the constituents they are attached to, and are therefore subjected to thermomechanical tensile stresses that can initiate their fracture. Because of inherent brittleness, their probabilistic (Weibull) tensile failure strength was examined to understand sustainable tensile stresses and any exhibition of strength-size-scaling. Failure stress testing of entire (10-mm-square) chips was conducted using uniaxial flexure (3-point-bending) and biaxial flexure (anticlastic bending). The advantage of the anticlastic bend test is all eight primary edges are subjected to identical sinusoidal stress distribution so tensile failure stress is concurrently sensitive to edge-state quality, surface-state quality, crystallographic orientation, and any strength anisotropies of any of those.

Tensile stress tolerance of both Si and SiC chips was limited by extrinsic strength-limiting flaws located at their edges and on lapped surfaces too in the case of the Si. Both materials exhibited strength-size scaling; namely, a larger chip is likely to fail at a lower tensile stress. The anticlastic bend test method was effective for evaluating edge failure stress provided surface-type strength-limiting flaws were not dominant. Edge-strength anisotropy (i.e., crystallographic orientation dependence) was observed with both the Si and SiC chips. Surface-strength anisotropy also occurred with Si chips because one side was lapped and the other polished. Lastly, the SiC chips failed at much higher tensile stresses than Si chips; however, that strength difference could be a ramification of differences in edge-slicing quality and not necessarily from intrinsic material differences.

Key words: Weibull distribution, failure probability, strength, tensile stress, strength-limiting flaw, reliability

Introduction

Silicon (Si) and silicon carbide (SiC) chips in power electronic devices are subjected to thermal gradients, have coefficient of thermal expansion mismatches with the constituents they are attached to, and therefore are subjected to consequential thermomechanical tensile stresses during operation that can initiate their fracture.

Being they are brittle like glasses and ceramics, it stands to reason that their tensile failure strength is statistical in nature. Several studies have pursued the mechanical testing of silicon chips and interpreted the measured failure stress in this manner.

Wereszczak *et al.* [1] conducted 4-pt bend tests using different test specimen dimensions and statistically examined the strength of etched and polished surfaces. They found that edge-slicing quality could be quite limiting of the overall failure stress but that surface-type flaws, and hybrids of edge- and surface-type flaws could be operative too. A convenient manner to portray their competition is shown in Fig. 1. Extrinsic flaws (e.g., surface pitting, scratches, edge-chipping) tend to limit the mechanical strength of chips whereas intrinsic flaws (volume- or bulk-based) are very rare. Another class of brittle materials that is like semiconductor chips is glass.

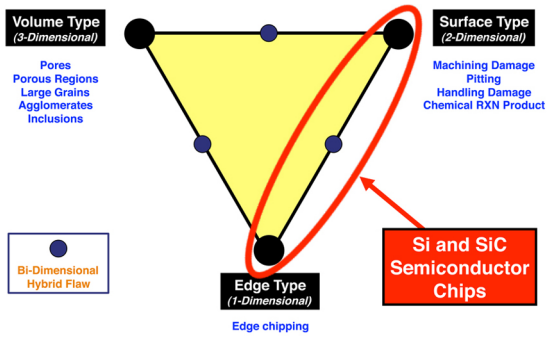

Figure 1. Potential strength-limiting flaw types in semiconductor chips.

Cotterell *et al.* [2] examined the statistical failure stress using 4-pt-bend and ring-on-ring (i.e., axisymmetric 4-pt-bend) testing. While Cotterell's work was systematic, concern over those results arises from the relatively large spans that were used relative to the chip thickness, and the belief that nonlinear elastic effects were likely introduced as a consequence. These were not accounted for and inaccuracy in the results was likely caused. Such issues need to be considered in flexure testing and indeed are considered in standardized tests for uniaxial and biaxial flexure testing [3-4].

Colleti *et al.* [5] considered the competition of edge- and surface-based strength limiting but used ring-on-ring testing to focus study on the latter.

Zhao *et al.* [6] used 3-pt-bending and ball-on-ring (i.e., axisymmetric 3-pt bending) to study the convolution of edge- and surface-type flaws that limit failure stress. A problem with ball-on-ring testing is its generated effective area (i.e., sampled area under tension) is quite small and uncertainty can therefore be produced when comparing the failure strength of different surface conditions. Additionally, Zhao *et al.* used a 3-parameter Weibull distribution to fit the failure stress data; while a "good" fit was perhaps produced, disadvantages of using the 3-parameter fit are it can mask the presence (and problems) of exclusive flaw populations (an indicator of inhomogeneously distributed flaw populations) [7-8], and it does not lend itself easily to strength-size-scaling analysis [9] that is routinely used with 2-parameter Weibull distributions [10] when designing brittle material components and estimating their mechanical reliability.

The present study had several objectives. First, it sought to measure and compare failure stresses in Si and SiC semiconductor chips that had the same physical size and mechanically tested in the same manner. Second, owing to the author's past experience with edges limiting strength in sliced Si semiconductors [1], we sought to use mechanical test methods that would promote failure initiation at the edges. Third, the authors have performed an extensive amount of mechanical testing involving edge characterization of glass tiles [11]. Owing to the fact that glass tiles have similarity to semiconductor chips (i.e., very smooth surfaces with cut, chamfered, or sliced edges or the same flaw types of interest in Fig. 1), and that the authors have found anticlastic bend testing to be an effective method to measure failure stresses with glass tiles, anticlastic bending of Si and SiC chips was pursued to judge its applicability.

Experimental

Silicon {111} and silicon carbide (n-type 4H {0001}) chips were acquired from commercial sources. Dimensions were 10 x 10 x 0.25 mm. One side of the Si chips was lapped and the other was polished. Both sides of the SiC chips were polished. None of the chips of either material had metallization on them. Neither specific slicing method nor procedure was prescribed for either material. Record of the orientation of all chips (or specimens) was kept through the testing history. The primary flat of the silicon wafer was parallel to <112> and that for the silicon carbide was parallel to <112bar0>.

Flexure testing of the entire (square) chips was conducted using uniaxial flexure (three-point-bending) and biaxial flexure (anticlastic bending).

For 3-pt bending, a 5.0-mm span was chosen to sustain classical Eulerian beam bending with respect to the 0.25-mm thick chips. A schematic of the test configuration is shown in Fig. 2. 4-pt bending typically has an advantage over 3-pt-bending in that more of a specimen is desirably subjected to a uniform tensile stress; however, if test specimen geometries and fixtures are small (such as they are in this study), then it can be experimentally difficult to promote, sustain, and validate alignment with the 4-pt configuration. Because of that, the authors pursued 3-pt-bending because maintaining alignment is experimentally easy to achieve, and that advantage was deemed to be more important than the disadvantage of it sampling less material to a tensile stress.

The failure stress (S_{3pt}) for 3-pt-bending is represented by

$$S_{3pt} = \phi \frac{3PL}{2bt^2} \qquad (1)$$

where P is failure load, L is the fixture span (5.0 mm), b is the base (10.0 mm), and t is thickness

(0.25 mm), and ø (=1.02) is a correction factor that takes into account the relatively large base to thickness ratio for the chip to distinguish it from a beam [12]. The outer-fiber tensile stress profile across the span is shown in Fig. 3.

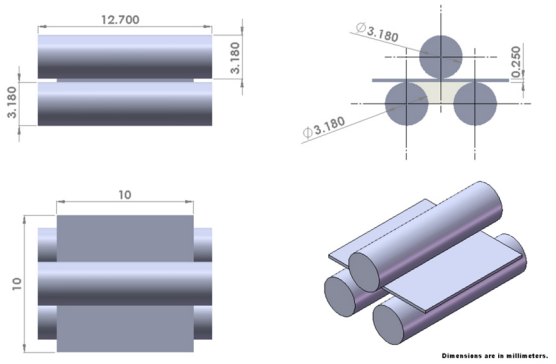

Figure 2. Schematic diagram of the 3-pt-bend test setup. The support span was 5.0 mm.

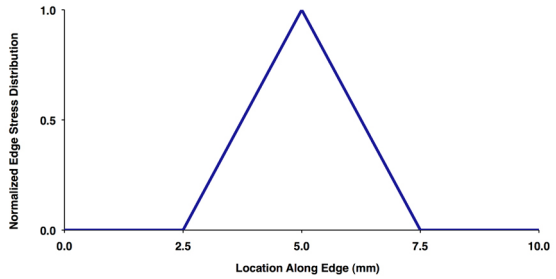

Figure 3. Outer-fiber tensile stress distribution for the 3-pt-bend fixture.

The anticlastic (AC) biaxial flexure specimen was first used by Zamrik *et al.* [13-14] to study crack growth behavior under biaxial fatigue conditions.

The advantage of the anticlastic bend test is all eight edges are subjected to identical sinusoidal stress distribution so the tensile failure stress will be sensitive to the chip's edge-state quality, crystallographic orientation, and surface condition too. Four balls, two on each side of the chip or plate, aligned along counter-opposing diagonals are compressed to produce the anticlastic bending state. This is an example where a schematic (see Fig. 4) is much more effective to describe the manner of loading than a narrative is.

A finite element analysis (FEA) model was constructed to examine the stress state of the 10 x 10 x 0.25 mm chips subjected to anticlastic bending. The first principal (equivalent) stress profile is shown in Fig. 5 for an applied compressive load of 100 N.

High radial tensile stresses around the four Hertzian loading positions are not the source of failure initiation if the surface condition of the plate is of high surface finish or has minimally sized flaws and if there are edge-located flaws of relatively large size or severity. This scenario is why AC bending works well with glass and also why it was considered for use in this study with semiconductor chips.

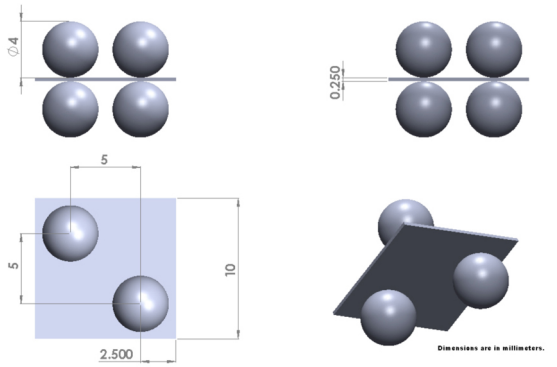

Figure 4. Schematic diagram of the anticlastic bend test setup.

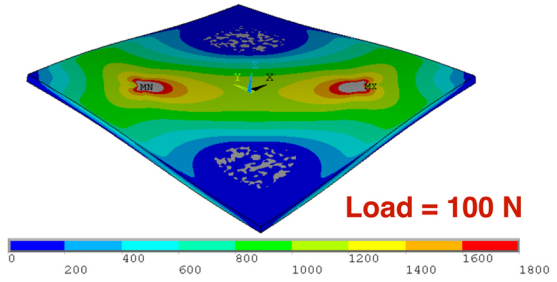

Figure 5. First principal (or equivalent) stress profile of an anticlastically bent silicon chip.

The stress profiles along two of the edges of an anticlastically bent specimen are shown in Fig. 6, and the relationship between compressive force and maximum tensile stress, as determined by FEA, is shown in Fig. 7. The sinusoidally produced stress profile along each edge is apparent, and all 8 of the primary edges are subjected to this. If the stress-limiting flaws at an edge are larger in size than those flaws on the surface of the plate, then failure initiation will commence from an edge. This is accomplished within a single specimen. Additionally, this AC bend method is sensitive to the chip's edge-state quality, crystallographic orientation, and surface condition too. Many specimens would be needed for a uniaxial flexure (i.e., 3-pt or 4-pt bending) test matrix to equivalently examine all these

effects, and "surface- based" test methods, such as ball-on-ring and ring-on-ring would not be effective at concurrently sampling edge-effects like the AC bend method.

To examine strength-size-scaling or tensile-failure-size-scaling based on Weibull effective length, the probability of failure (P_f) can be represented by

$$P_f = 1 - \exp\left[-\left(\frac{\sigma_{\max}}{\sigma_{0L}}\right)^m L_e\right] \qquad (2)$$

where s_{max} is the maximum applied tensile stress along the edges, s_{0L} is the scale parameter due to edge-type flaws, m is the Weibull modulus, and L_e is the effective length. The effective length is described as

$$L_e = \int \left(\frac{\sigma(x)}{\sigma_{\max}}\right)^m dx \qquad (3)$$

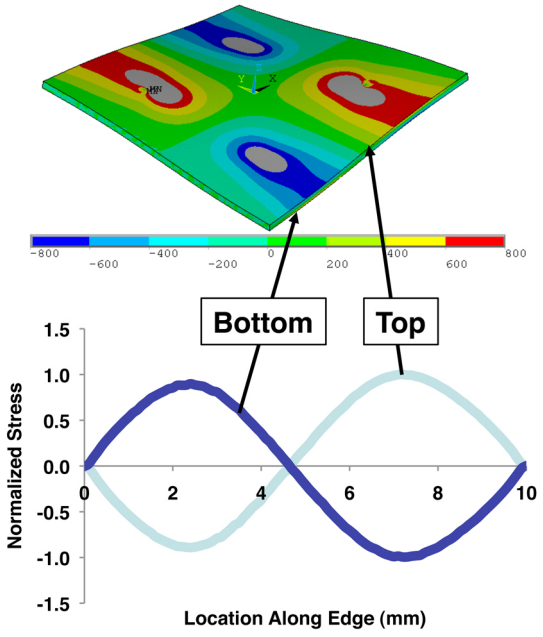

Figure 6. Stress profile along the edges of an anticlastically bent chip.

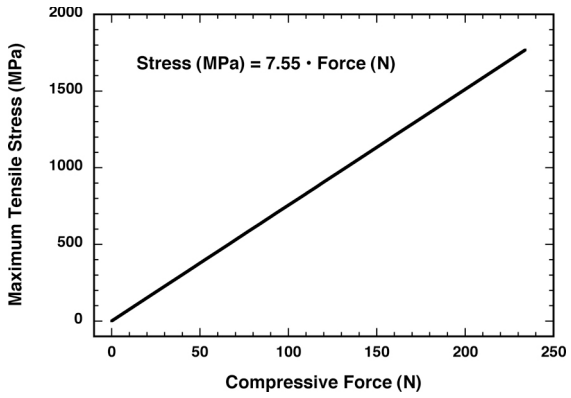

Figure 7. Maximum tensile stress as a function of compressive for the anticlastic bend specimen whose loading is shown in Fig. 4.

The effective length can be used for strength scaling whereby the strength of one component (or specimen in this case) can be predicted from that of another with different stress distribution and edge length by equating their probabilities of failure according to

$$\left(\frac{\sigma_{f1}}{\sigma_{f2}}\right) = \left(\frac{L_{e2}}{L_{e1}}\right)^{\frac{1}{m}} \qquad (4)$$

In order to evaluate the effective length using Eq. 3 for the AC bent chip, the stress distributions along the edges of the chip must be described as a function of position, x. This stress profile is illustrated in Fig. 6. Hence, Eq. 3 for the AC flexure specimen simplifies to

$$L_{e,AC} = \frac{4}{\sigma_{\max}^m}\left[\int_0^{x1} \sigma_{top\_edge}^m(x)\,dx\right] + \frac{4}{\sigma_{\max}^m}\left[\int_0^{x2} \sigma_{bottom\_edge}^m(x)\,dx\right] \qquad (5)$$

Unlike the AC flexure specimen, the 3-point bend test induces tensile stresses along only two edges. The effective length formula for a 3-point bend specimen is associated with the stress profile in Fig. 3 is given by

$$L_{e,3pt} = \frac{2L}{m+1} \qquad (6)$$

The effective lengths are a function of Weibull modulus and the profiles for the anticlastic and 3-pt bend specimens and are shown in Fig. 8. This figure shows that, for a given Weibull modulus, the anticlastic bend specimen subjects much more edge length to a tensile stress than the 3-pt bend specimen does.

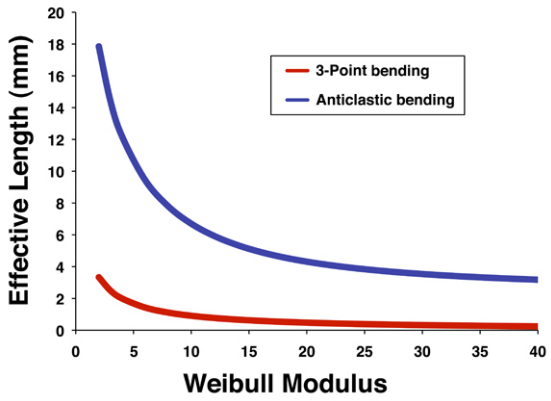

Figure 8. Weibull effective length as a function of Weibull modulus for the two bend test configurations used in this study.

All 3-pt and anticlastic bend tests were done using an electromechanical test frame and a crosshead displacement rate of 0.5 mm/min. At least 14 specimens were tested for each condition and their Weibull failure stress distributions were determine using commercial statistical software which uses maximum likelihood estimation to determine the (2-parameter) Weibull modulus and characteristic strength of each set. 95% confidence ratio rings were determined for each set and were used to compare data sets.

Optical microscopy was used to identify the failure locations of all the specimens. Scanning electron microscopy was used with a select few specimens to examine the edge and surface qualities of the chips.

Results and Discussion

The 3-pt strength distributions for the Si chips are shown in Fig. 9. There were two surface conditions for the Si (lapped and polished) and two crystallographically aligned orientations with the chip's edges (<112> and <110> directions), so there were four combinations tested with the 3-pt bending. The <112> lapped set had the lowest characteristic strength among the four while the <112> polished set exhibited the least amount of scatter (as represented by a higher Weibull modulus). The characteristic strengths of both polished orientations were equivalent.

Optical microscopy showed that failure initiation with the 3-pt bend specimens occurred on the surfaces (and not the edges) of the lapped Si chips but that initiation occurred at edges of the polished Si chips.

Examples of chipping along edges on the lapped and polished surfaces are illustrated in Figs. 10-11. Edge chipping on the two crystallographic directions (Fig. 10) was not noticeably different and that is probably why their characteristic strengths were equivalent. However, the edge chipping on the edges bordering the lapped surface was was much more severe (Fig. 11); however, the surface-located flaws inherent to the lapped surface were still more dominant in limiting strength than these severe edge-type flaws.

When a component is mechanically confined and concurrently subjected to a thermal gradient through its thickness (i.e., such as these chips during service), then higher tensile stresses will occur on the colder side. For an attached chip subjected to cooling, the lapped side of the chip will be that colder side. How may the results in Fig. 8 be interpreted in context with this? If an attached chip is subjected to a uniform biaxial tensile stress, then (Mode I) failure initiation is more likely to occur perpendicular to the weakest direction <112> and away from the edge. From a design perspective, if a rectangular chip could be used instead of a square chip (but with the same area or edge length), then a rectangular chip whose longer axis is parallel to <110> will have a higher probability of survival (all other things being equal).

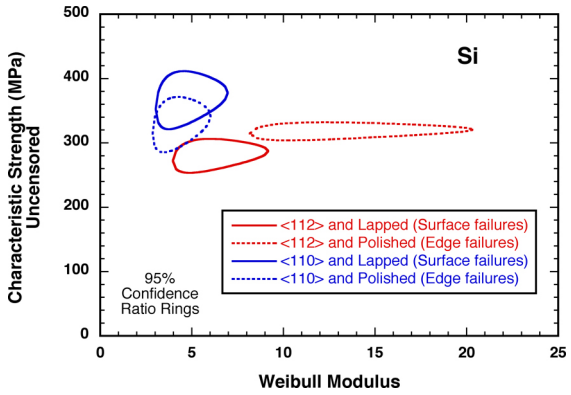

Figure 9. A Weibull strength distribution for the four combinations of 3-pt-bend test sets on the Si chips. 95% confidence ratio rings shown.

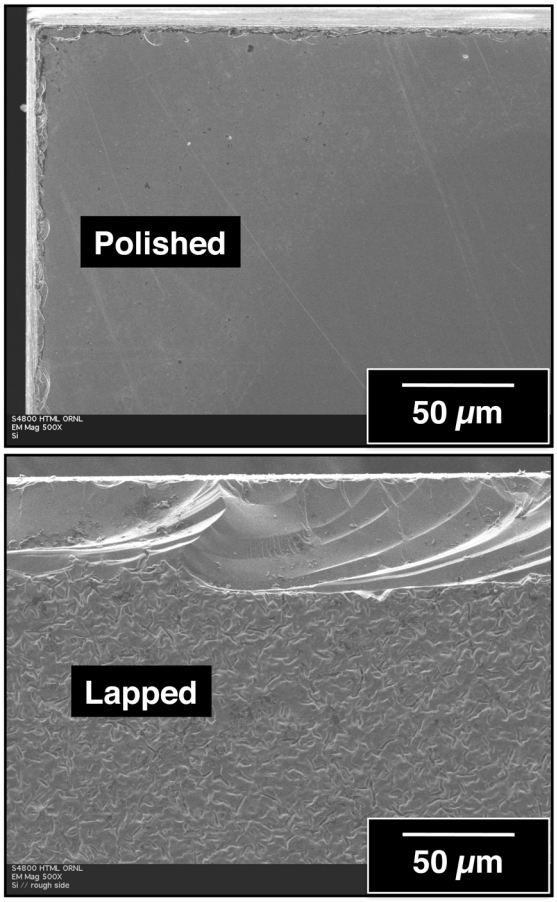

Figure 10. Representative edge chipping and comparison of polished and lapped surfaces on a Si chip.

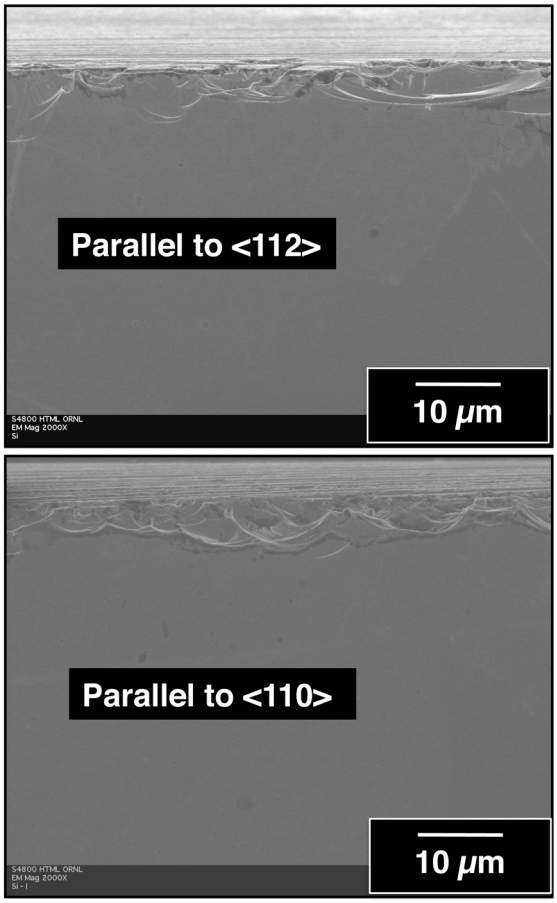

Figure 11. Representative edge chipping and comparison of polished surfaces on edges parallel to <112> and <110> directions on a Si chip.

The 3-pt failure stress distributions for the two SiC chips are shown in Fig. 12. The two surfaces of the SiC chips were both polished so only crystallographic orientation effects were examined. While the characteristic strengths of all the SiC chips were approximately an order of magnitude larger than those for the Si chips, the characteristic strength of the SiC chips tensile stressed perpendicular to <112bar0> were stronger than those stressed parallel to that direction. Additionally, the failure initiation of all SiC chips occurred at their edges. This shows that surface polishing removes (or minimizes the effects of) surface-type strength-limiting flaws and that translates into failure initiation at the edges.

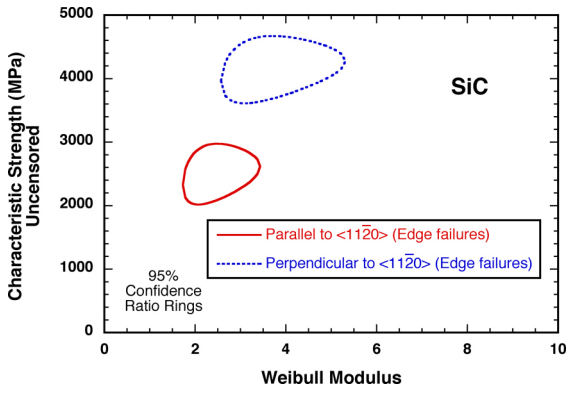

Figure 12. A Weibull strength distribution for the two combinations of 3-pt-bend test sets on the SiC chips (both sides were polished). 95% confidence ratio rings shown.

The significantly higher characteristic strength of the SiC chips compared to the Si chips is likely a consequence of the difference in the quality of the edge slicing. Examples of edge chipping on the SiC chips are shown in Fig. 13. The chipping is much smaller in stature than the chipping in the Si chips (compare with Figs 10-11). Given these differences in edge quality, one could conclude that the differences in characteristic strength are due to differences in these extrinsic type of strength-limiting flaws and not differences in intrinsic or bulk material differences.

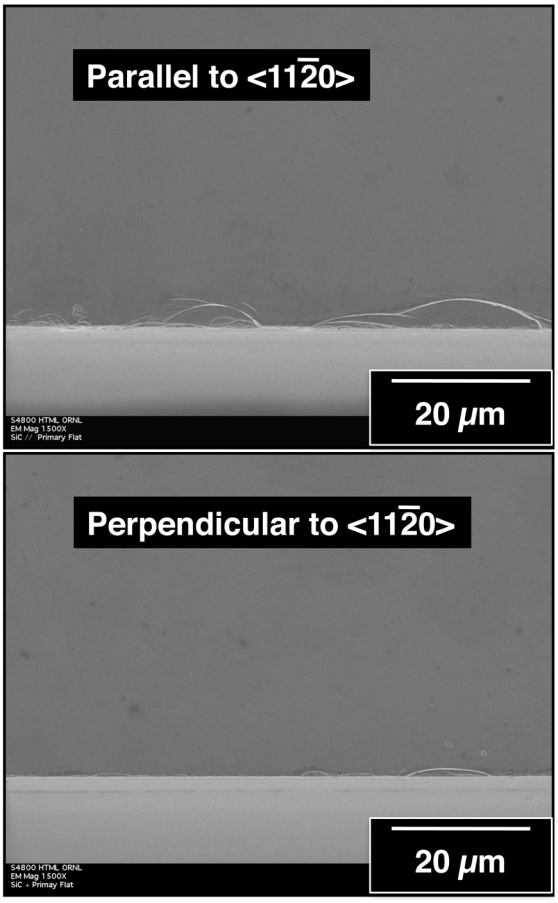

Figure 13. Representative edge chipping and comparison of polished surfaces on edges parallel and perpendicular to <1120> direction on a SiC chip.

The anticlastic bending characteristic strength of the SiC chips was almost an order of magnitude larger than that for the Si chips as shown in Fig. 14. Failure initiation with the SiC chips occurred at an edge whereas failure initiation with the Si chips occurred away from the edge. In fact, optical fractography showed that failure initiation with the Si chips routinely occurred on the lapped surface directly opposite (or under) where one of the two balls was making contact with the polished surface.

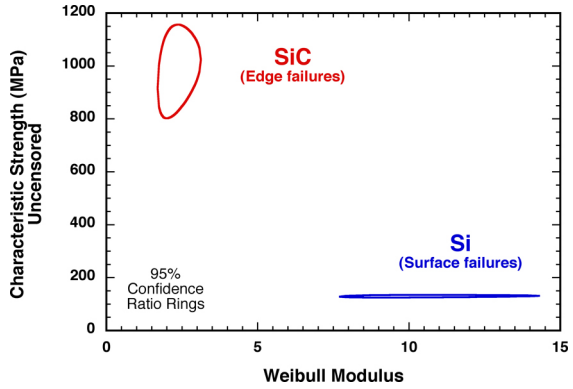

Figure 14. Weibull strength distributions for anticlastic bend test sets. 95% confidence ratio rings shown.

Anticlastic bending tensile stresses operate over greater total lengths of chip edges than 3-point bending does, and because of that, its specimens fail at lower failure stresses when surface type-flaws are not operative (i.e., in the case of the SiC chips). The anticlastic failure stress for SiC chips was approximately one-third that of the 3-pt bend characteristic stresses. For more confident design and mechanical reliability analysis, it is always advantageous to have failure stress data from test coupons that sample (or tensile stress) as much material as possible. Therefore, anticlastic bending can be an effective test method for evaluating edge failure stress in semiconductor chips if surface-type strength-limiting flaws are not dominant.

Conclusions

Extrinsic strength-limiting flaws located at their edges and on lapped surfaces limit tensile stress tolerance of Si and SiC chips. And that tensile stress tolerance exhibits size scaling. Namely, failure stress is lower with longer (effective) edge lengths and with larger (effective) areas. This is consistent with the established utilization of censored Weibull tensile

strength distributions for the design and mechanical reliability estimation of brittle material components.

Anticlastic bending tensile stresses much greater lengths of chip edges than 3-point bending does, and because of that, this specimens fails at lower failure stress when surface type-flaws are not operative. For more confident design and mechanical reliability analysis, it is always advantageous to have failure stress data from test coupons that sample (or tensile stress) as much material as possible. Therefore, anticlastic bending can be an effective test method for evaluating edge failure stress in semiconductor chips if surface-type strength-limiting flaws are not dominant.

Edge-strength anisotropy was observed with both the Si and SiC. This suggests that if non-square chips are used (e.g., rectangular chips) that there is an advantage to having the longer axis being parallel with the stronger direction.

Surface-strength anisotropy was observed with the Si because one side was lapped and the other polished. The lapped side is weaker. Others have described this effect too. For conservative design or mechanical reliability estimation, the use of the strength distribution measured with the (weaker) lapped should be used.

The SiC chips failed at higher tensile stresses than Si chips; however, that difference may be a ramification of edge slicing differences and not intrinsic material differences.

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