# High Temperature Capacitors Based on [0001] and [1120] Sapphire Dielectrics

Liang-Yu Chen
Ohio Aerospace Institute (OAI)/NASA Glenn Research Center, Cleveland, Ohio 44135
Tel: (216) 433-6458, Email: Liangyu.Chen-1@nasa.gov

### Abstract

The test results of the dielectric properties of [0001] (C-plane) and [ $11\overline{2}0$ ] (A-plane) sapphire (single crystalline  $Al_2O_3$ ) at high temperatures indicate that these materials have very stable dielectric constants and low dielectric losses (compared with polycrystalline alumina) at low frequencies in the temperature range from room temperature to  $550^{\circ}$ C. Therefore, sapphire materials have become likely candidate dielectric materials for high temperature capacitors. This paper reports prototype low-volume ( $\sim 100 pF$ ) capacitors based on sapphire dielectrics for high temperature and low frequency applications.

Low-volume parallel-plate capacitors using C-plane and A-plane sapphire as dielectric material were fabricated by stacking metallized sapphire substrates. These prototype capacitors were characterized in the temperature range from room temperature to 550°C by measuring the capacitance and parallel resistance of these devices at 120Hz, 1kHz, 10kHz, 100kHz, and 1MHz. The capacitance and equivalent parallel resistance of these capacitors were all directly measured by an AC LCZ impedance meter in controlled temperature environments.

These prototype devices demonstrate stable capacitances over a wide temperature range, and therefore, have the potential to be integrated with silicon carbide (SiC) devices to enable high temperature electronics. The needs of thin-film metallization and encapsulation for these sapphire substrates are also discussed.

Keyword: Capacitor, sapphire, high temperature.

#### 1. Introduction

Capacitors operable at temperatures up to 500°C are key passive components needed for SiC high temperature electronic systems. The major challenge for high temperature capacitor technology is finding a dielectric with low dielectric loss and stable dielectric constant over both a wide frequency range and the entire operating temperature range. Polycrystalline aluminum oxides (Al<sub>2</sub>O<sub>3</sub>) are low cost dielectrics with desirable characteristics of excellent physical and chemical stability, and high electrical resistivity. These materials have been used widely as packaging substrates for conventional electronics, and proposed for high temperature electronics packaging as well [1, 2, 3]. Various thin-film and thick-film metallization schemes have been developed for aluminum oxide substrates. However, previous test results show that the dielectric properties of most polycrystalline alumina (ceramic) substrates have significant frequency and temperature dependent dielectric constants [4]. At low frequencies the dielectric constants of these materials increase rapidly with temperature. And at high temperature and low frequencies the dielectric loss of these materials is also high. Preliminary test results of [1120] (A-plane) single crystalline aluminum oxide, sapphire, show excellent dielectric properties in a temperature range up to 550°C [5] indicating possible use of sapphire as the dielectric for high temperature

capacitors. This paper reports the detailed dielectric properties including dielectric constant, electrical conductivity, and quality factor/dissipation factor of both A-plane and [0001] (C-plane) sapphire from 120Hz to 1MHz in a temperature range from room temperature to 500°C. Prototype low volume capacitors were fabricated by stacking metalized sapphire substrates. These capacitors were characterized from room temperature up to 550°C at 120 Hz, 1 kHz, 10 kHz, 100 kHz, and 1 MHz.

#### 2. Experimental Details

Sapphire substrates used for measurements of dielectric properties are finely grounded 6.6 cm x 6.6 cm x 0.3937 mm (2.6 inch x 2.6 inch x 15 mil) substrates with crystal orientation of A-plane ±2°, and 5.08 cm x5.08 cm x 0.3937 (2.0 inch x 2.0 inch x 15 mil) substrate with crystal orientation of C-plane. The total atomic impurity of these materials is less than 22.2 ppm. The surface roughness of the sapphire substrates was less than 0.8 µm (32 micro-inch) (rms). The DC resistivity of these materials is  $10^{14}$  Ohm-cm [6]. A parallel plate capacitive device for measuring temperature dependent dielectric properties of each kind of sapphire substrate was fabricated with gold (Au) thick-film metallization (used as the two electrodes) on both sides of the substrate. electrode/metallization areas for A-plane sapphire were

5.08 cm x 5.08 cm (2.0 in. x 2.0 in.) and located at the center region of the substrate, as shown in Figure 1. The electrode/metallization areas for C-plane sapphire substrate were 4.06 cm x 4.06 cm (1.6 in. x 1.6 in.). Au thick-film material was painted, and cured at 850°C in air. Au wires were bonded onto the Au electrodes (metallization) to electrically connect the capacitive device with measuring instruments via 1 m long coaxial cables [4]. The capacitive devices were thermally soaked in a box oven in which the temperature was controlled to an accuracy of ±2°C during the experiment. Prior to data acquisition, the capacitive device was first heated in 550°C air ambient for 12 hours. The AC impedance of the sapphire capacitive devices was measured by an AC LCZ meter with (1 V rms) sinusoidal voltage at frequency f = 120 Hz, 1 kHz, 10 kHz, 100 kHz, and 1 MHz. The measured capacitances (or dielectric constants) were quite stable and reproducible after the initial 12-hour anneal at 500°C. The dielectric constant and parallel conductance were calculated from the impedance data.

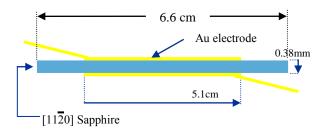
Prototype low volume capacitors were fabricated by stacking multiple layers of metallized sapphire substrates with dimensions of 2 cm x 2 cm x 15 mil. A cross-section of the structure of these capacitors is shown in Figure 2. 10 mil Au wires were attached to the edges of Au metallizations for electrical connections. The capacitor with A-plane sapphire was composed of three layers of metallized sapphire substrates, and the C-plane sapphire capacitor was composed of four layers of metallized sapphire. The metallized substrates were bonded together through (Au) diffusion achieved by heating at 850°C for 20 minutes.

The experimental details of characterization of these capacitors are the same as that for characterization of sapphire materials.

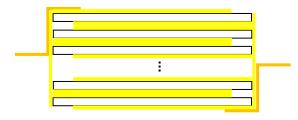
#### 3. Results and Discussion

# 3.1 Dielectric Properties of Sapphires

The upper graph of Figure 3 shows the plots of the relative dielectric constant, of the C-plane sapphire versus frequency at various temperatures. At room temperature, the dielectric constant is ~11.75 at 1MHz. Dielectric constant changes slightly with frequency at all temperatures. At 550°C, it is in a narrow envelop from 12.7 to 12.8. The dielectric constant of C-plane sapphire changes less than 10.4% in the frequency range between room temperature and 550°C. The lower graph of Figure 3 shows the plots of the relative dielectric constant, of the A-plane sapphire versus frequency at various temperatures. At room temperature, the dielectric constant is ~9.23 at 1MHz. Dielectric constant changes slightly with frequency at



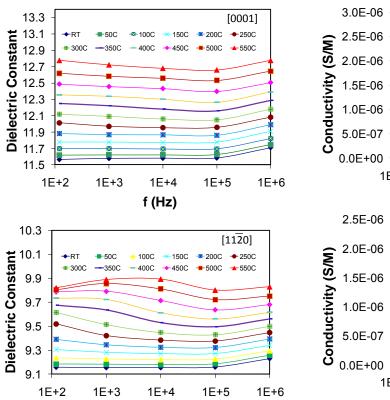
**Figure 1**: Schematic of parallel plate capacitor for measurement of dielectric properties of sapphire substrates. Dimensions shown are for [1120] (Aplane) sapphire substrate.



**Figure 2**: Schematic of prototype sapphire capacitors fabricated by stacking metallized sapphire substrates.

all temperatures. At 550°C, it is in a narrow envelope from 9.8 to 9.89. The dielectric constant of A-plane sapphire changes less than 7.5% in the frequency range between room temperature and 550°C. Compared with the dielectric constants of polycrystalline (ceramic) aluminum oxide substrates, the dielectric constants of sapphire materials are much more stable with temperature. The dielectric constant of C-plane sapphire is higher than A-plane sapphire, but it also changes slightly more with temperature than that of A-plane sapphire.

Figure 4 shows the frequency dependence of conductivity of C-plane and A-plane sapphire substrates. At the low frequency end, the conductivities of both materials are too low to be measured by the impedance meter at room temperature and 100°C. At 550°C and 1 MHz, the conductivity of both C-plane and A-plane sapphire substrates is ~2.5·E-06 S/m, the highest for both materials in the entire temperature and frequency ranges. This highest conductivity is about an order of magnitude lower compared with the conductance of the 96% alumina previously tested [4, The conductivity increases with frequency monotonically and dramatically, for both materials, indicating that it is mainly contributed from AC dielectric loss rather than current DC leakage. Overall, the conductivity of C-plane sapphire is close to that of A-plane sapphire.



**Figure 3:** Relative dielectric constant of [0001] (C-plane) and [1120] (A-plane) sapphires vs. frequency at various temperatures.

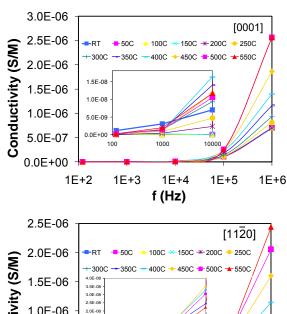
f (Hz)

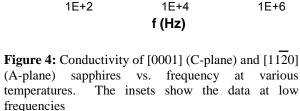
Figure 5 shows the frequency dependent dissipation factor (1/*Q*, *Q* is the quality factor) at various temperatures. For polycrystalline alumina substrates, the dissipation factor basically increases with temperature monotonically and rapidly above 50°C [1]. However, the dissipation factor of C-plane and A-plane sapphire substrate does not simply increase monotonically with temperature as shown in Figure 5. The dissipation factor of C-plane sapphire is less than 0.004, and that of A-plane sapphire is less than 0.0075, in the entire temperature and frequency ranges. Compared with polycrystalline (ceramic) aluminum oxide substrates, the dissipation factor of sapphire materials is about two to three orders of magnitude lower in the same temperature and frequency ranges.

Both sapphire substrates have stable dielectric constant and low dielectric loss in a wide temperature range indicating they are excellent dielectric materials for high temperature application.

# 3.2 Prototype Capacitors

Figure 6 shows the capacitance, resistance, and the ratio between the resistance and capacitive

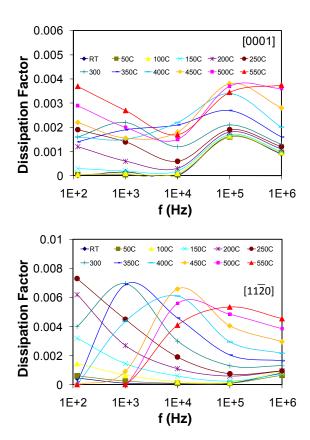




impedance of a C-plane sapphire based capacitor at various frequencies and temperatures. As shown in the top graph of Figure 6, at a constant temperature, the capacitance changes less than 3% with frequency between 120Hz and 1MHz.

The capacitance increases with temperature monotonically, the capacitance changes less than 13.5% with temperature between room temperature and 550°C. As shown in the middle graph of Figure 6, the resistance decreases monotonically with frequency, as well as with temperature. The resistance reaches 1 M $\Omega$  at 550°C and 100 kHz. At 550°C and 1 MHz, it is 140 k $\Omega$ . Even though the resistance at high frequency and high temperature is relatively low, the ratio between the resistance and the capacitive impedance, R $\omega$ C, remains above 85 at frequencies above 1 kHz in the entire tested temperature range, as shown in the bottom graph of the Figure 6. At 120Hz and 550°C, the ratio at its lowest is 65.

The capacitance, resistance, and the ratio between the resistance and capacitive impedance of an A-plane sapphire based capacitor, at various frequencies and

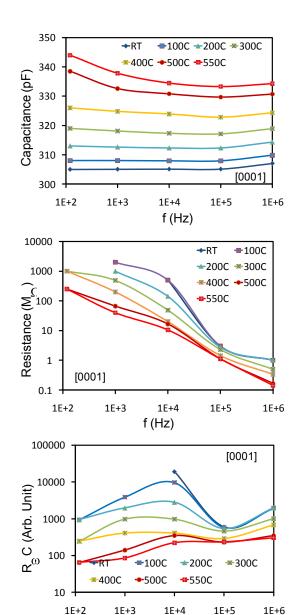


**Figure 5:** The measured\_dissipation factors of [0001] (C-plane) and [1120] (A-plane) sapphire substrates vs. frequency between room temperature and 550°C.

temperatures, are shown in Figure 7 f. At a constant temperature, the capacitance changes less than 4% with frequency between 120Hz and 1MHz, as shown in the top graph of Figure 7. The capacitance increases with temperature monotonically, the capacitance changes less than 11% with temperature between room temperature and 550°C in the entire frequency range. As shown in the middle graph of Figure 7, the resistance decreases monotonically with frequency, as well as with temperature but not monotonically. It reaches  $0.91~\text{M}\Omega$  at  $550^{\circ}\text{C}$  and 100~kHz. At  $550^{\circ}\text{C}$  and 1 MHz, it is  $\sim 125 \text{k}\Omega$ . Even though the resistance at high frequency and high temperature is low, the ratio between the resistance and the capacitive impedance is above 82 in the entire temperature range, as shown in the bottom graph of Figure 7.

# 4. Discussion

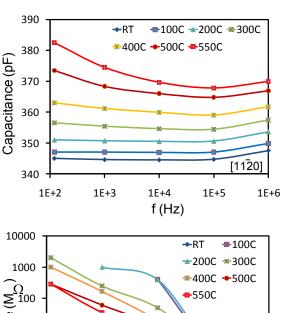
The parallel resistances of these sapphire capacitors, at high temperatures, are relatively high compared with those estimated from the dielectric properties measured for C-plane and A-plane sapphire

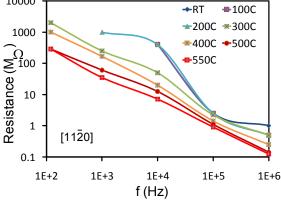


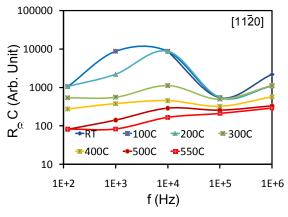
**Figure 6:** Electrical parameters of [0001] (C-plane sapphire based capacitor: The frequency dependen capacitance (top), resistance (middle), and ratio betweer the resistance and capacitive impedance (bottom) vs frequency, from room temperature to 550°C. The device was not passivated.

f (Hz)

substrates. Most likely this is attributed to possible surface conduction resulting from the narrower blank sapphire surfaces surrounding the metallization areas. Effective surface passivation may further improve the dielectric performance of these capacitors at high temperature. However, finding an insulator that outperforms sapphire at high temperatures is a challenging topic.







**Figure 7:** Electrical parameters of  $[11\overline{20}]$  (A-plane) sapphire based capacitor: The frequency dependent capacitance (top), resistance (middle), and ratio between the resistance and capacitive impedance (bottom) vs. frequency, from room temperature to  $550^{\circ}$ C. The device was not passivated.

Using thinner sapphire substrates is necessary in order to achieve higher volume (~1000pF) sapphire capacitors. This would require using thin-film metallization instead of thick-film metallization. The binder in the thick-film metallization may interfere with

the overall dielectric performance of the metal/sapphire/metal structure at high temperatures when the sapphire dielectric becomes much thinner. Platinum (Pt) and Au thin-films, ~5000Å, have been tested on finely ground sapphire surfaces. After heat treatment at 500°C for over hundreds of hours, it was observed that these thin-film coatings became non-uniform and the surface coverage of these thin-films on substrates decreased indicating that these thin-film materials do not sufficiently wet the sapphire surface at high temperatures. Metallization schemes remain a research topic to largely improve capacitance volume.

# 5. Summary

The dielectric properties of both C-plane and Aplane sapphire substrates have been measured at temperatures up to 550°C at 120 Hz, 1 kHz, 10 kHz, 100 kHz, and 1 MHz. The results indicate that these sapphire materials have stable dielectric constants in the tested temperature range. The dielectric constant of Cplane and A-plane sapphire changes less than 10.7% and 8%, respectively, in the tested temperature and frequency ranges. Conductivities of both C-plane and A-plane sapphire substrates increase with frequency, they are  $\sim 2.5 \cdot \text{E-6 S/m}$  at 550°C and 1MHz. In the entire tested temperature and frequency ranges, the dissipation factor of C-plane sapphire is less than 0.004, and dissipation factor of A-plane sapphire is less than Sapphire with relatively stable dielectric constants and low dielectric loss are candidate dielectrics for high temperature applications.

Low volume prototype C-plane and A-plane sapphire dielectric based capacitors were demonstrated for high temperature applications. These prototype capacitors were fabricated by stacking Au metallized sapphire substrates through high temperature (Au) These capacitors were electrically diffusion. characterized from room temperature up to 550°C at 120Hz, 1kHz, 10kHz, 100kHz, and 1 MHz. capacitance of C-plane sapphire capacitor changes less than 13.5% in the entire tested temperature and frequency ranges, while the capacitance of A-plane sapphire based capacitor changes less than 8% in the entire tested temperature and frequency ranges. Even though the parallel resistances of these capacitors are relatively low at high temperature and high frequency, the ratios of the parallel resistance and capacitive impedance of C-plane and A-plane sapphire capacitors remain above 65 and 82, respectively.

The metallization scheme for the sapphire surface needs to be further developed to largely increase the capacitance volume of sapphire based capacitors. A high temperature durable thin-film metallization for sapphire surfaces is especially critical to cover the capacitance range up to ~ 1000pF. A

passivation material suitable to sapphire substrate and operation at high temperatures is also important to make these capacitors more durable, and eventually to commercialize sapphire capacitors.

## Acknowledgements

The author thanks Drs. Lawrence G. Matus, Carl Chang, Mary V. Zeller for proofreading the manuscript. This work is supported by the NASA Integrated Vehicle Health Monitoring (IVHM) project of Aviation Safety program under NASA ARA grant NNC07ZA11A monitored by Dr. Gary W. Hunter.

#### References

- 1. F.P. McCluskey, R. Grazybowski, and T. Podlesak, *High Temperature Electronics*, CRC Press, Boca Raton, 1996.
- 2. J.S. Salmon, R. Johnson, and M. Palmer, "Thick Film Hybrid Packaging Techniques for 500°C Operation," in Trans. Fourth Int. High Temperature Electronics Conf. (HiTEC), Albuquerque, NM, June 15-19, 1998.
- 3. L.-Y. Chen and G.W. Hunter, " $Al_2O_3$  and AlN Ceramic Chip-level Packages for  $500^{\circ}$ C Operation," in Proceedings of 2005 European High Temperature Electronics Conference (2005 HiTEN), Paris, France, September 2005.
- 4. L.-Y. Chen, "Temperature Dependent Dielectric Properties of Polycrystalline Aluminum Oxide Substrates with Various Impurities," in Proc. 8<sup>th</sup> International Conference on Electronic Packaging Technology (2007 ICEPT), Shanghai, China, August 14-17, 2007.
- 5. L.-Y. Chen, "Dielectric Properties of [1120] Sapphire at High Temperatures," presented on International Conference on High Temperature Electronics (HiTEC 2008), May 12-15, 2008.
- 6. http://www.crystalsystems.com/sapphys.html
- 7. L.-Y. Chen and G.W. Hunter, "Temperature Dependent Dielectric Properties of Polycrystalline 96% Al<sub>2</sub>O<sub>3</sub> Substrate," Proceedings of Symposium G (Materials, Integration, and Packaging Issues for High-Frequency Devices II), 2004 MRS Fall Meeting, Boston, MA. November 2004.