A 200 °C Quad-Output Buck Type Switched Mode Power Supply IC

Daniel T. Goff[1,2], Steve J. A. Majerus[1,2], and Walter Merrill[1]

1. BluBerry, LLC, Columbia Station, Ohio
2. Case Western Reserve University, Cleveland, OH

Abstract

A high temperature (>200 ˚C), quad-output, buck type switched-mode power supply (SMPS) IC capable of operating over a wide input supply range of 6 V to 15 V is described. The IC is a compact power supply solution for multi-voltage microprocessors, sensors, and actuators. The SMPS topology is a 112 kHz fixed-frequency, synchronous buck converter with slope compensation. A novel internal feedback design enables the output voltages to be pin-programmed to one of three common supply voltages—5 V, 3.3 V, or 1.8 V—while an external resistor divider can also be used for arbitrary voltage programming. Integrated power supply output MOSFET switches minimize the external part count and synchronous rectification reduces power dissipation and improves current capacity. The IC was fabricated in a conventional, low-cost, 0.5 µm bulk CMOS foundry process. Patented circuit design techniques allow the IC to operate in excess of 200 ˚C and circuit operation was demonstrated at ambient temperatures up to 225 ˚C. The foundry process is optimized for 5 V applications, however, the IC accepts input voltages up to 15 V and can produce outputs up to 10 V by utilizing extended drain single- and double-sided NMOS and PMOS transistors for the linear regulator pass transistor, error amplifier, and SMPS switches. The high-side FETs are controlled through capacitive coupled level shift circuits to ensure the gate-oxide voltage limits are not exceeded while still maintaining fast signal transitions. The IC also includes a tunable, 25 MHz monolithic oscillator that is programmable over a SPI serial interface. The oscillator bias current is comprised of a programmable constant-g_m bias current and a programmable PTAT bias current. The programmability can be used to set the oscillation frequency, but can also be used together with a calibration curve on a microcontroller to achieve a more stable oscillation frequency over temperature. The output current of the quad SMPS was limited to 70 mA by a lower than expected saturation current of the extended-drain PMOS switch devices. The system showed good line regulation (<0.1%) and 50% load step response stability (+/- 100 mV) at a nominal output current of 50 mA when tested at 200 ˚C ambient.

Key words: switched mode power supply, buck converter, programmable oscillator, high temperature

I. Introduction

Reliable integrated circuits capable of operating at elevated temperatures are needed to reduce size and improve performance of systems for turbine engine control, down hole well logging and automotive applications. In this paper, we present an analog integrated circuit (IC) design that performs essential power supply functions for measurement and control systems. Called the HHT301, this IC is a quad-output buck type switch mode power supply (SMPS) capable of operating over a wide input supply range and is intended for microprocessor and sensor applications requiring several supply voltages.

The HHT301 quad-output SMPS presented in this paper is one IC in a set of high temperature ICs developed by researchers at CWRU and BluBerry LLC to perform sensing, actuation, and power supply functions essential for a closed loop sensor or actuator system [1]. The other ICs have already been combined into a high temperature actuator controller development system where operation from -55 ˚C to 200 ˚C was demonstrated [2].

II. High-Temperature and High Voltage Integrated Circuit Design

The HHT301 was fabricated in a conventional, 0.5-micron bulk CMOS process. To achieve high performance and stable operation over a wide temperature range, patented circuit design

techniques are used to stabilize gain, operating frequency, and output current. Besides these methods, the circuit architectures have been designed such that their characteristics are dominated by temperature-insensitive factors such as component ratios. Several of these design techniques and the constant-g_m biasing have been described in [2], [3] and [4].

The HHT301 has been designed to operate at ambient temperatures of 200 ˚C, with an expected maximum junction temperature of 250 ˚C. High-reliability IC layout techniques reported in [5] and [6] were used to improve reliability at elevated temperatures.

The low-voltage process used for this design is extended to higher voltage operation (up to 15 V) by using special devices with thick gate oxides and unique geometries. Circuit topologies were chosen to minimize the number of high voltage (HV) nodes required since the conventional low voltage devices offer higher performance and a higher density layout. Figure 1 shows the notation and symbols used in this text for these higher voltage extended drain transistors, where a double bar indicates the extension.

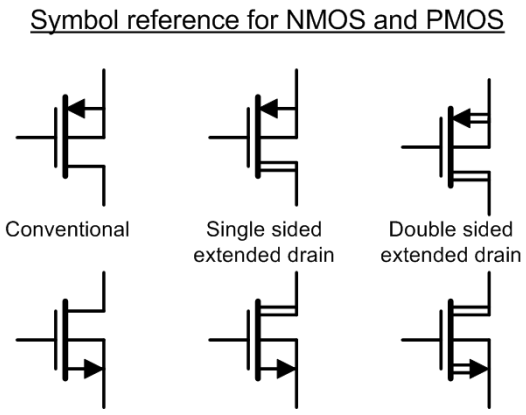

Figure 1: Notation and symbol reference for single- and double-sided extended drain HV MOSFETs.

III. SMPS Circuit Descriptions

HHT301 Quad-Output Buck Type SMPS

The HHT301 block diagram is shown in Figure 2. The IC contains four identical SMPS buck converter cores that each operate independently. A band-gap voltage reference circuit, constant-g_m bias circuit, programmable temperature stable oscillator, PWM ramp generator, and 5 V low dropout (LDO) linear regulator are shared among the four separate cores. Each core includes over-current protection for the output MOSFET switches and local over-temperature protection to prevent device damage.

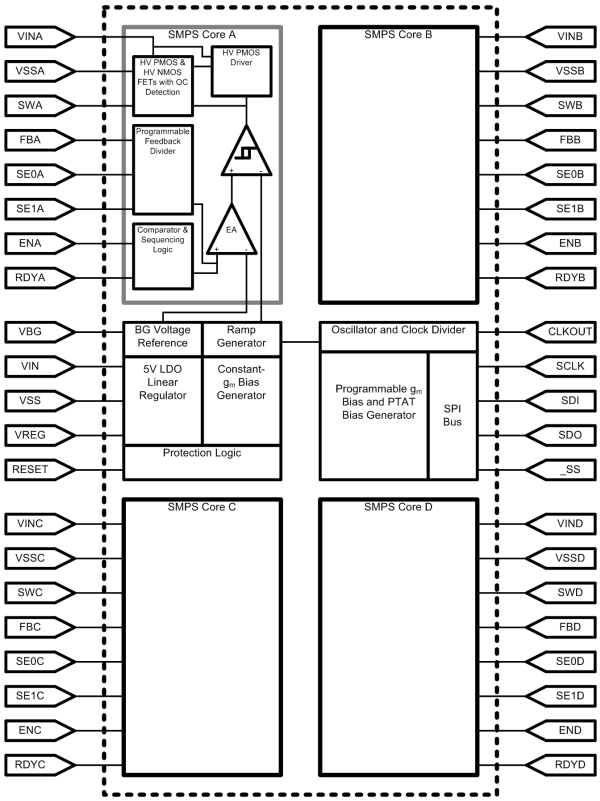

Figure 2: HHT301 block diagram. The HHT301 is a quad-output buck-type SMPS IC intended for high temperature systems that require several supply voltages, low power dissipation, and must accept a wide input voltage range.

Each SMPS core has an "Enable" input and a "Ready" output to facilitate power supply sequencing. This feature reduces node startup current and prevents latch-up in multiple-supply systems. The "Ready" signal is asserted when the SMPS output voltage exceeds 85% of the user-programmed steady state value. The Ready/Enable pins may be connected locally to allow the IC to start without external control.

HV LDO 5 V Linear Regulator

A low dropout (LDO) 5 V linear regulator provides a stable voltage supply for the internal operation of the buck converter logic and control circuits, which were designed using only conventional low voltage devices. The regulator utilizes double-sided extended drain NMOS and PMOS transistors in the error amplifier and a single-sided extended drain PMOS pass transistor so that the entire chip can be powered from the same high voltage supply (up to 15 V) as the SMPS cores.

The basic structure of the regulator is shown in Figure 3. It features a low-load no-buffer topology that allows for stable operation without the need for a large external bypass capacitor [7]. The feedback topology still requires frequency compensation to achieve closed-loop stability, and in this case, stability is achieved by using a Miller-capacitor compensation technique.

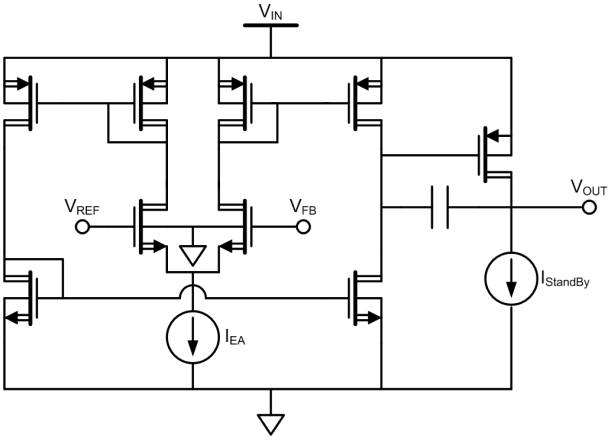

Figure 3: 5V LDO regulator. Double-sided extended drain transistors are used in the error amplifier and a single-sided extended drain PMOS is used for the pass transistor to allow for an input voltage supply up to 15 V in this 5 V 0.5-µm process.

HV -5 V Linear Regulator

To simplify the SMPS control loop compensation, the HV PMOS output devices are always driven with a fixed gate voltage range of V_{IN} to (V_{IN} − 5 V). A negative voltage linear regulator is used to generate this regulated intermediate voltage level that is referenced to V_{IN}. The negative regulator is similar in design to the HV LDO 5 V regulator, except that it utilizes a single-sided extended drain NMOS pass transistor, the error amplifier uses a double-sided extended drain PMOS input, and all the ancillary circuits are referenced to V_{IN} instead of GND.

Capacitive Coupled Level Shift

For the low-side HV NMOS output transistors, conventional CMOS inverter chains that are scaled for greater drive strength are used as gate drivers. However, neither a conventional or HV CMOS inverter chain can be used as a gate driver for the high side power transistors because the CMOS inverters could potentially see voltages greater than the maximum allowable gate to bulk (substrate) voltage (V_{GB}) in the process.

The single-well foundry process biases the bulk connection on all NMOS devices to 0 V, and V_{GB} may never exceed 13 V for the high voltage devices. Therefore, even HV NMOS devices cannot be used in the output PMOS gate driver circuit. Instead, RTL (resistor transistor logic) inverters using only HV PMOS devices are used to drive the PMOS gates in the driver. This approach reduces conversion efficiency, but the circuit does not draw static power when the supply is shut down. The voltage rails for the RTL inverter gate drivers are V_{IN} and the (V_{IN} − 5 V) intermediate supply voltage from the HV -5 V linear regulator.

The logic signals created from the buck converter controller circuits must be level shifted to ensure the signals to the high side HV PMOS power transistor gate drive circuits have the appropriate rails. The gate of the integrated output HV PMOS transistors must be driven from (V_{IN} − 5 V) to V_{IN} in order to turn on and off the device. However, V_{IN} may range from 6V to 15V, while the feedback and control logic operates on 5 V.

A capacitive coupled level shifter was designed to accomplish this control logic voltage to HV PMOS gate drive voltage translation, and is shown in Figure 4. Unlike a typical differential cascade voltage switch logic (DCVSL) level shifter, this

capacitive implementation allows both outputs to change simultaneously while removing the possibility of short circuit current at the switching instant [8].

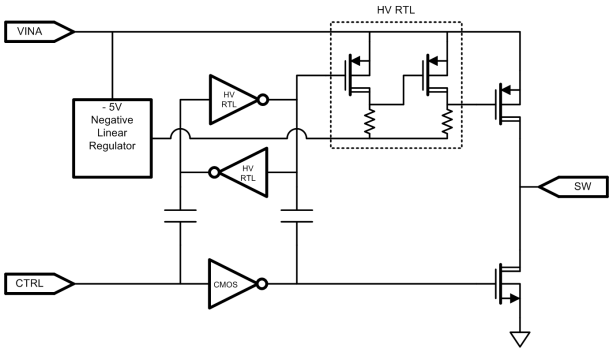

Figure 4: Capacitive coupled level shift circuit. Translates 0 V to 5 V logic signals to levels appropriate for the high-side HV PMOS transistors, V_{IN} to V_{IN} – 5 V.

The signal level voltage shift from logic levels (0 V to 5 V) to HV PMOS drive levels (V_{IN} to V_{IN} – 5 V) is achieved using capacitors and a pair of cross-coupled inverters. When a fast logic transition occurs, the voltage across the capacitors will be maintained (V_{IN} – 5 V). The cross-coupled RTL inverters will toggle their outputs and the output state will be stored. The RTL inverters ensure that logic high is at V_{IN} and logic low is V_{IN} – 5 V. These capacitors are implemented on-chip as poly1-to-poly2 devices.

SMPS Design

The SMPS buck converter core is a 112 kHz fixed-frequency, synchronous buck converter with slope compensation [9]. A voltage-mode control topology is used to minimize external components, reduce design complexity, and to achieve reliable operation at high temperatures. A block diagram of a single SMPS core is shown in Figure 5. The diagram shows how the low voltage control logic circuits and the high voltage circuits are combined to create the SMPS.

This topology uses a scaled version of the output voltage and compares it to an internal band-gap reference to produce the error signal. A voltage ramp is generated on-chip and compared to the error signal to determine the PWM duty factor required for each switch cycle.

A novel mixed-signal feedback divider mechanism enables the output voltage to be pin-programmed to one of three common supply voltages—5 V, 3.3 V, or 1.8 V—with no additional components. A fourth "bypass" option allows

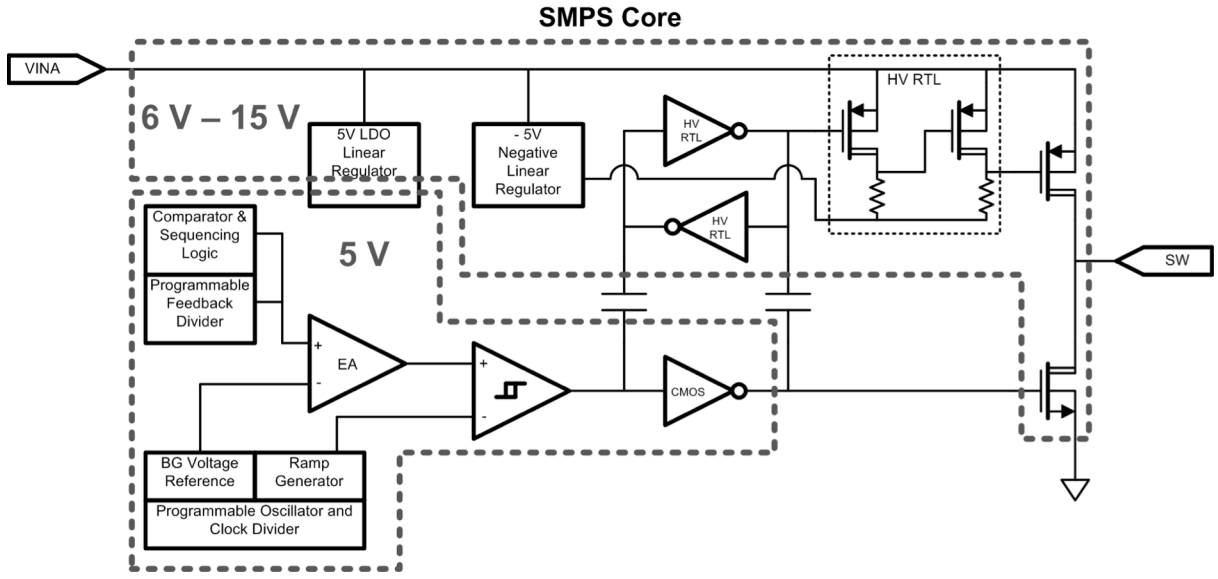

Figure 5: Block diagram of a single SMPS core. The diagram shows how the high voltage positive and negative linear regulators, capacitive level shifter, and SMPS mixed-signal circuits combine to make a complete switched-mode power supply.

other voltages to be set by using an external resistor divider. This feedback mechanism requires no external loop compensation components that are typically required in switching power supplies.

The SMPS core includes the HV output switches on-chip to reduce the external parts count and the synchronous rectification increases switching efficiency and output current capacity.

Tunable 25 MHz Monolithic Oscillator

The on-chip oscillator uses a well-known topology, a 3-stage ring of linear amplifiers depicted in Figure 6. The frequency of oscillation is the frequency at which there is a 60˚ phase shift per amplifier stage, which is determined by a ratio of transconductance (g_m) to capacitance. Capacitance is inherently stable over temperature and g_m is stabilized using our patented biasing technique [10].

In practice, however, the oscillation frequency stability is limited by the temperature coefficient of a resistor in the biasing network [10]. To cancel this resistor temperature coefficient, a programmable bias current that is proportional to absolute temperature (PTAT) and has a temperature coefficient opposite in magnitude to the resistor is injected into the amplifier bias current. The nominal oscillation frequency can also be tuned by varying the programmable constant-g_m amplifier bias current, which allows chip-to-chip variations in oscillation frequency to be removed. Both currents are programmed over an integrated serial peripheral interface (SPI) bus.

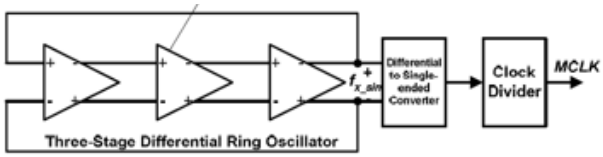

Figure 6: Differential 3-stage ring oscillator

IV. Test Results

The HHT301 was packaged in a 48-pin side-braze ceramic DIP to facilitate high temperature testing. A clamp heater was attached to the DIP package to control the temperature of the IC while all the other components on the test system PWB remained at room temperature. Figure 7shows the clamp heater and system PWB.

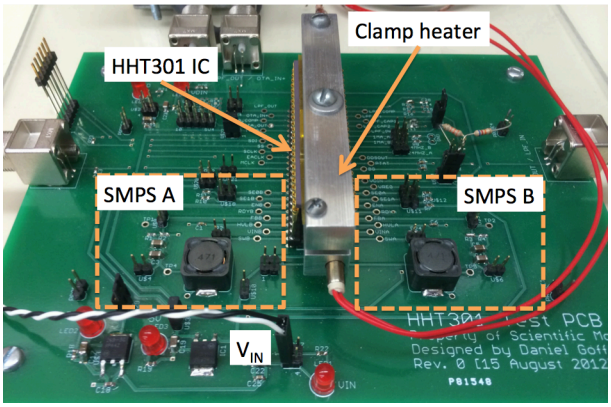

Figure 7: HHT301 high temperature test setup.

The HHT301 IC generally functioned as expected, however, a lower than anticipated saturation current of the single-sided extended drain PMOS transistors used for the high side output switch, limited the maximum output current to only 70 mA. Under that limit it performed well with a fast response to transient loads and very good line regulation.

The output transient response to a 50% increase in load current from a nominal 50 mA is shown in Figure 8. For an output of 5 V, the output transient is less than +/- 100 mV and the recovery time is less than 1 millisecond. Line regulation was measured to be less than 0.1% for the V_{IN} range of 6 – 15 V and across the temperature range of 25 ˚C to 200 ˚C.

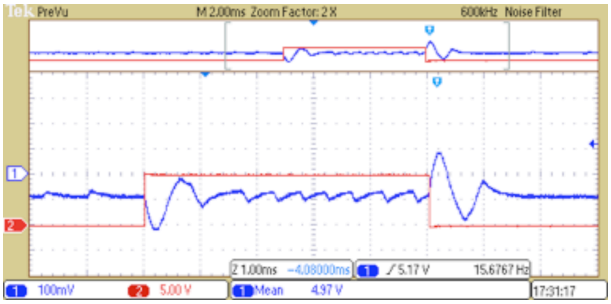

Figure 8: SMPS transient load response for 5 V output, showing 50% load step response stability of +/- 100 mV.

V. CONCLUSION

A quad-output buck type switched mode power supply IC capable of operating at temperatures beyond 200 ˚C has been developed. The system architecture was chosen to allow the operation from wide input voltage range of 6 V to 15 V. Stable operation of the SMPS has been demonstrated over the input voltage range and operating temperature range up to 200 ˚C.

VII. REFERENCES

[1] S. Majerus, D. Howe, S. Garverick, D. Hiscock and W. Merrill, "High-temperature, bulk-CMOS integrated circuits for a distributed FADEC system," in IMAPS Int'l Conf. & Exhibition on High Temperature Electronics (HiTEC 2010), Albuquerque, 2010.

[2] S. Majerus, W. Merrill and S. L. Garverick, "Design and long-term operation of high-temperature, bulk-CMOS integrated circuits for instrumentation and control," in *IEEE EnergyTech 2013*, Cleveland, 2013.

[3] X. Yu and S. L. Garverick, "A 300°C, 110-dB sigma-delta modulator with programmable gain in bulk CMOS," in Custom Integrated Circuits Conference, 2006.

[4] X. Yu and S. Garverick, "Mixed-Signal, 275 C Instrumentation Amplifier in Bulk CMOS," in IEEE Custom Integrated Circuits Conference, 2005.

[5] F. Shoucair, "Design considerations in high temperature analog CMOS integrated circuits," *IEEE Transactions on Components, Hybrids, and Manufacturing Technology,* vol. 9, no. 3, pp. 242-251, 1986.

[6] J. Schroeder, "Latch-up elimination in bulk CMOS LSI circuits," *IEEE Transactions on Nuclear Science,* vol. 27, no. 6, pp. 1735-1738, 1980.

[7] G. Giustolisi, G. Palumbo and E. Spitale, "Robust miller compensation with current amplifiers applied to LDO voltage regulators," in IEEE Transactions on Circuits and Systems, vol. 59, no. 9, pp. 1880-1893, 2012

[8] S. Bandyopadhyay, Y. K. Ramadass and A. P. Chandrakasan, "20 µA to 100 mA DC-DC converter with 2.8-4.2 V battery supply for portable applications in 45 nm CMOS," in *IEEE Journal of Solid-State Circuits,* vol. 46, no. 12, pp. 2807-2820, 2011

[9] Unitrode (now Texas Instruments), "DN-62: Switching Power supply topology voltage mode vs. current mode," 1994.

[10] D. Howe, S. Majerus, S. Garverick, W. Merrill and K. Semega, "High-temperature, bulk-CMOS integrated circuits for a distributed FADEC system – performance results," in IMAPS Int'l Conf. & Exhibition on High Temperature Electronics (HiTEC 2012), Albuquerque, 2012.