Development of Passives on Sapphire Backside

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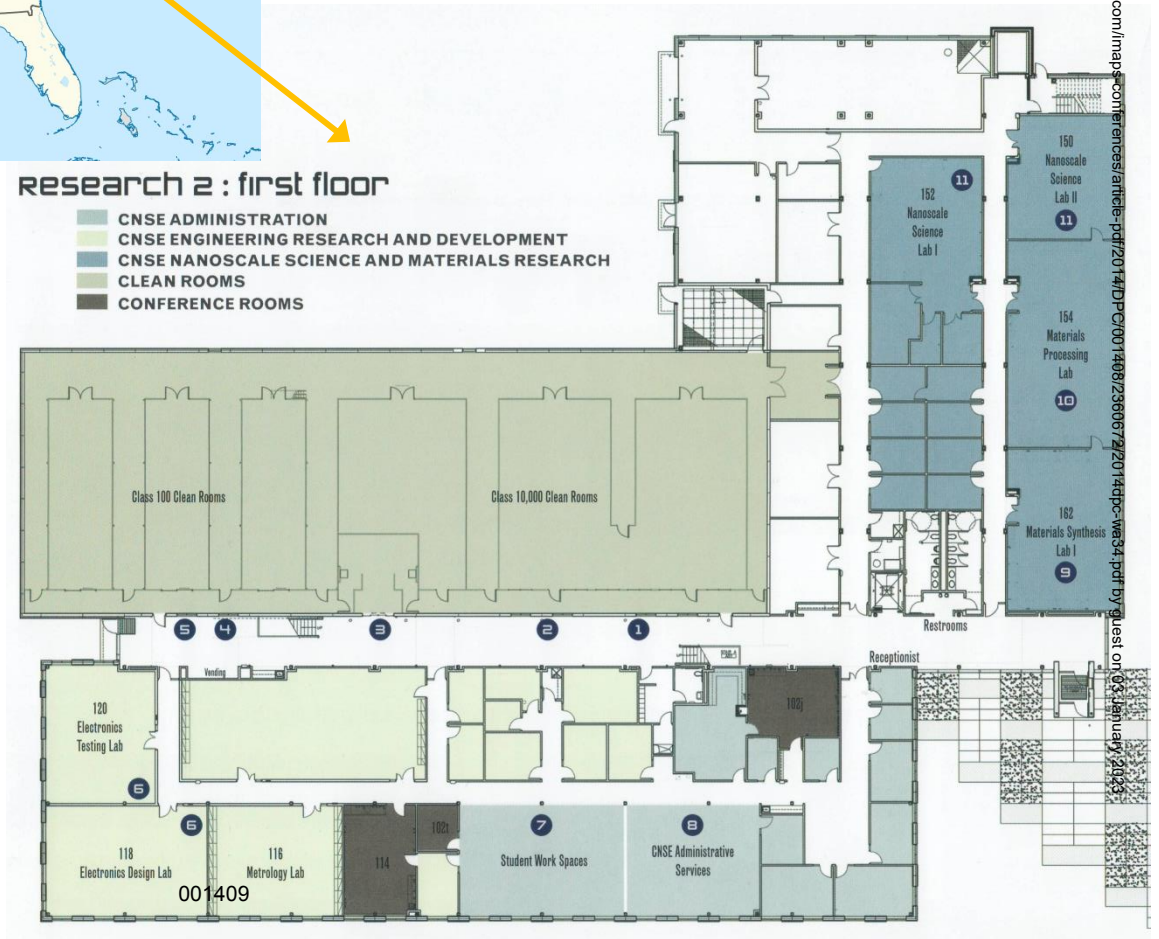
NDSU CENTER FOR NANOSCALE SCIENCE AND ENGINEERING

Micro-Fab, Packaging and SMT Labs

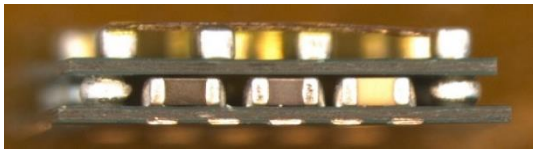
Center for Nanoscale Science and Engineering (CNSE) North Dakota State University (NDSU) at Fargo ND

- CNSE: 75,000 sq. ft. facility
- 3 class 100 cleanrooms (MicroFab): 2,300 sq. ft.
- 3 class 10,000 cleanrooms (Pkgg/SMT): 4,000 sq. ft.
- Staffed by full time trained and experienced employees.
- Service chase, gowning area, etc: 5,850 sq. ft.
- Total 12,150 sq. ft.

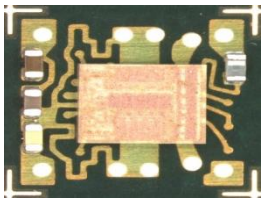


Examples of CNSE/NDSU Packaging/SMT Products

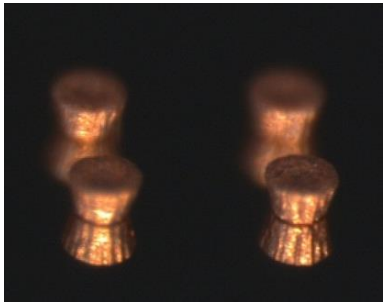
Top Substrate–
Matching Network



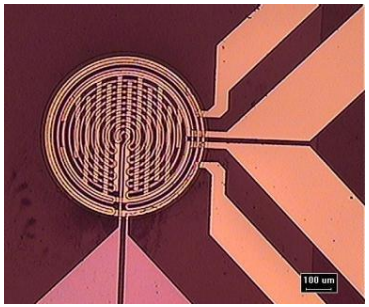
Package-on-Package



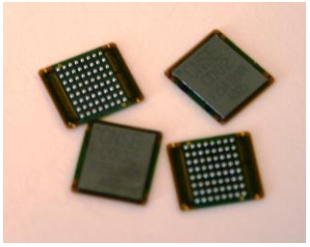
Bottom Substrate–
RF Die



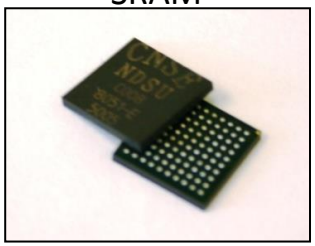
Cu Pillars on Si and sapphire



Micro-Hotplate

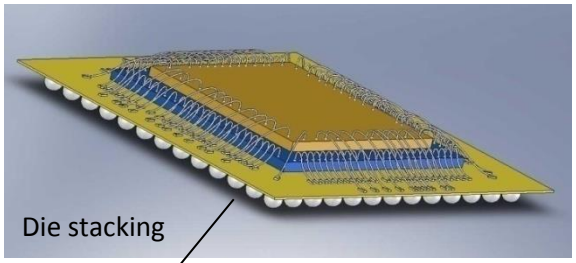


SRAM



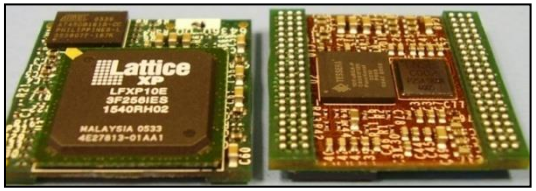
8051 uC

Chip Scale Packages



Dice are extracted from the two packages on right and integrated into the package on left.

3D Package



Digital SiP

Transceiver Module

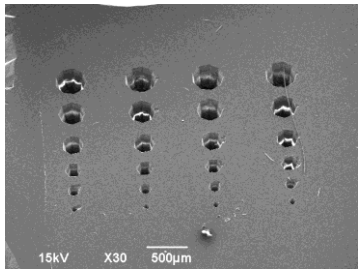
System-in-Package

Sapphire provides unique opportunities for system densification

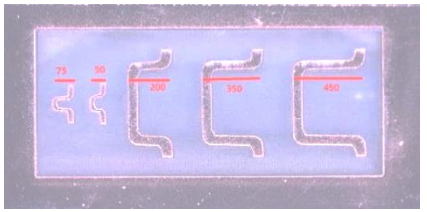
	Sapphire	Silicon
Conductivity	Insulator	Semiconductor
Through Via Insulation	Does not require insulation of through-vias	Requires insulation of through-vias
Backside Insulation	Circuitry on backside will not require insulation	Circuitry on backside will require insulation
Backside Micromachining	Laser can be used for sapphire micromachining	Wet processes are necessary for the silicon which are slow and hazardous
Laser-Via Cleaning	Laser vias are clean	Silicon's crystal structure necessitates laser-vias cleaning
Laser-Via Wall Condition	Sapphire micromachining yields clean even cuts	Crystal structure renders laser- cut features raggedy after cleaning

Electronics Applications of Sapphire Micromachining

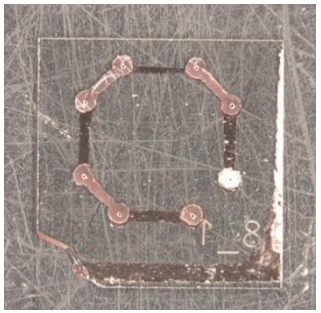
- Through-sapphire vias for
  - Chip stacking
  - Wafer stacking
  - Interconnect to circuitry or components on the backside
  - Chip backside interconnect to substrate
- Pockets or trenches for adding passive components to the back of die or wafer.
- Backside grooves for
  - circuitry
  - antennas
  - micro-mixing or dispensing channels for use with nano-materials or liquids.
  - nano-imprinting of inks and other liquids on the backside.
- Laser pattern metal circuitry on back



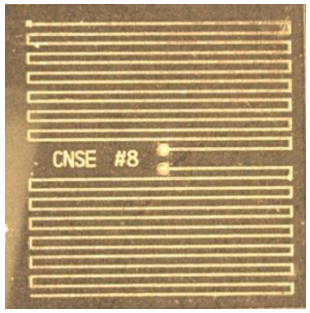
Vias



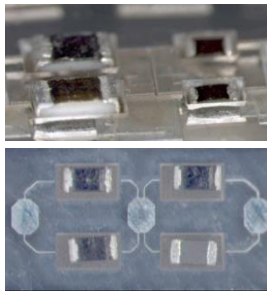
Passives



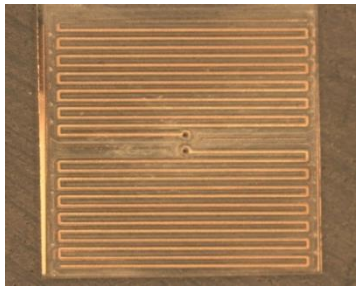
Sapphire through-via interconnect demonstration using daisy chain traces



Pattern produced on the back of sapphire by filling laser etched grooves with conductive ink



Passives in pockets on the back of sapphire

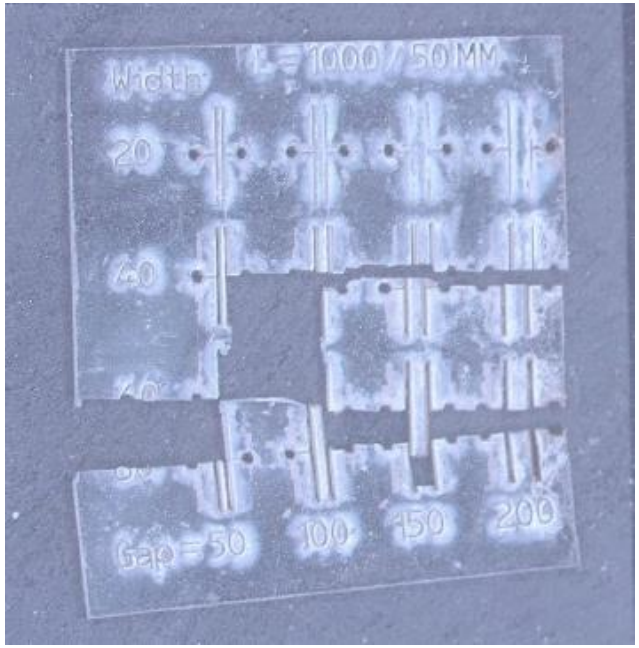


Sputtered metal laser etched to produce a pattern on sapphire

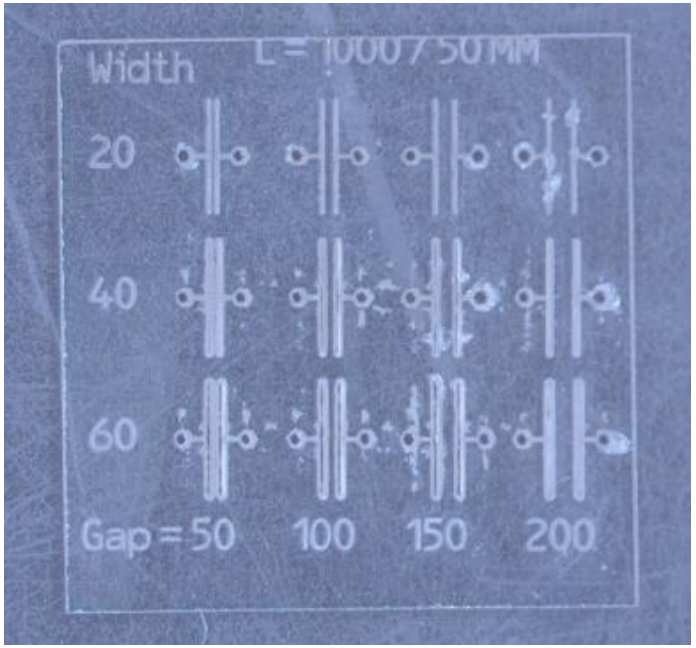
001412

Examples of developments at CNSE/NDSU

Trenches for parallel capacitor



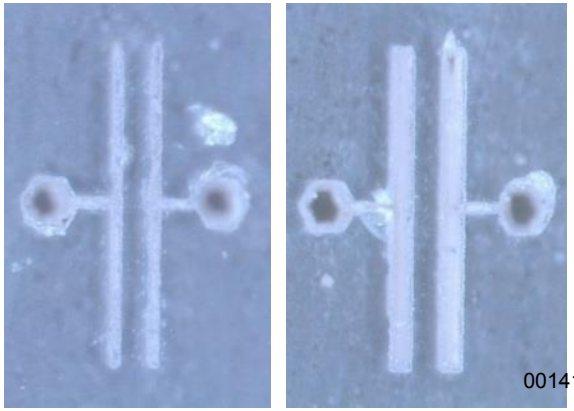
Batch drilling al patterns at once caused chip to crack.



Actual width
26
45
67

Sequential drilling provided better results.

Before Cu sputter



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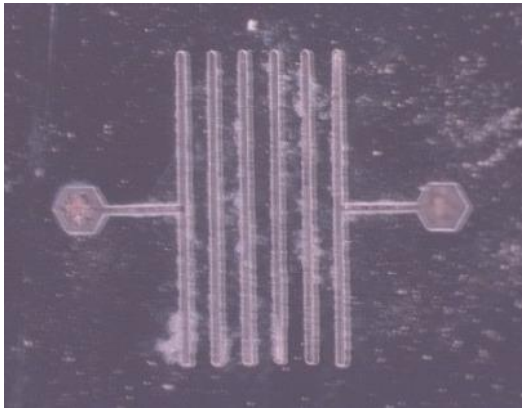
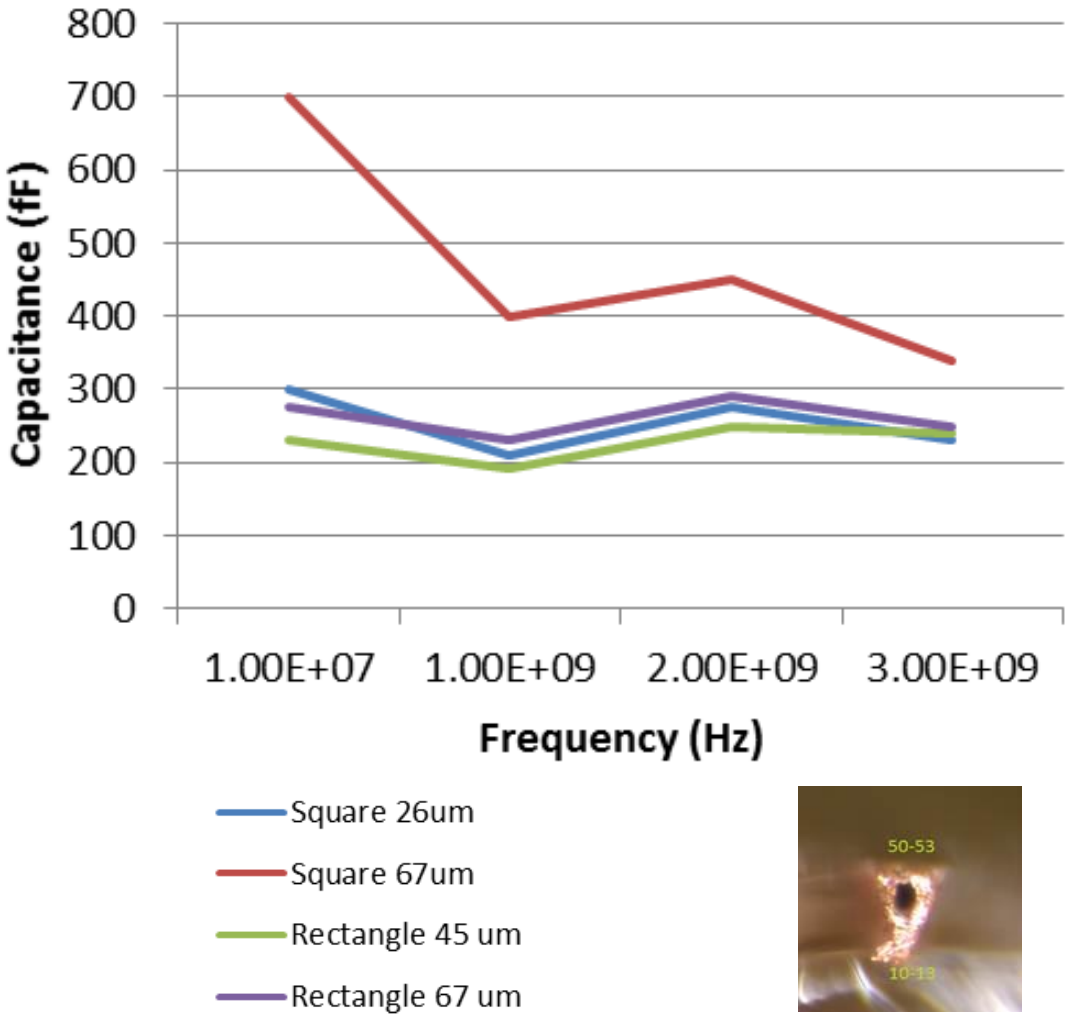


After Cu sputter

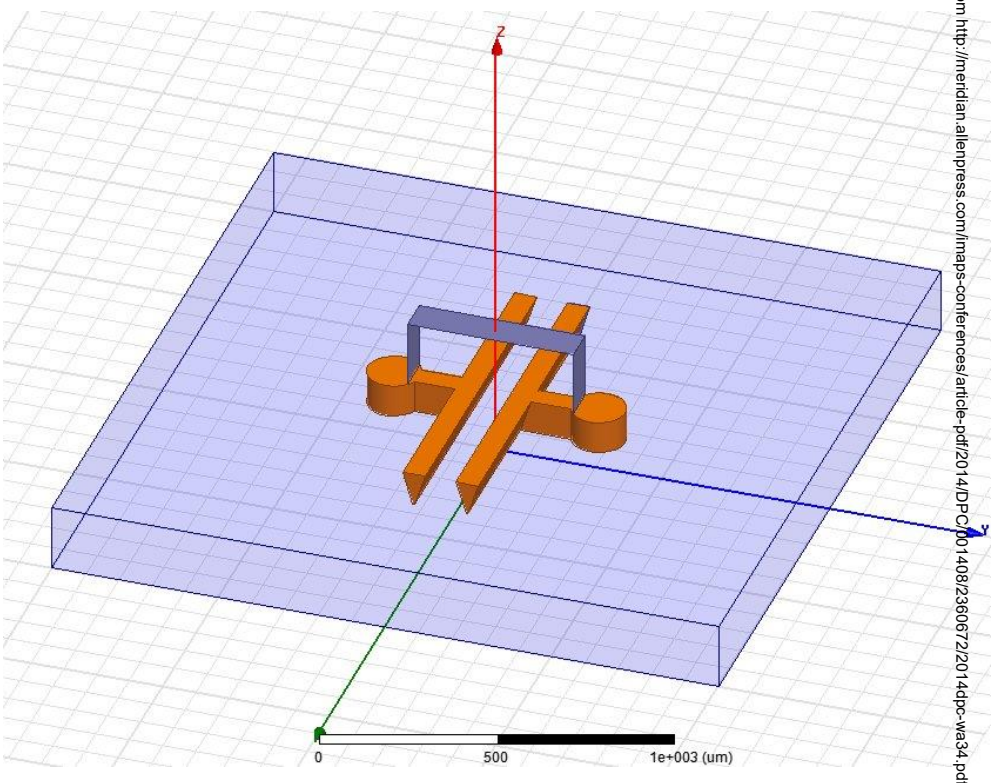
Capacitor fabrication and capacitance measurement

- Capacitor trenches were fabricated with laser.
- Trenches were filled with electroplated Cu on sputtered Cu seed layer.
- Plate widths were approx. 26, 45, and 67 µm at the top.
- Dice were fixed to square and rectangular aluminum blocks.
- Capacitance was measured on a microprobe station with Agilent E4991A impedance analyzer.



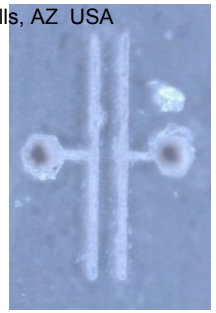
Model preparation

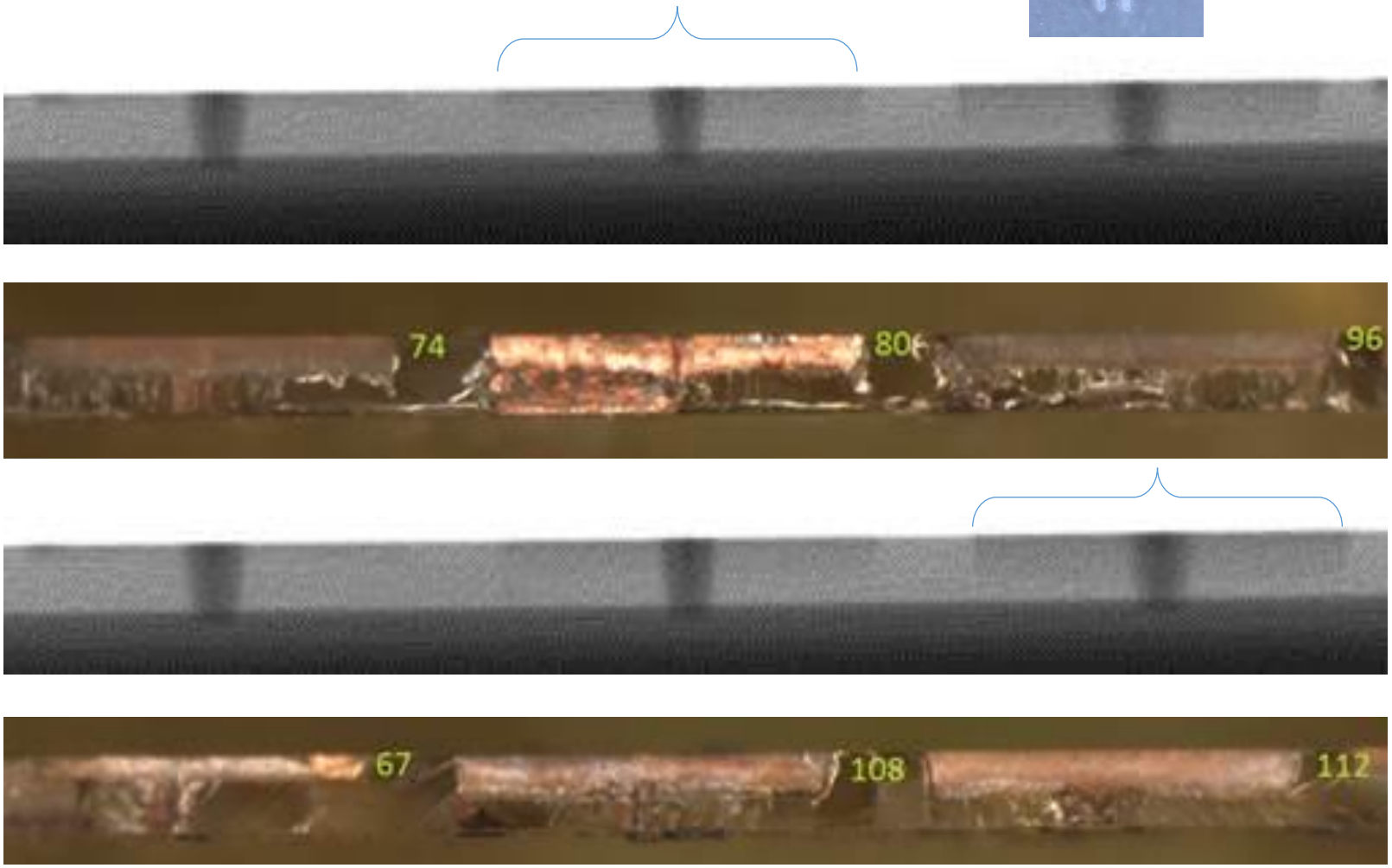
- A model of the parallel plate capacitor was developed in Ansys HFSS.
- The capacitor plate was designed as a trapezoid with the base at the surface being 67 µm wide and the other base, inside the sapphire, was 5 µm wide.
- The grey band going from the pads and above the capacitor is simply a simulation construct to measure the capacitance between the measurement points.



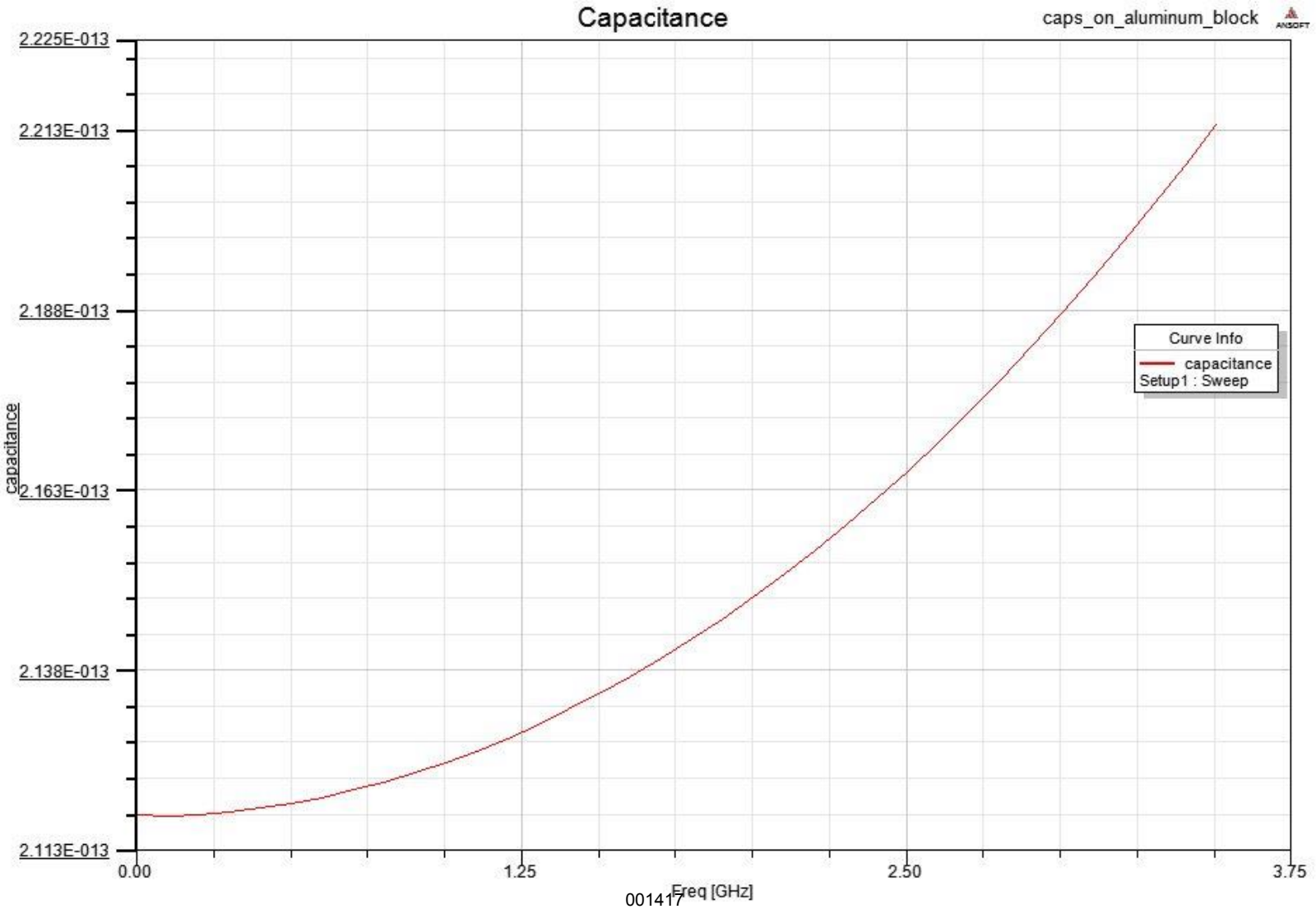
Ansys HFSS model of parallel plate capacitor

Cross-sections to measure actual dimensions for modeling (side views)





Modeled capacitance

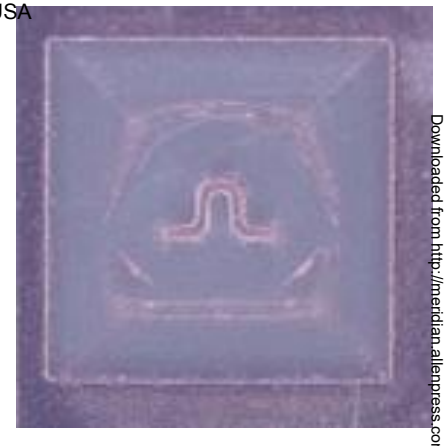


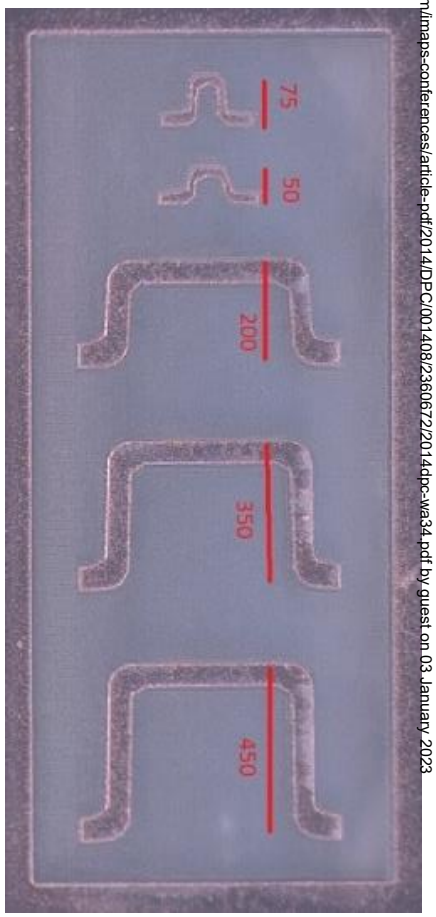
Simulation results

- Simulation indicated that, without the aluminum block, capacitances of 153 to 158 fF could be expected.
- The model with the aluminum plate was fairly close to the measurements of three of the four capacitors.
- Measurements were still somewhat higher than simulation for most frequency points.
- Differences in the actual geometry of the capacitors versus the simulated model likely will account for a significant portion of the differences.
- Surface roughness and voids may also play a role in this and will need to be explored.

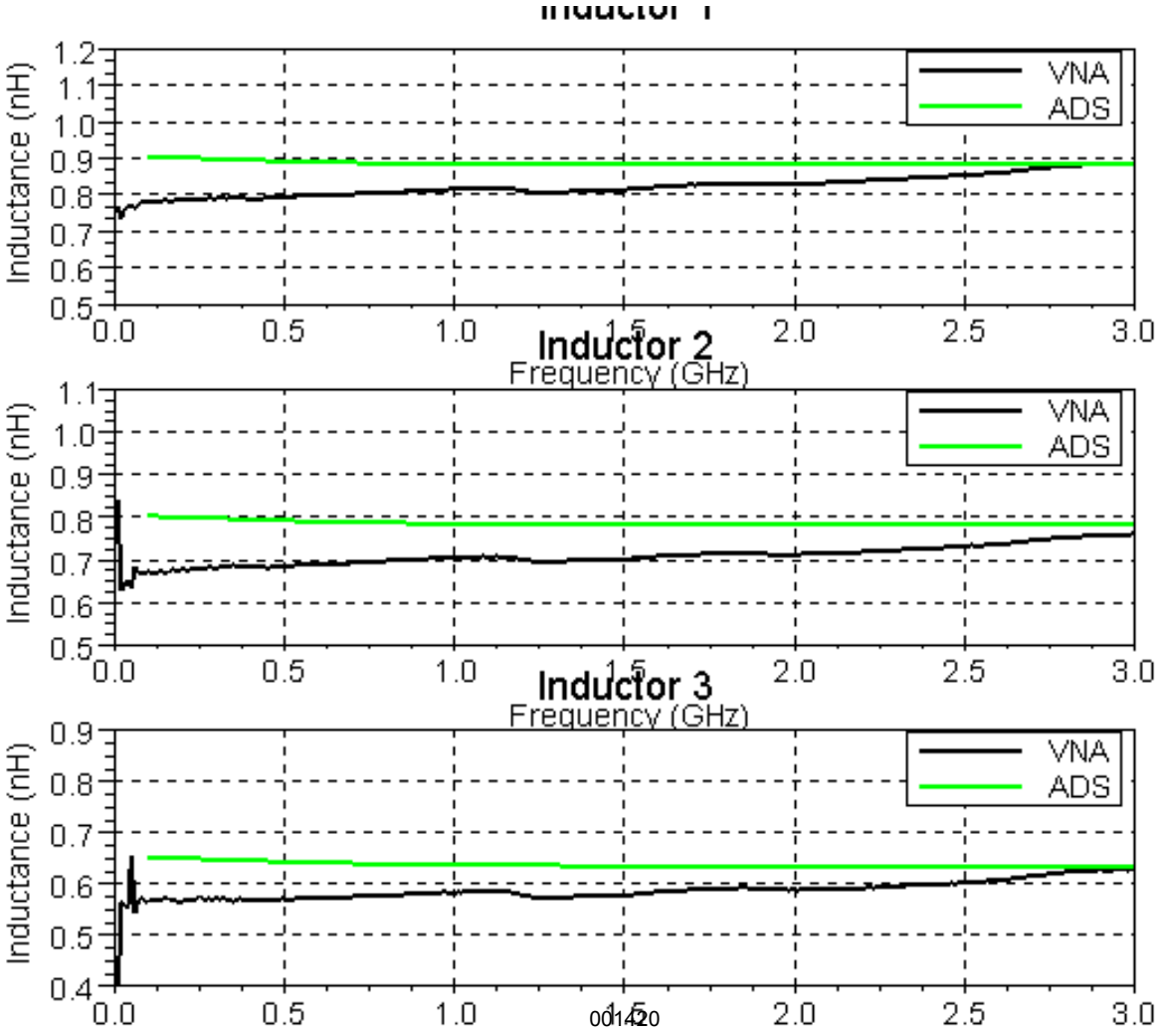
Meander Inductor Patterns Made by Isolating Etch on Copper Sputtered Sapphire Die

- 3,000Å sputtered Cu was ablated to create meander inductor patterns.
- modelled in Agilent ADS Momentum
- The largest three inductors were measured using a vector network analyzer (VNA) connected to a microprobe station
- While the VNA measurement showed a slightly lower inductance, particularly at lower frequencies, the measurement matched with simulation at the upper end of the frequency range.





Comparison of measured versus simulated inductance of largest three meander inductors



Conclusions

- This work demonstrates the possibility of fabricating passive elements on the back of sapphire devices.
- Particularly, capacitor and inductor design could be fabricated on the back of a sapphire substrate.
- Passive quality and consistency will depend on the process used to make it.
- Element design and its integration into a device will depend upon the device requirements and the equipment used for the purpose.