Wafer Level Packaging for High-Brightness LED Lighting with Optimized Thermal Dissipation and Optical Performance

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Outline

- Introduction
  - Invensas
  - LED packaging Market
- Technology
  - Industry status
  - Invensas focus
- Program
  - Invensas WLP LED
  - Flip chip
  - Wafer bonding
  - Laser liftoff

- ***Formation:*** Founded in 2011 as a wholly owned subsidiary of Tessera Technologies, Inc. (Nasdaq:TSRA)
- ***Goal***: Develop and commercialize breakthrough semiconductor interconnect solutions and IP in Mobile, Storage and Cons. Electronics
- ***Core Focus***: "Interconnectology": advanced interconnect, semiconductor packaging, memory circuitry, modules, 3D TSV architecture
- ***Company***: 50+ Employees (1/3 PhD). ***Headquarters***: San Jose, CA.

Assembly Prototyping Capabilities at Invensas

Die Placement

- FC Bonder
- Accuracy ±2 µm
- Flux Dip, TCB, Dispense
- C2C, C2W
- High-force, Ultra Low-force

D/A Print

- Auto alignment
- Wafer level printing
- Proflow for fine features
- ProActive (Ultrasonic squeegee)

Wire Bond

- Gold/Copper wire-bonder
- Fine-pitch
- Low Loop

Underfill

- Jet Dispense
- Volumetric Control
- Repeatability 25µm
- 350 x 350mm Work Area

Cure

- Batch Ovens
- Convection
- Vacuum
- Inert Gas Flow (N_2)

Flux Clean

- Centrifugal Action
- Zero Discharge
- Ionic Contamination Tester*

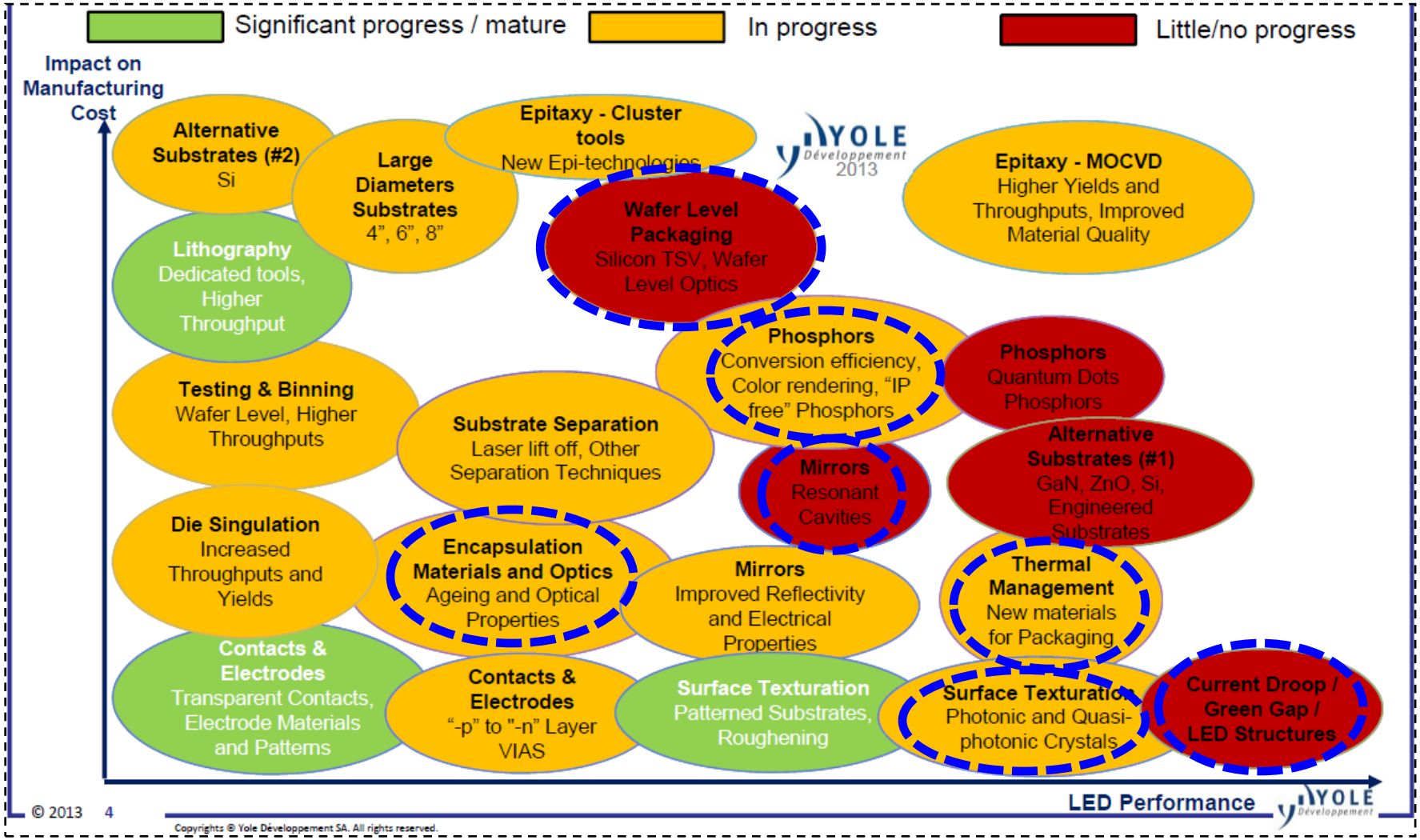
Reflow

- Lead Free Certified
- 10 Heat 3 Cool Zones
- CDA or N_2 Cover Gas

Encapsulation

- Transfer Mold
- Compression mold capable
- Film capable
- Vacuum assist

Industry status, Invensas focus



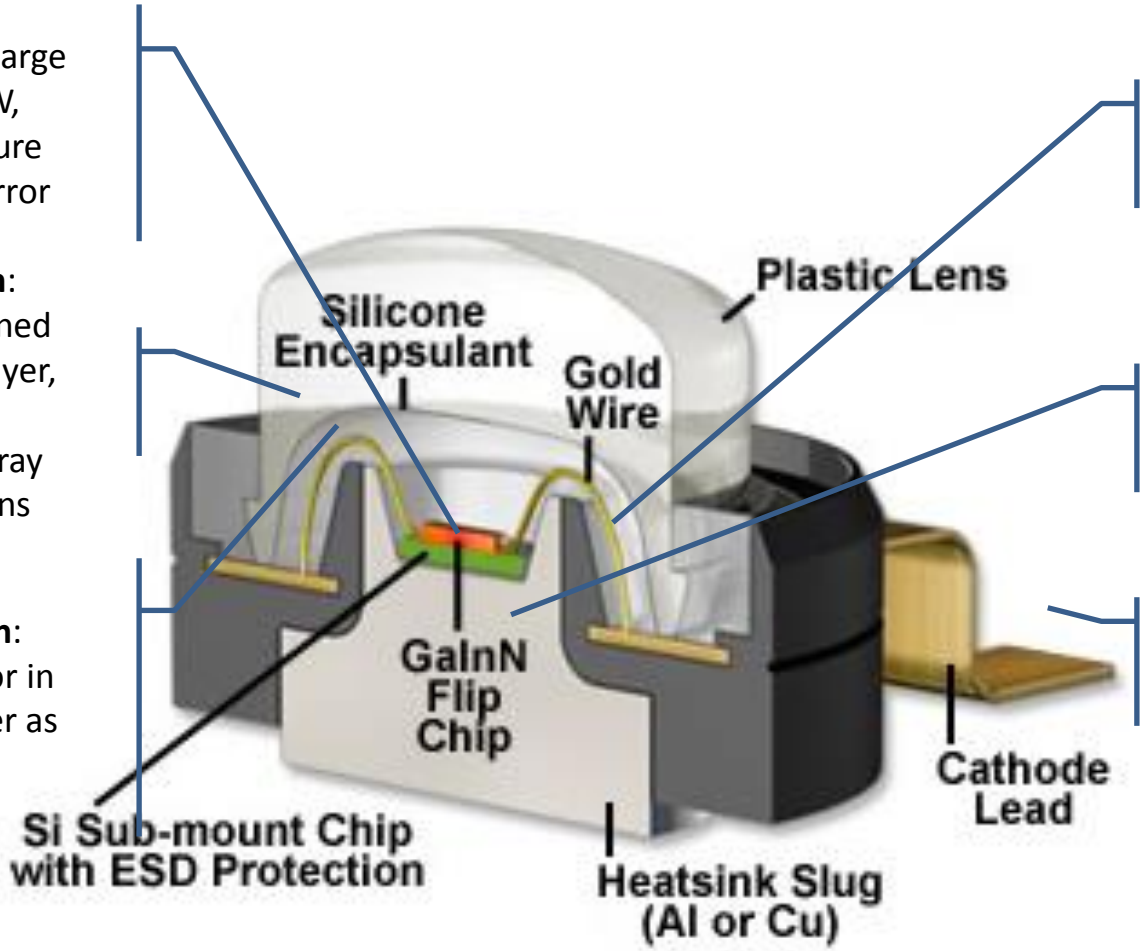
Reference: Yole Development, SemiconWest, 07/2013

Invensas solution to LED industry challenges

Light efficiency: charge balance in MQW, maximized aperture ratio, full-area mirror

Light extraction: Internal: Roughtened GaN, high-index layer, nanoparticles, External: large array molded micro lens

Light conversion: integrate phosphor in high-index polymer as micro lens



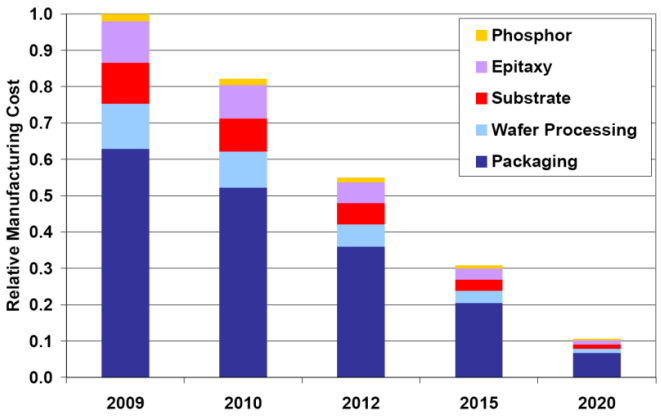
Electrical design: current spreading layer on both p and n sides

Thermal management: Maximized thermal dissipation area

Cost: full WLP Large wafer size (>8”)

Challenges for LED packaging

Packaging cost is very high

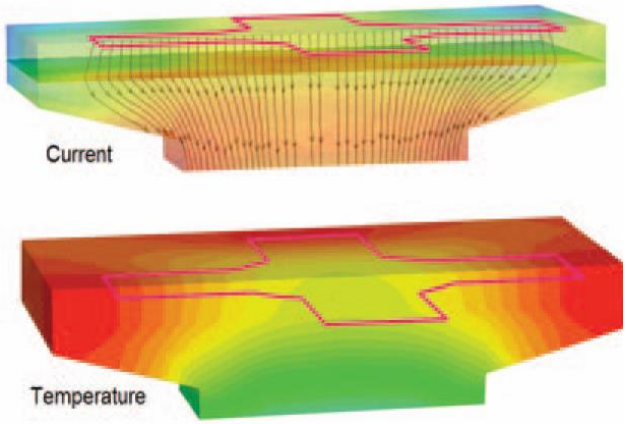


Parallel process→lower cost

Thermal management is very demanding

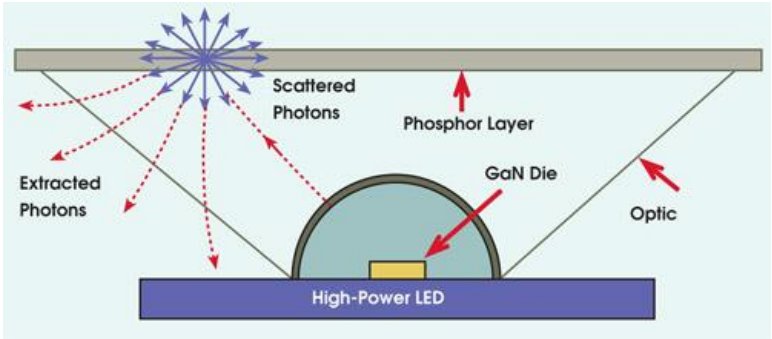
Max. heat dissipation path→better performance

Electrical field distribution is not optimal



uniform electric field→ higher efficiency

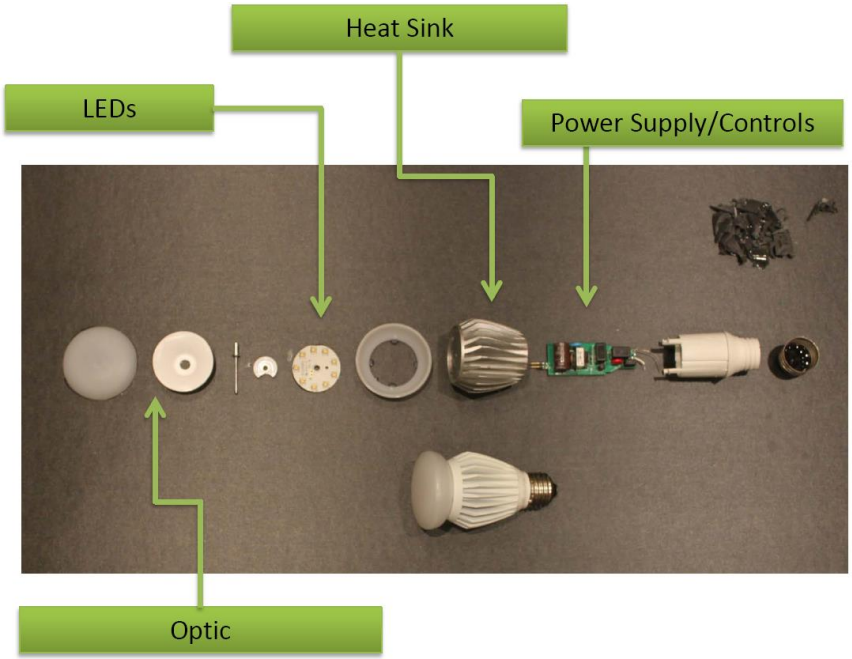
The phosphors degrade impacting white light



remote phosphor →longer lifetime

LED Packaging cost

- LED package currently ~50% of LED lamp cost
- DoE roadmap targets: >10x reduction for LED package cost



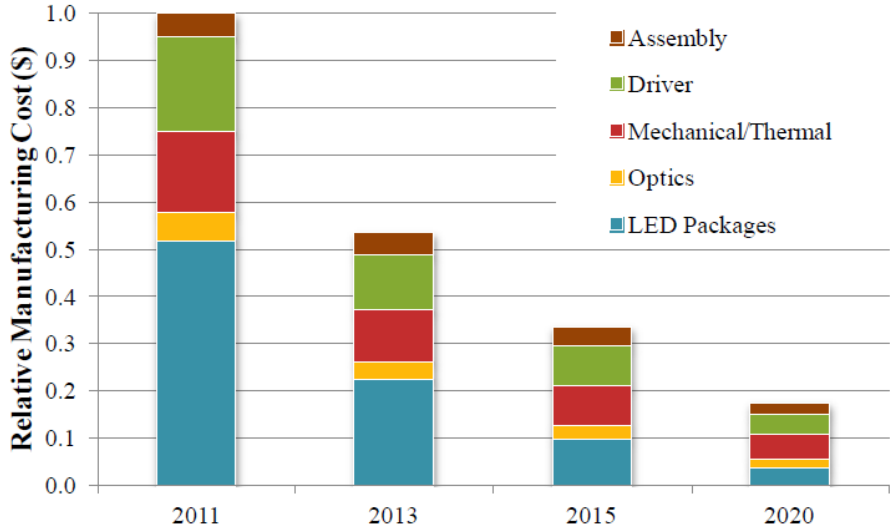


Figure 1-1. Projected cost track for an LED-based A19 60W replacement lamp

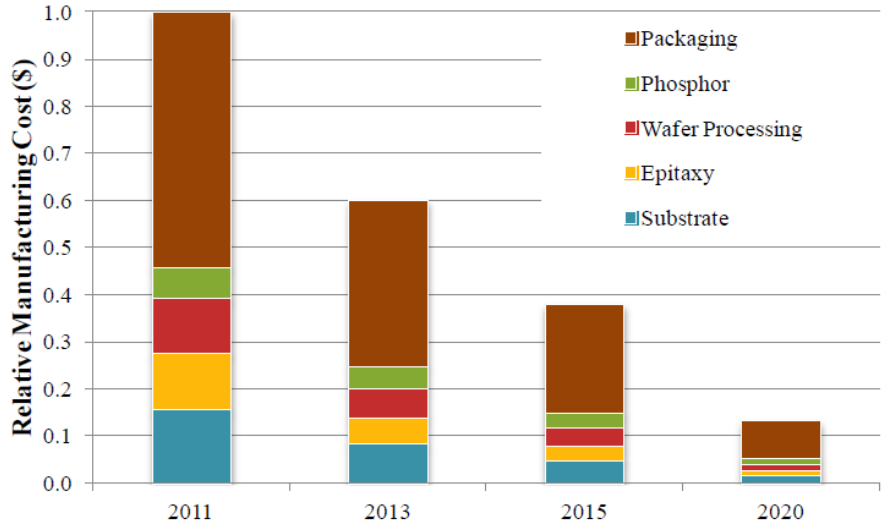
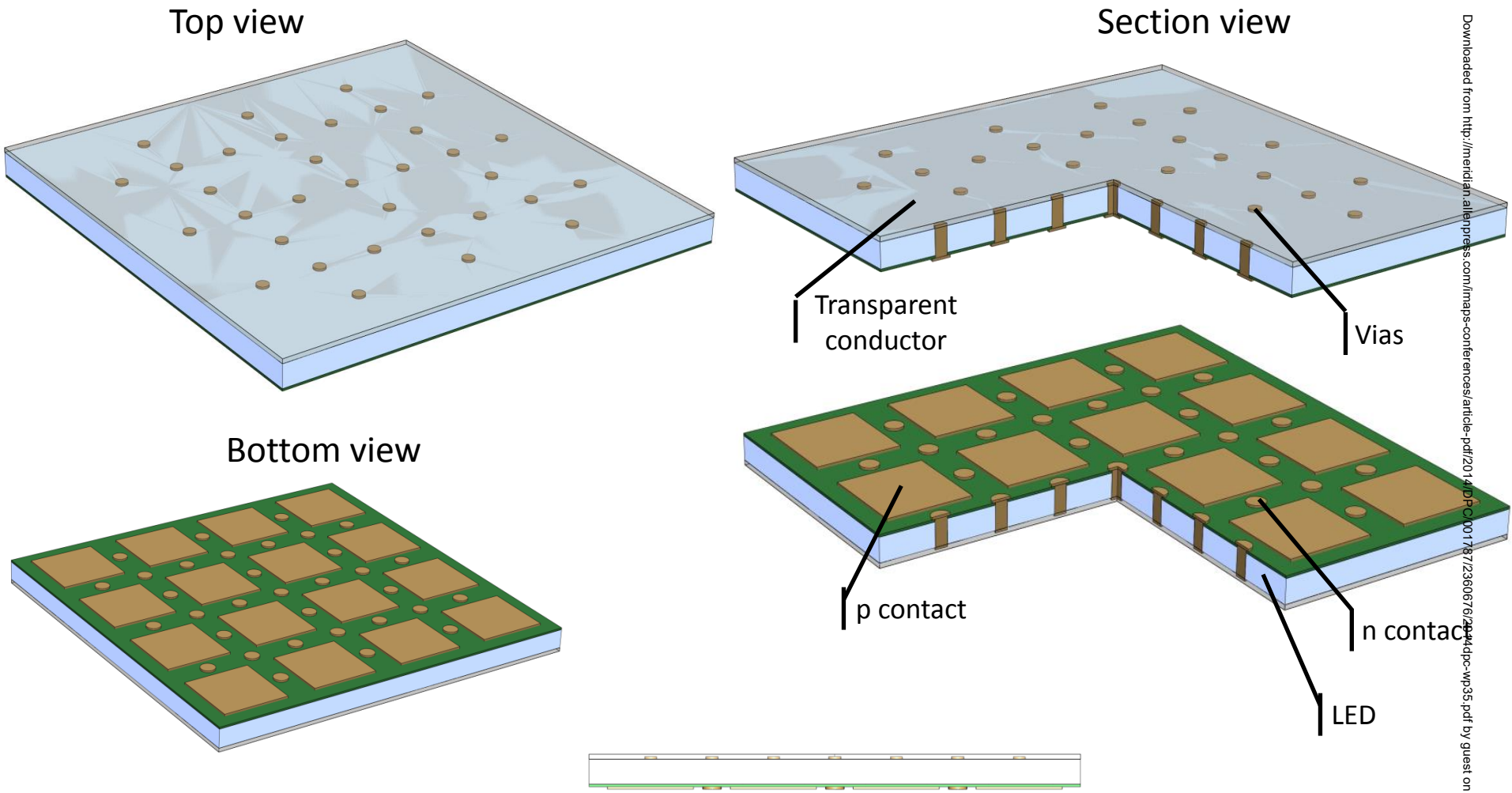


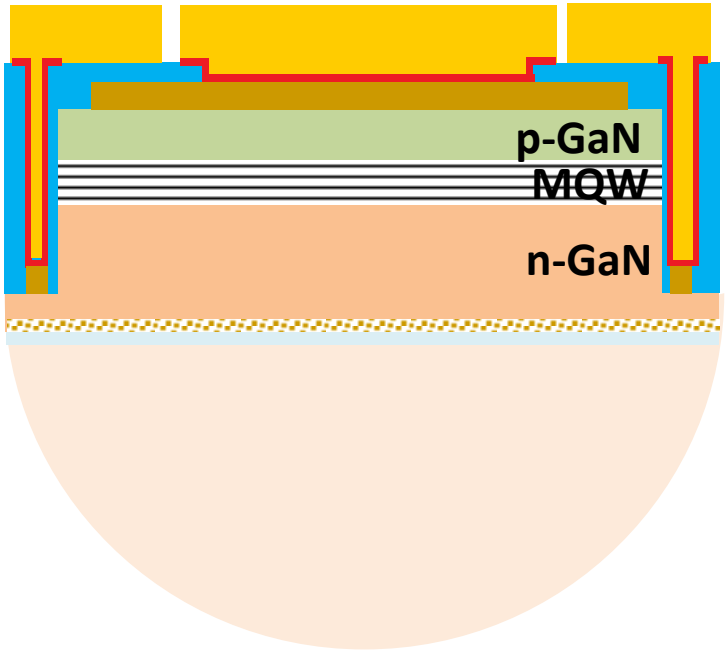
Figure 1-2. Projected LED package cost track *Source: Yole Development*

High Performance LED with Thermal Walls /vias



- An LED device with distributed walls or vias connecting to a common doped region w/ a transparent conductive layer for uniform current distribution.

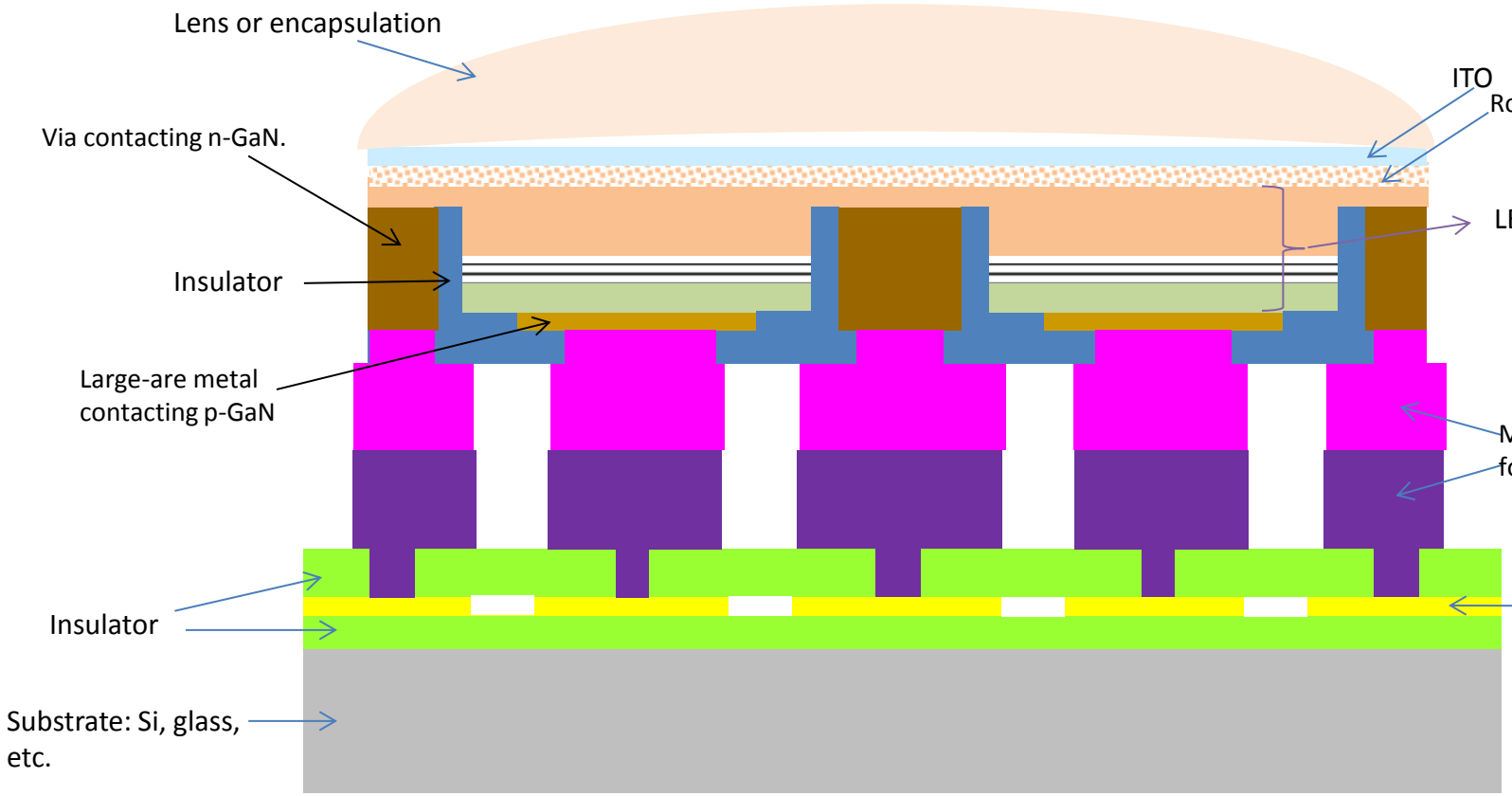
Novel wafer-level LED packaging structure



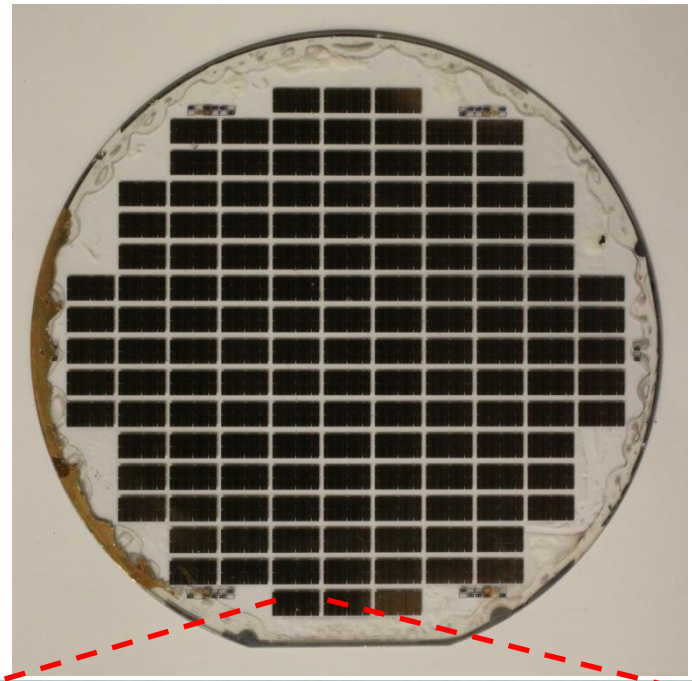
Advantage of the technology:

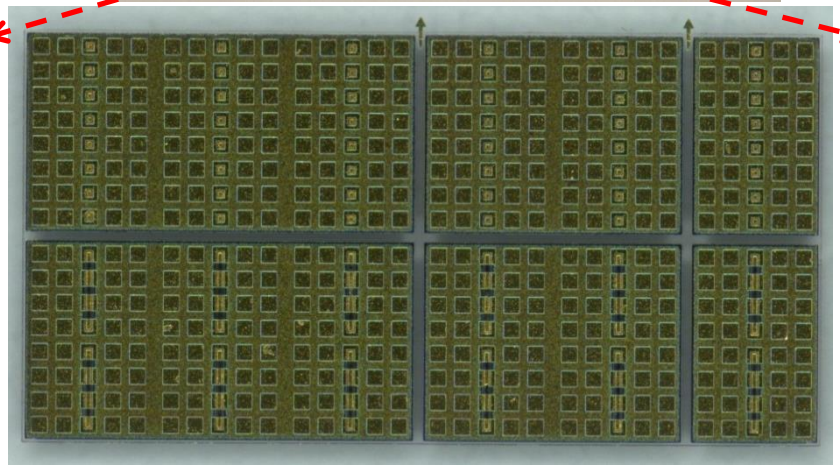
- Maximal thermal dissipation rate from active device stack to substrate (thermal path on 5 sides)
- High aperture ratio (>90% area of wafer emitting light)
- Optimal design for light output (mirrors on 5 sides)
- True wafer-level process all the way (no chip handling) for high throughput at low cost
- Uniform current spreading on both electrodes
- Big chip size for high brightness
- Scalable to large wafer size

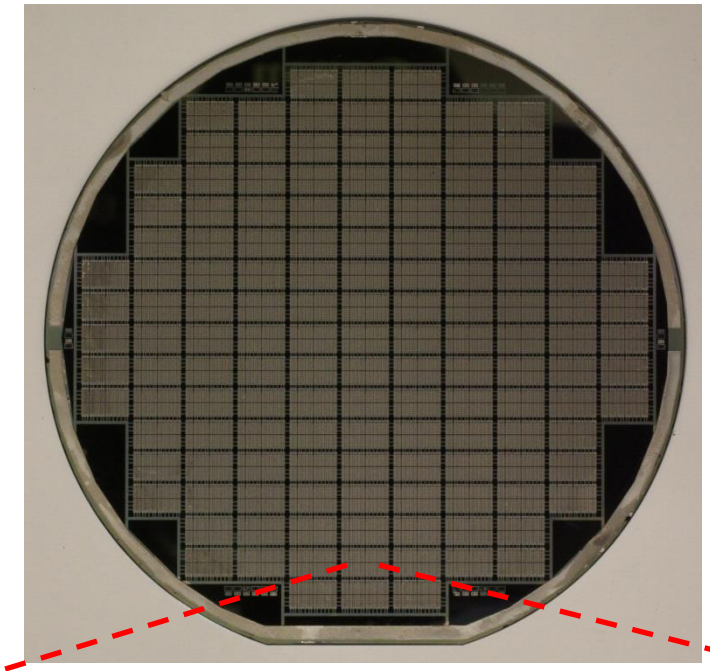
Structure design

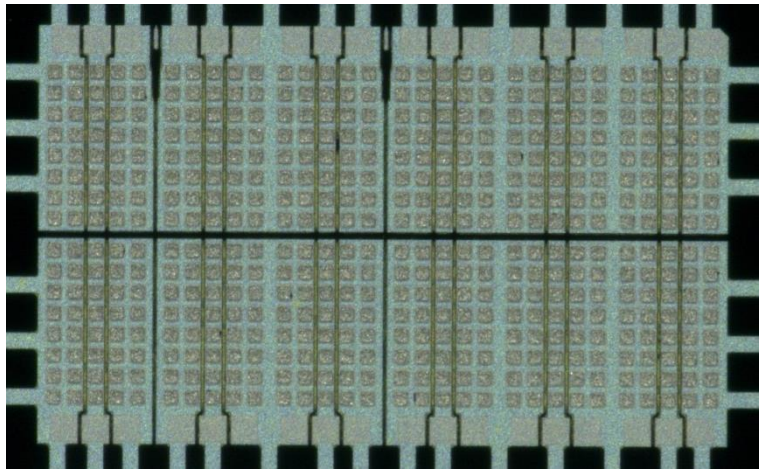


Wafers before dicing





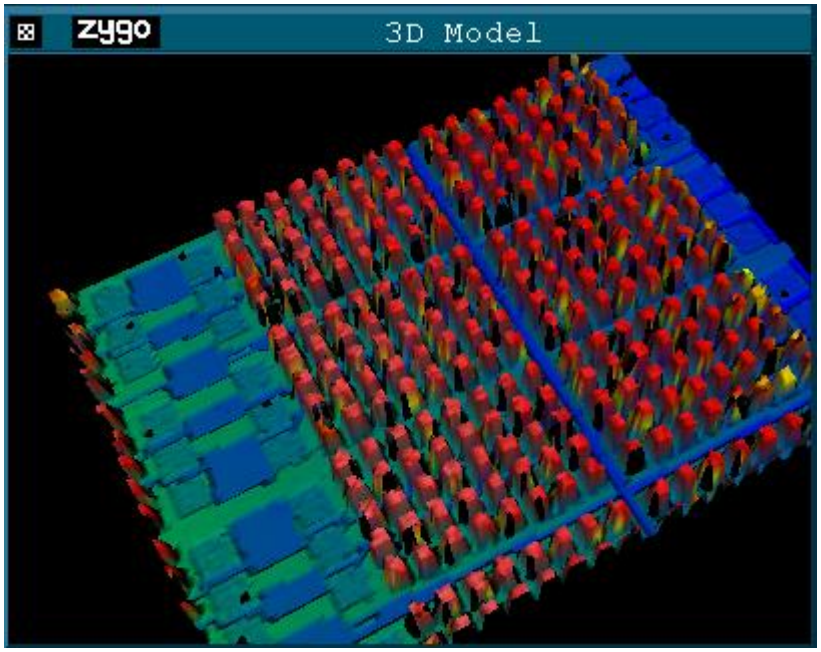




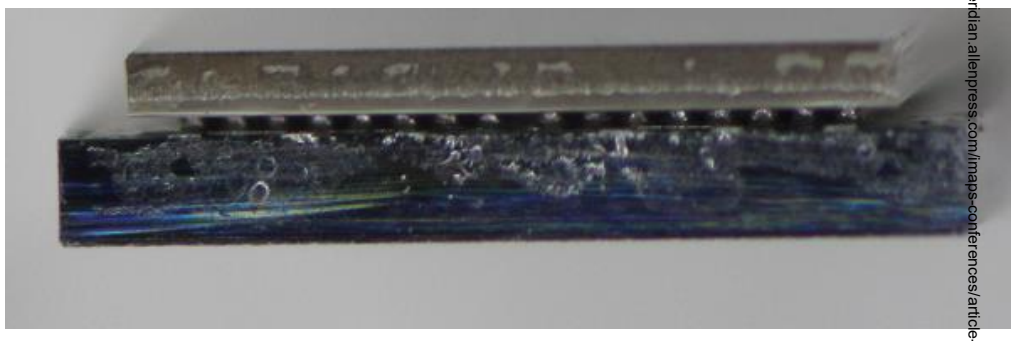
LED / sapphire

Si interposer

Reflow Flip chip: GaN LED - Si submount

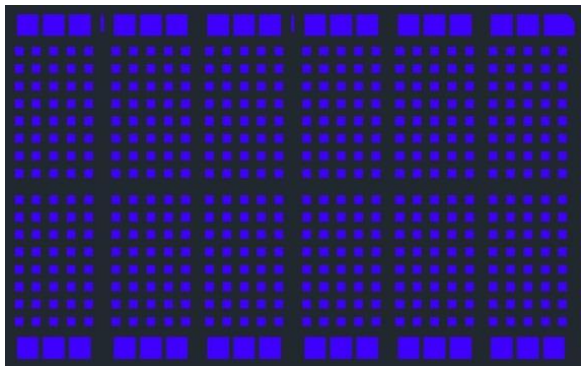


3D map of Si die with
solder bumps: ~30um height,
~110um pitch

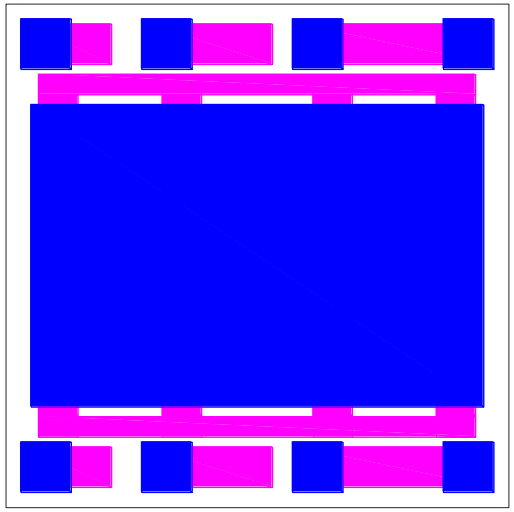


After flip-chip and reflow

Die attach and wire bond

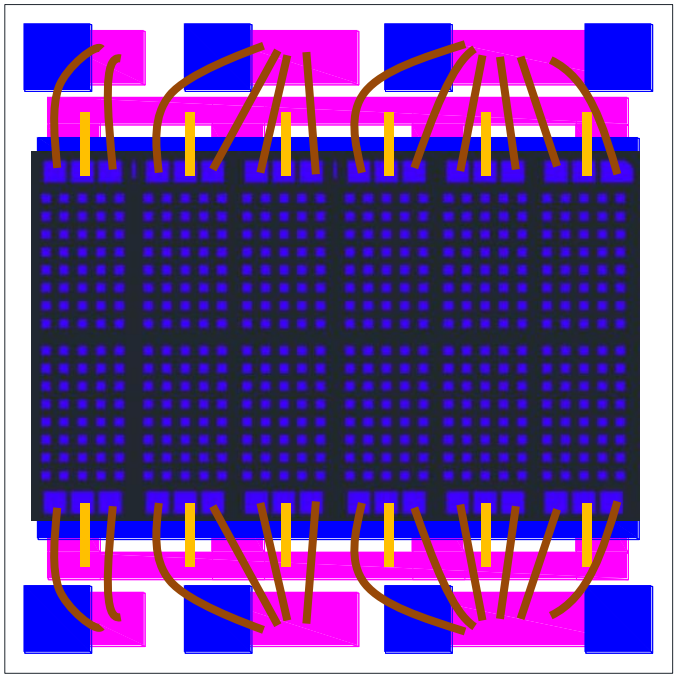


Si die, 4.1mmX2.5mm

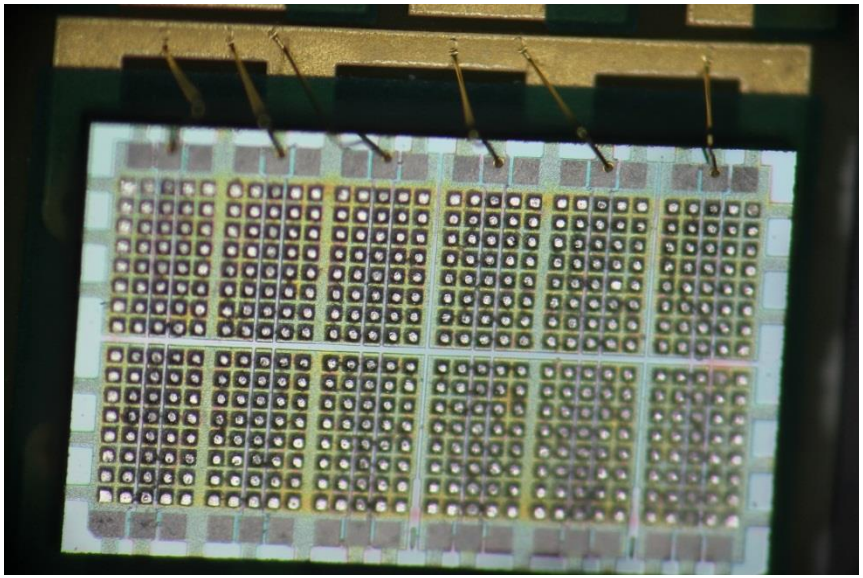


Front side of PCB,
5mmX5mm,
Blue area: solder mask.

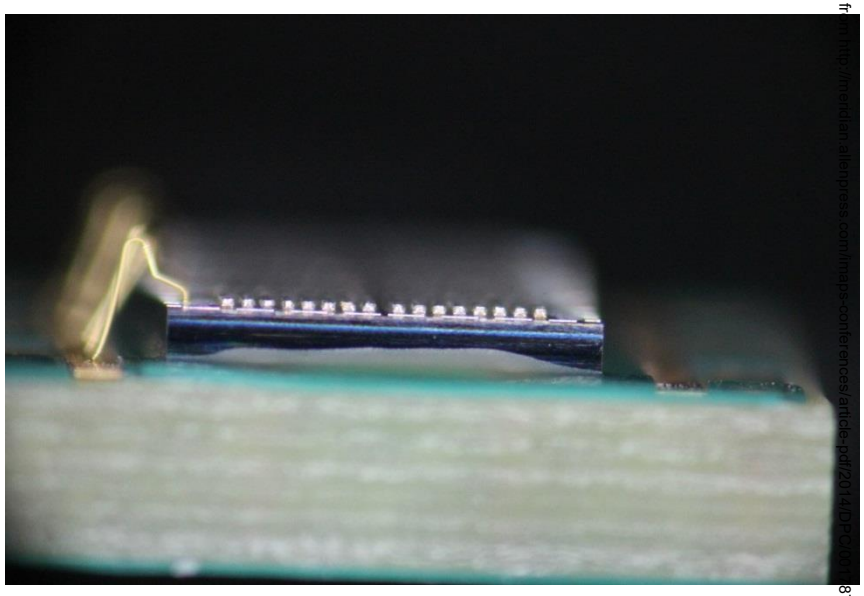
36 wire bond pads on a die



After wire bond

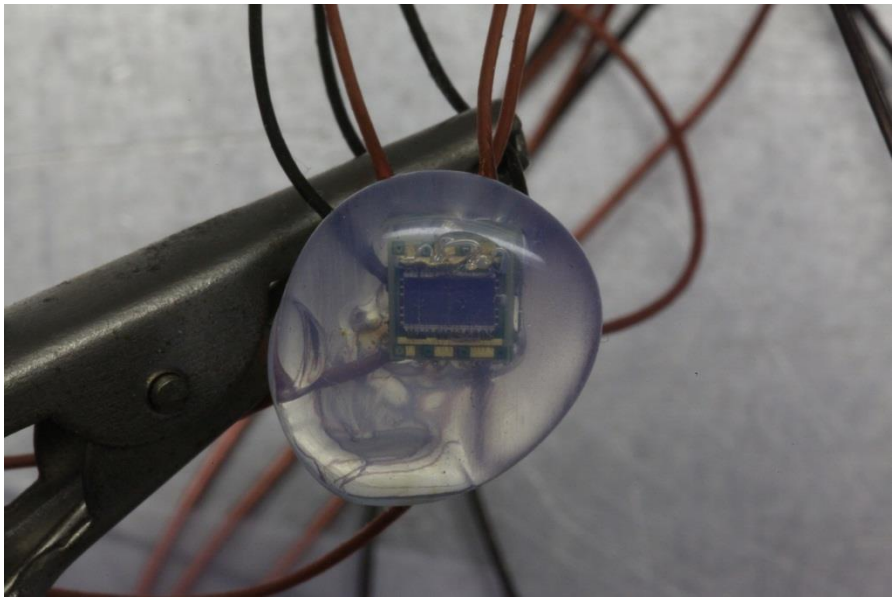


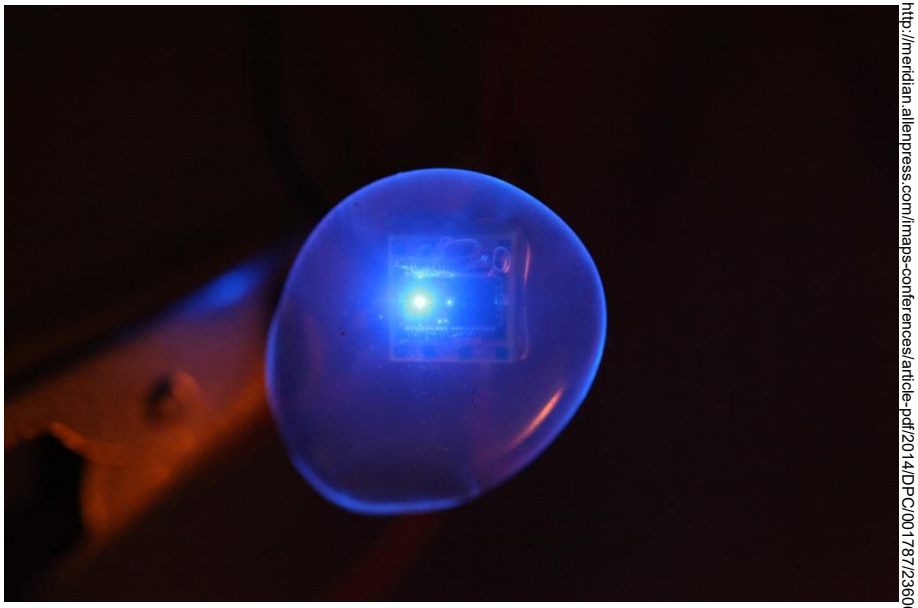
Top view of wire bond example



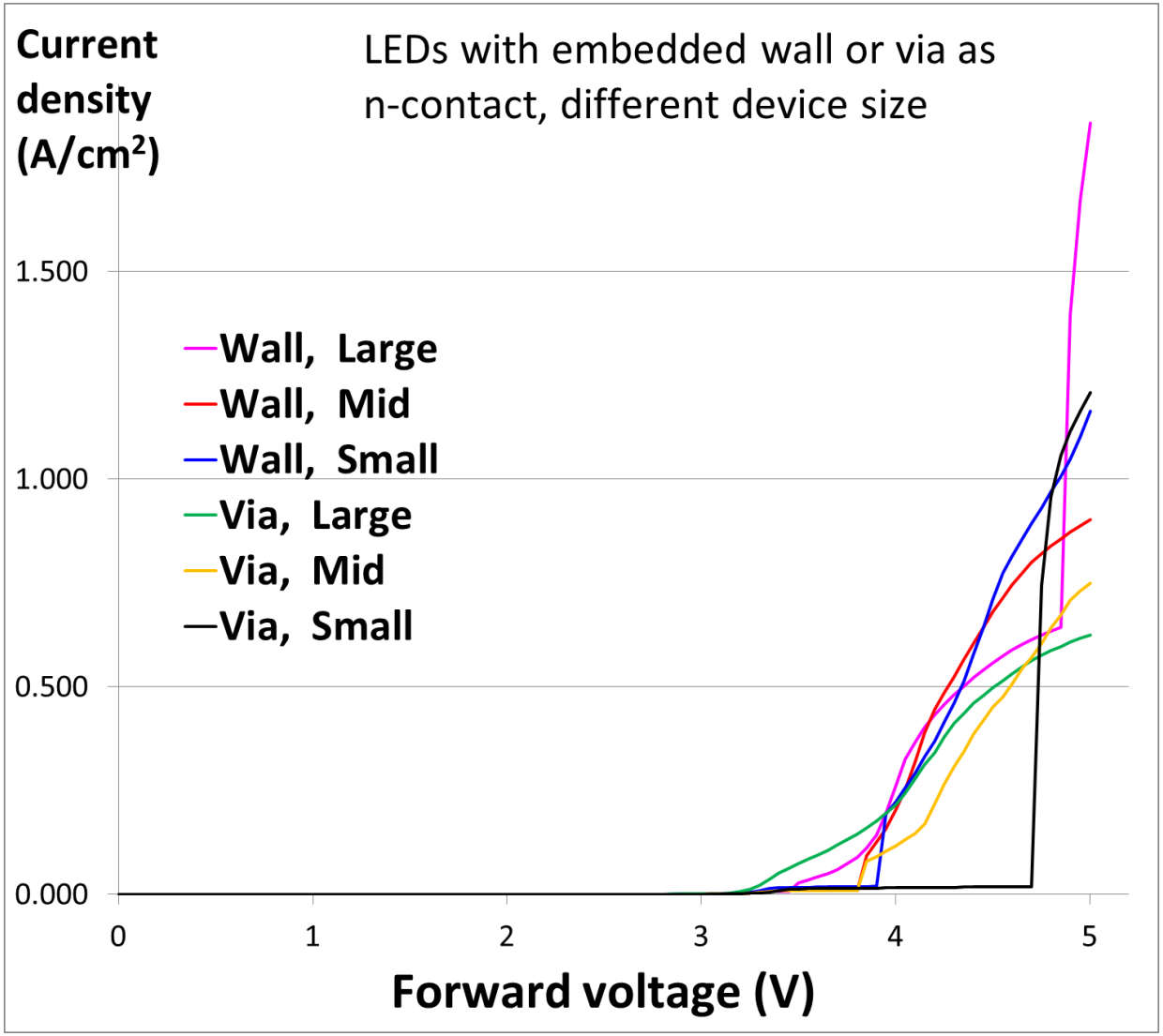
Side view of wire bond example

Packaged LED parts lighting

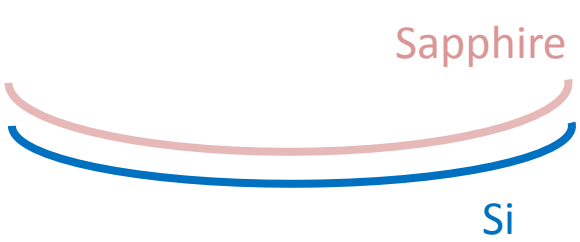




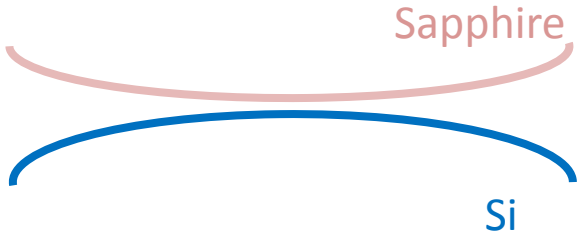
Electrical Characterization of 6 LED devices



Wafer-level warpage



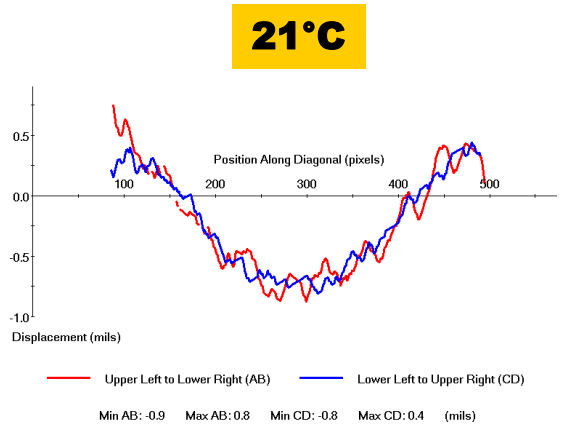
Room temperature

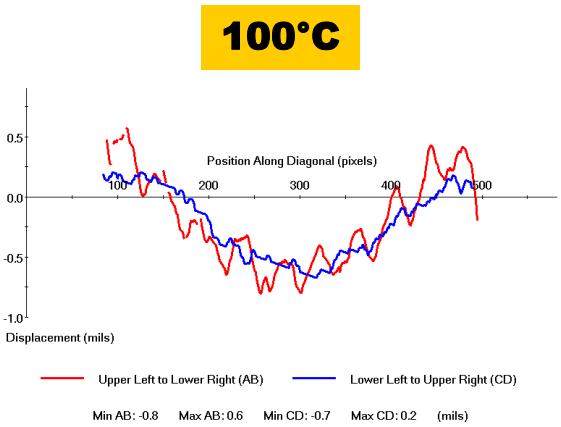


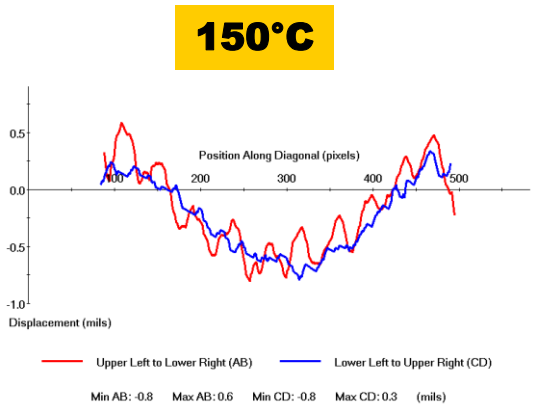
Reflow temperature

- Wafer-level warpage is one key challenge for wafer level packaging.
- LED/sapphire wafer: CTE (sapphire > GaN) → warpage towards sapphire.
- Si interposer wafer: CTE (metal routing > Si) →Warpage changes upon temperature.

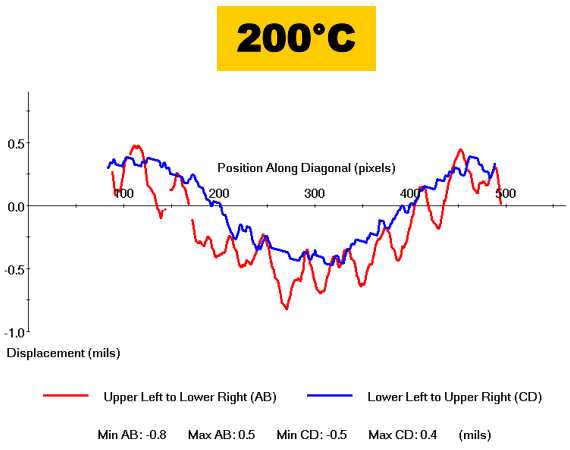
Sapphire wafer, Moire viewed from back side

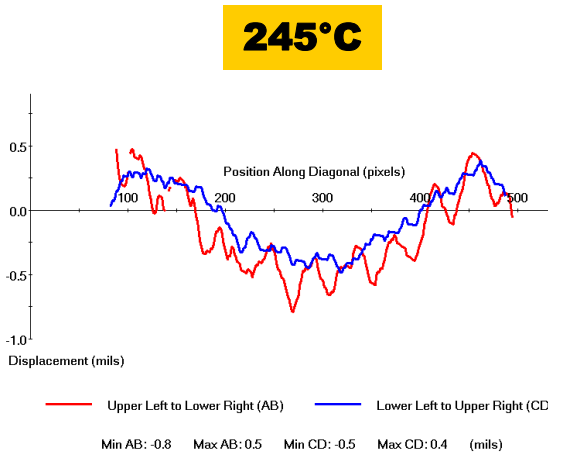


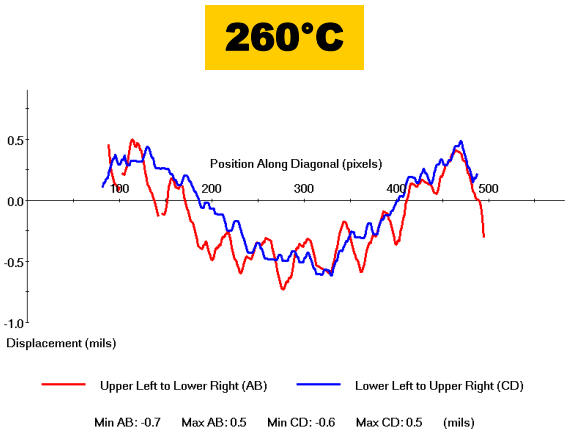




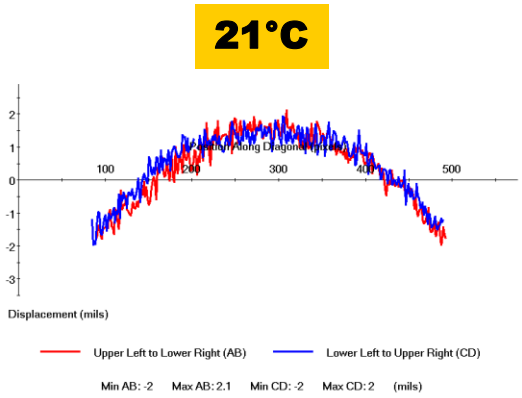
- Reflow temperature << MOCVD growth temperature → warpage profile remains unchanged during thermal cycle
- Unable to correct warpage after MOCVD growth

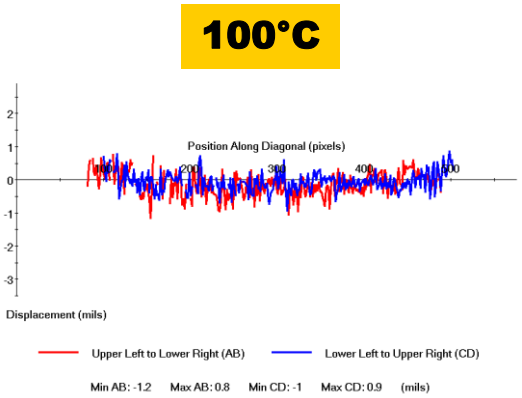


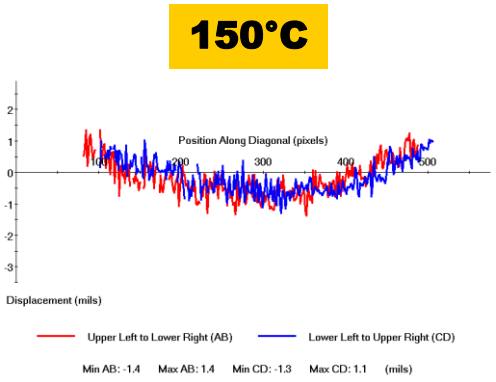




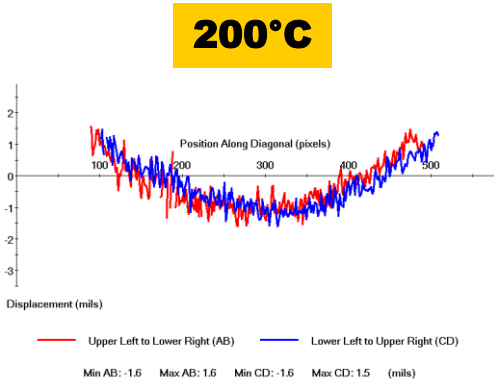
Si wafer, Moire viewed from backside

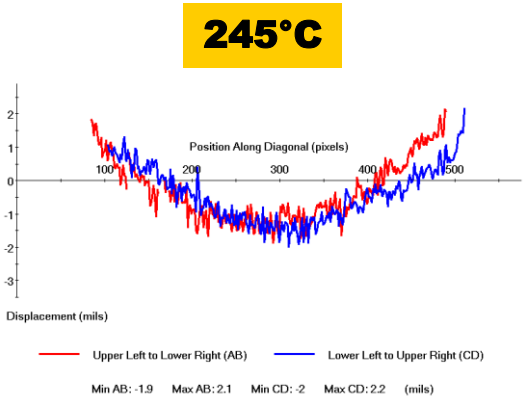


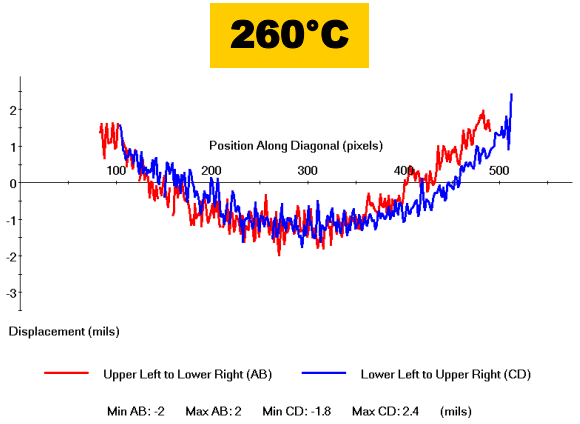




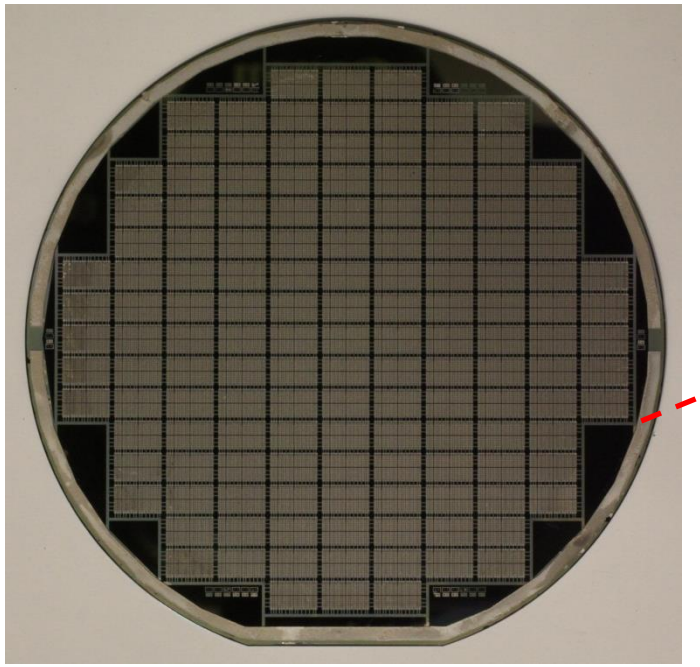
- Metal routing is the dominating contributor of warpage caused by CTE mismatch.
- Stress-free temperature is close to the temperature at sputtering deposition.







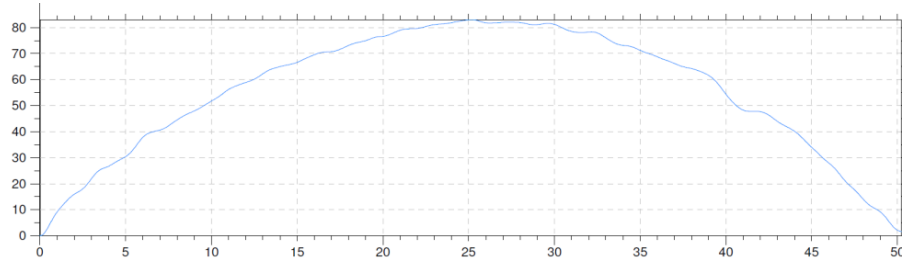
Warpage correction



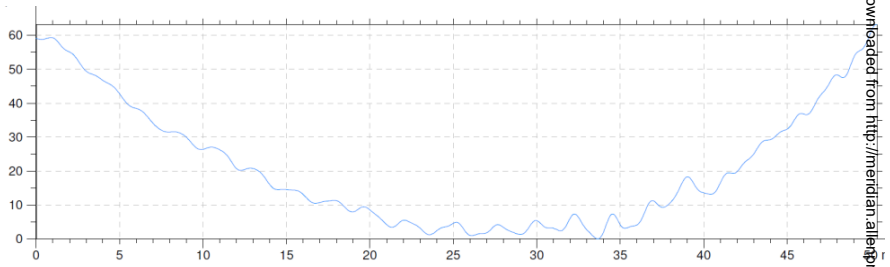
One main cause of warpage:
Metal ring from electroplating

- Deposit counter stress layer (Al) on backside to balance warpage
- Removal of plated metal ring around the frontside Si wafer periphery

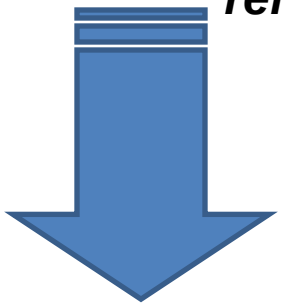
Sub-mount wafer warpage correction: Moiré data

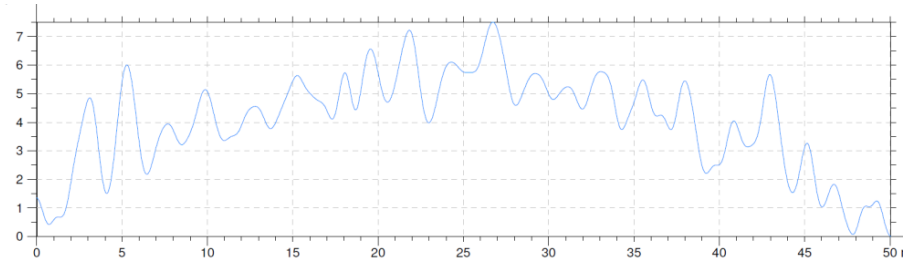


Warpage of sub-mount wafer at ***RT*** before correction

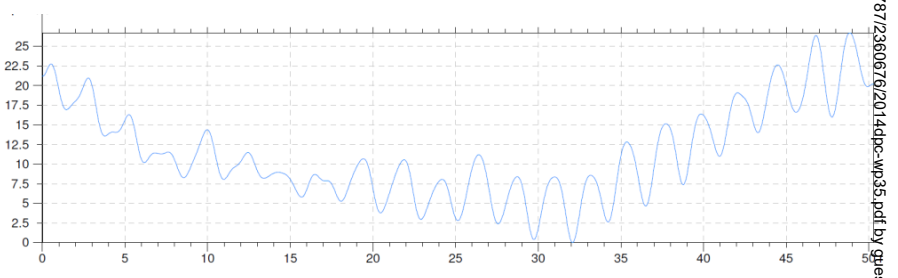


Warpage of sub-mount wafer at ***reflow temperature*** before correction



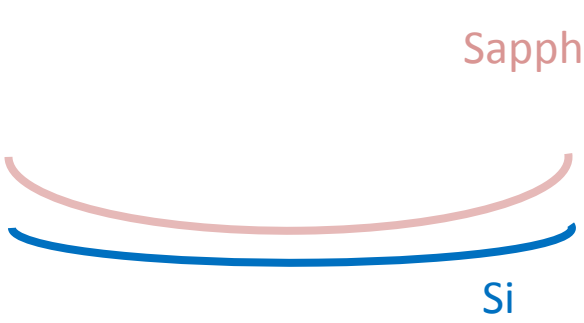


Warpage of sub-mount wafer at ***RT*** after correction

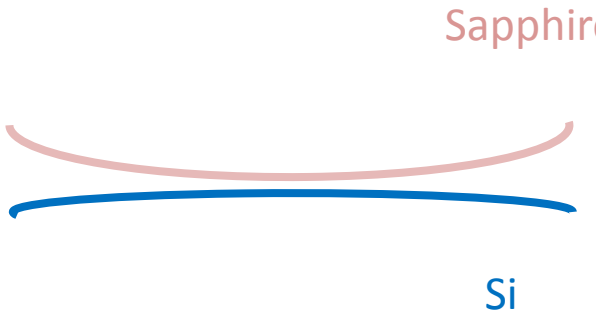


Warpage of sub-mount wafer at ***reflow temperature*** after correction

After warpage correction



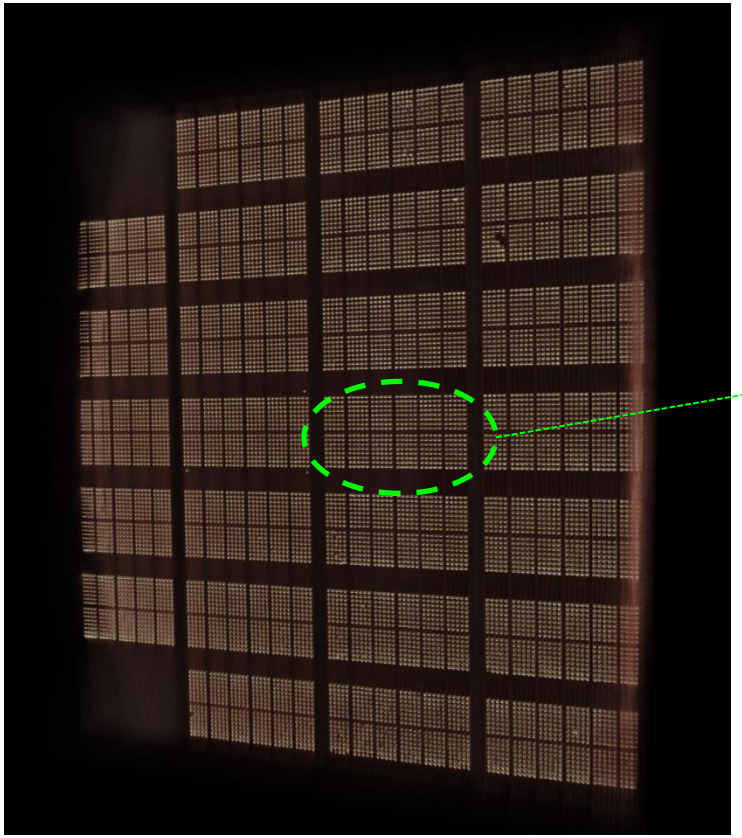
Room temperature

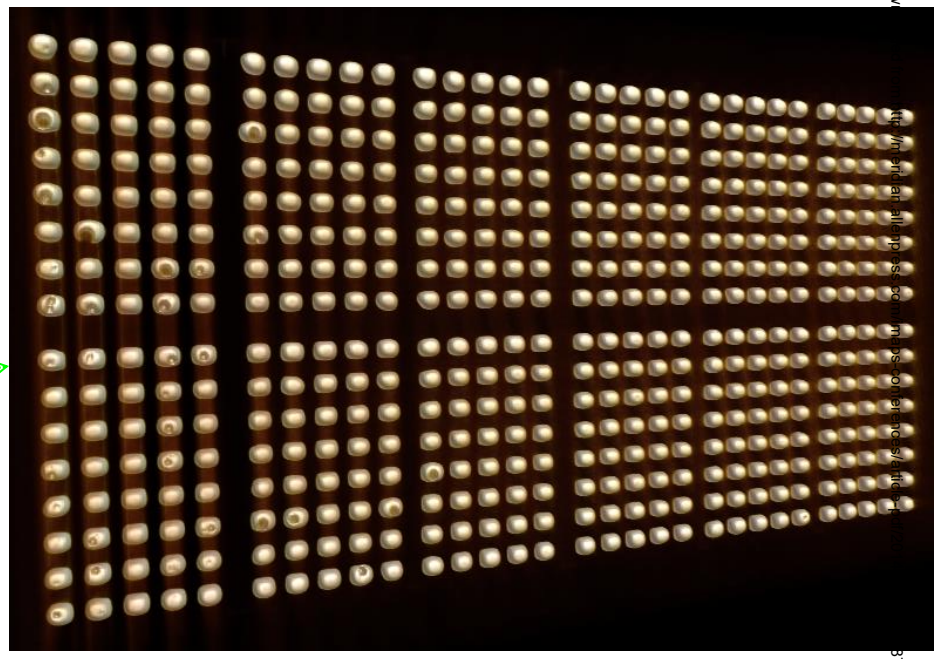


Reflow temperature

After warpage correction, the wafer-level warpage is manageable.

Wafer bonding characterization: X-ray tomography

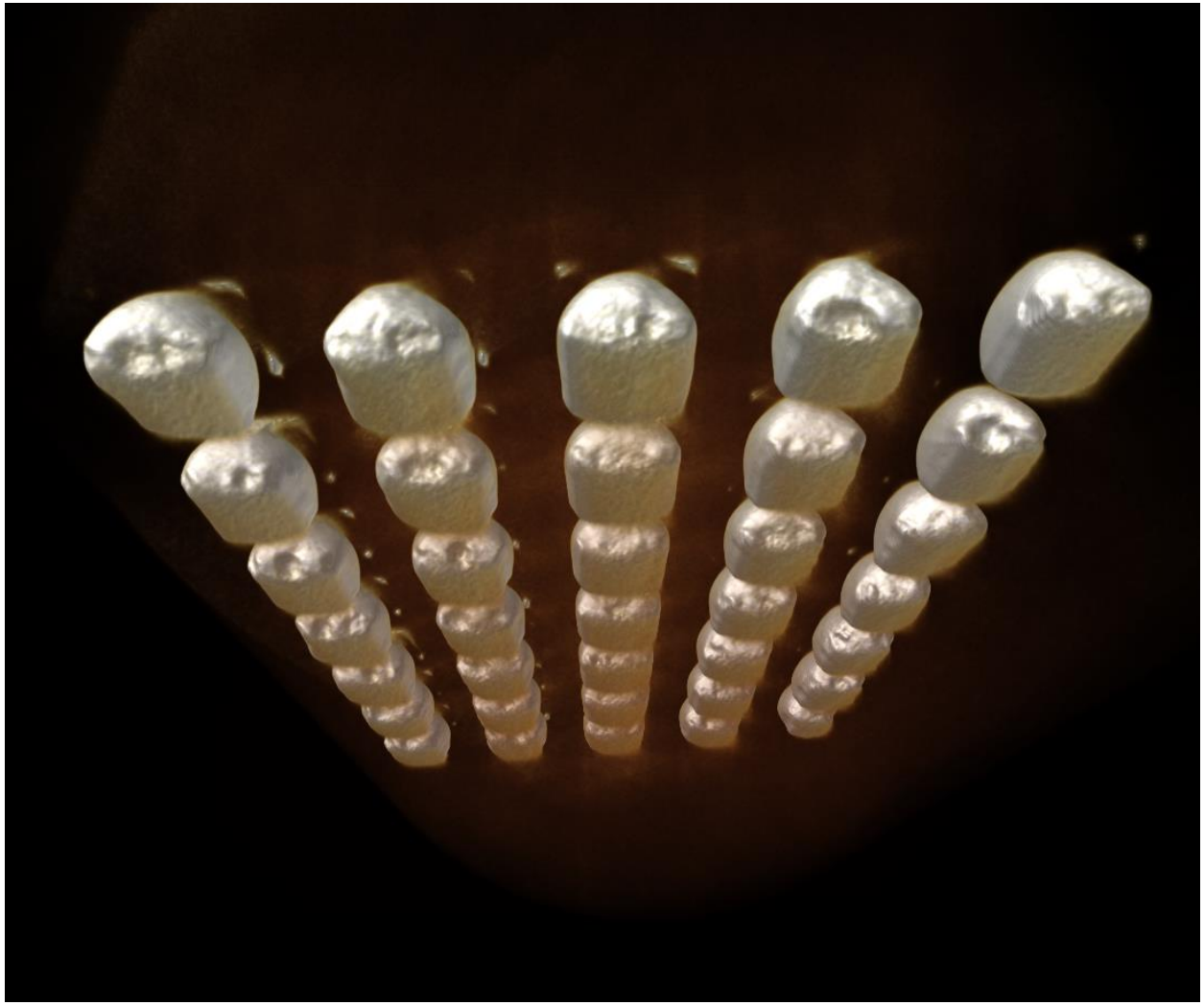




Center location:
4X, resolution=4.13um,
viewing from sapphire side

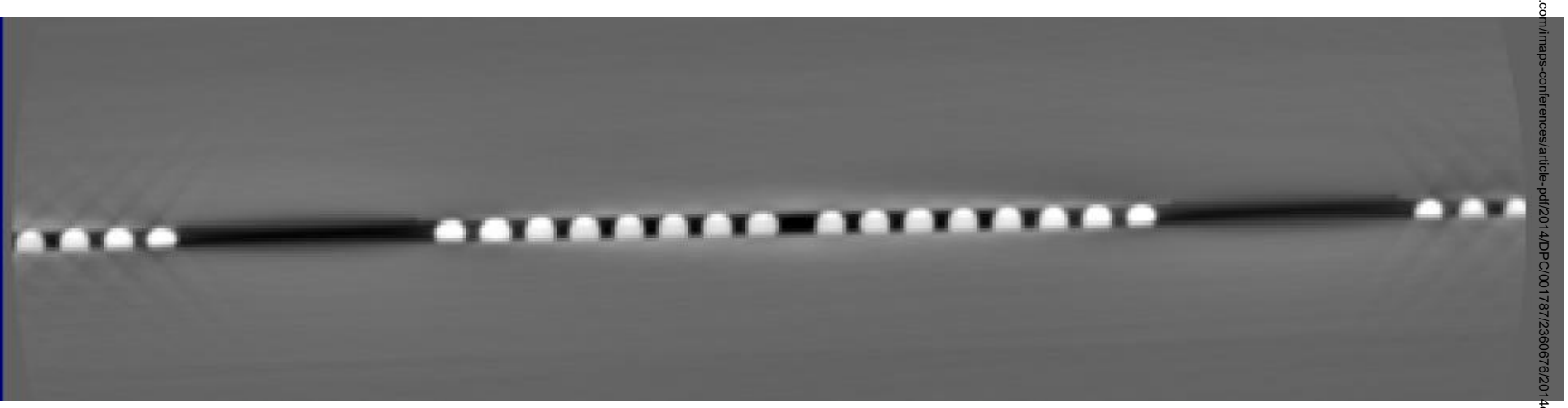
Macro view:
1X, resolution=9.23um

Wafer bonding characterization: X-ray tomography



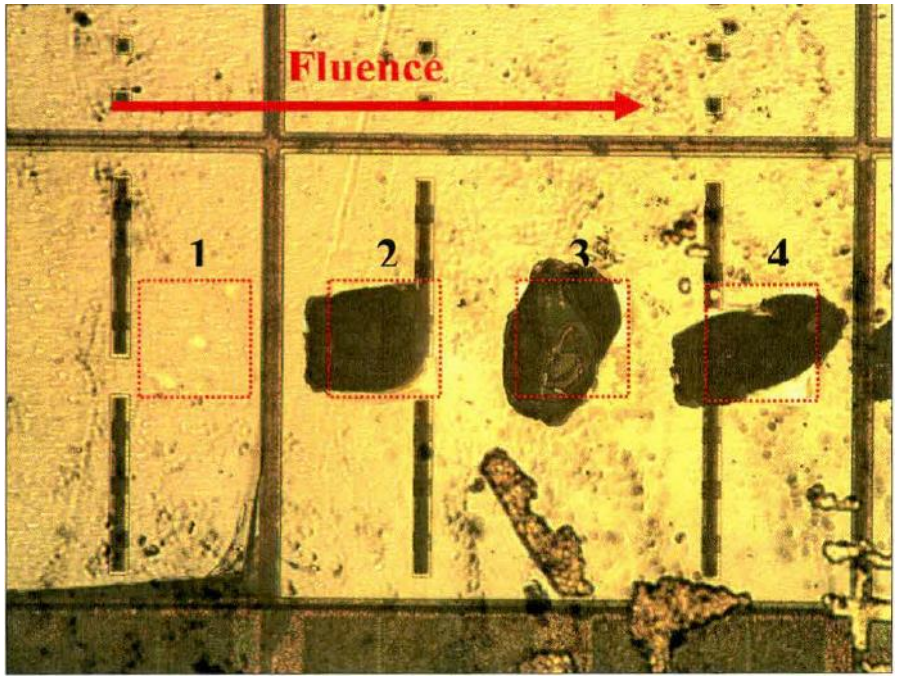
Center location: 20X, resolution=0.8um,
viewing from Si side

Wafer bonding characterization: X-ray tomography



cross-section view, Edge location, resolution=4.13um

Key learning : planar back support for laser liftoff

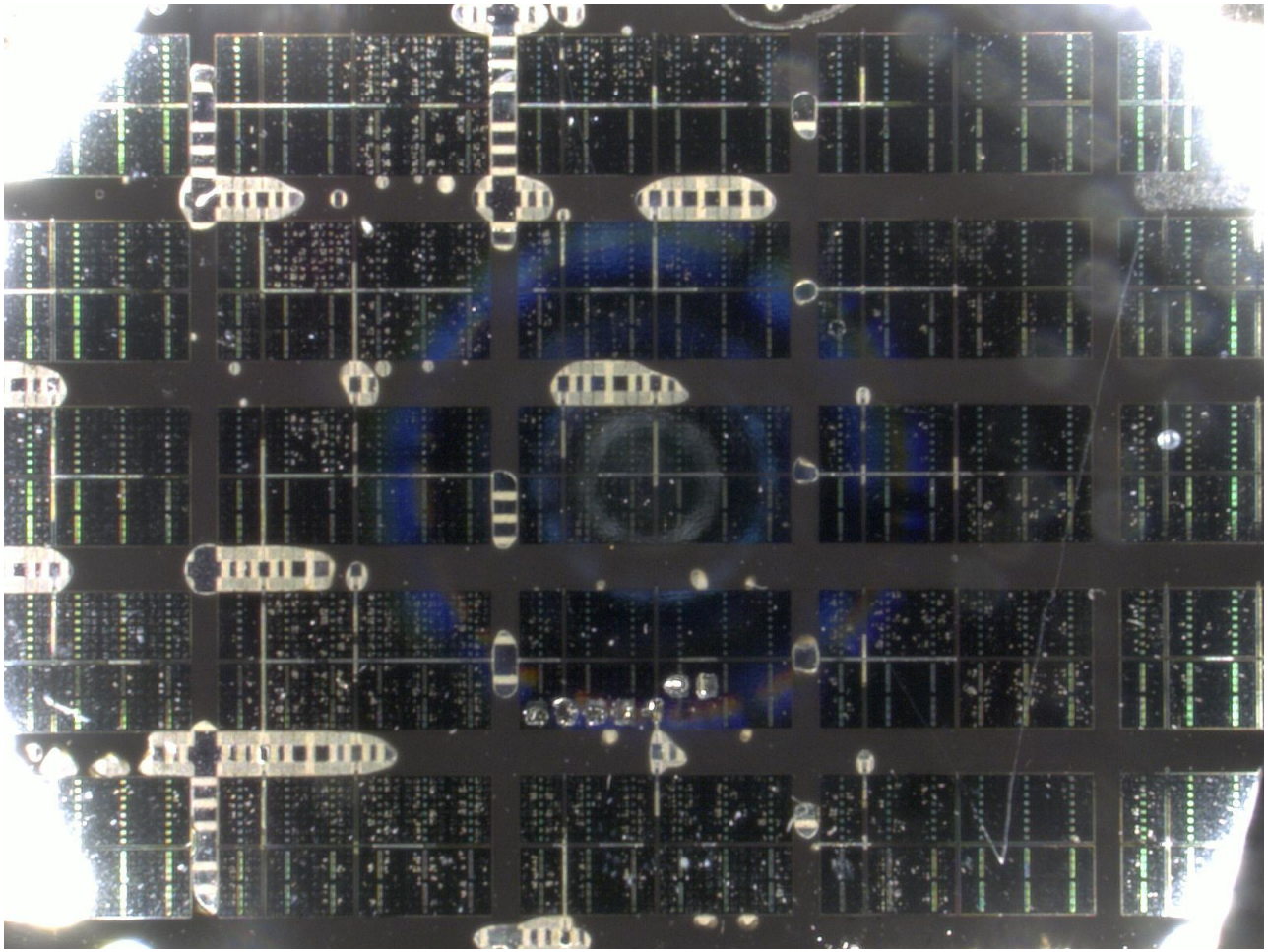


From left to right areas (1 to 4) were exposed with increasing laser flux. Fragmentation of the film is noticed starting with area 2

5um-thin GaN fractured due to lack of back support upon sapphire / GaN interface separation

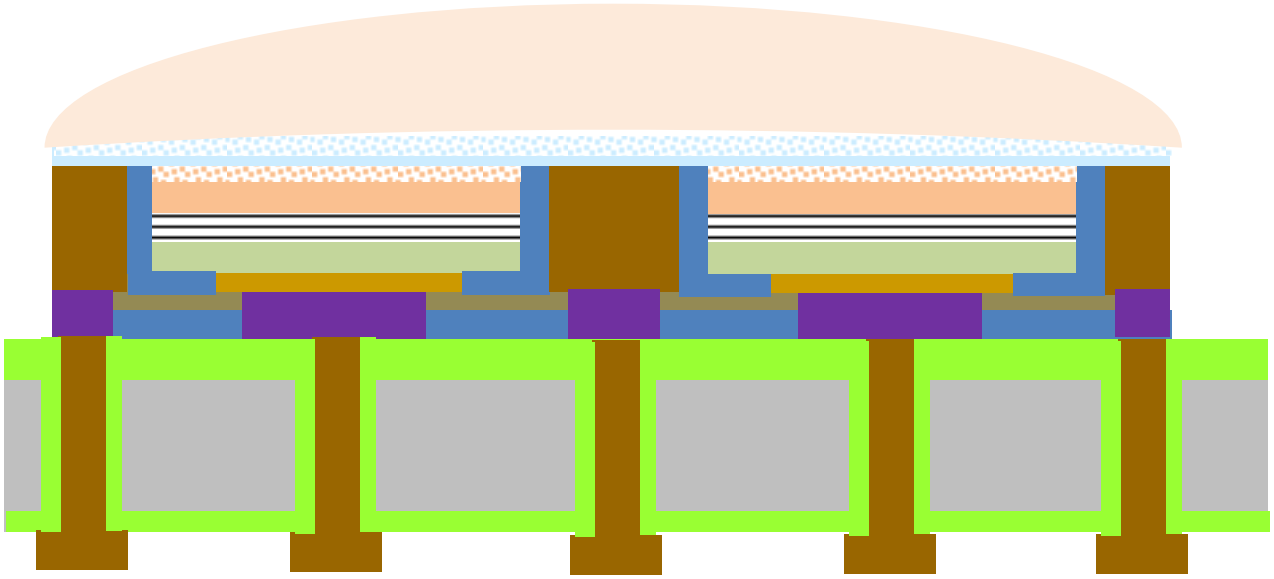
- **Root cause**: topology of solder bumps on Si mount wafer
- **Solution**: filling the air gap, or planarize the contact surfaces prior to wafer bonding

Large wafer level underfill is challenging: voids



- Wafer level underfill is challenging, not scalable to large wafer size
- Solution: pre-applied underfill (concern: particle entrapment);
  thru-hole openings distributed over wafer area (process concern)

Next for LED WLP



Thru-via sub-mount

- No need for PCB substrate.
- Superior thermal performance.
- Full wafer level process from fab to packaging.

Conclusion

- Unique design of vias and walls embedded in LED device stack for thermal and optical performance
- Flip-chip packaged LED part emits bright light at low voltage (3.5V)
- Wafer-level warpage of LED and submount are both challenging
  - GaN/sapphire wafer warpage must be corrected prior to MOCVD
  - Metal routing is the dominating contributor of Sub-mount wafer warpage induced by CTE mismatch.
  - Sub-mount wafer warpage can be corrected by balance layer
  - High CTE material near wafer periphery has high impact on warpage
- Planar back support is critical for WLP using laser liftoff
- Creative solution is needed for wafer-level underfill

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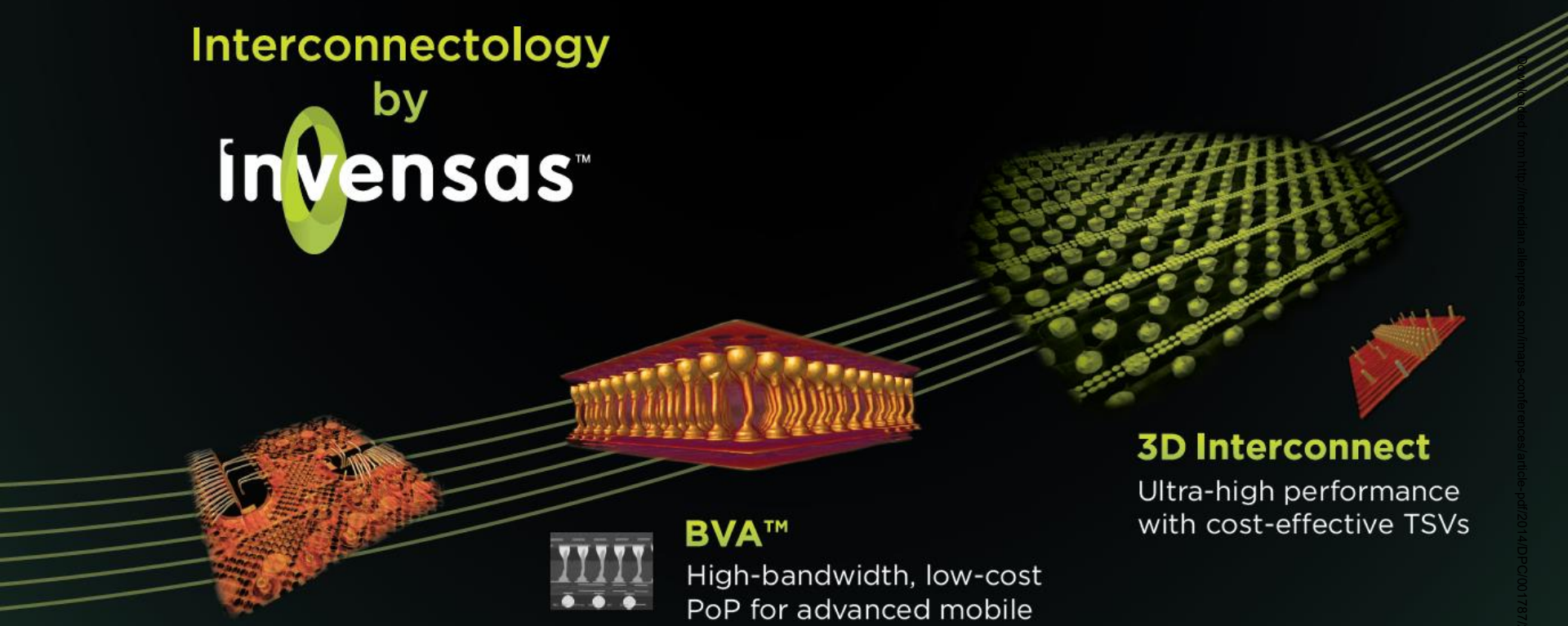

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