Dr. Steve Bezuk
Senior Director IC Packaging Engineering
Qualcomm Technologies, Inc.

Challenges and Directions in Mobile Device Packaging

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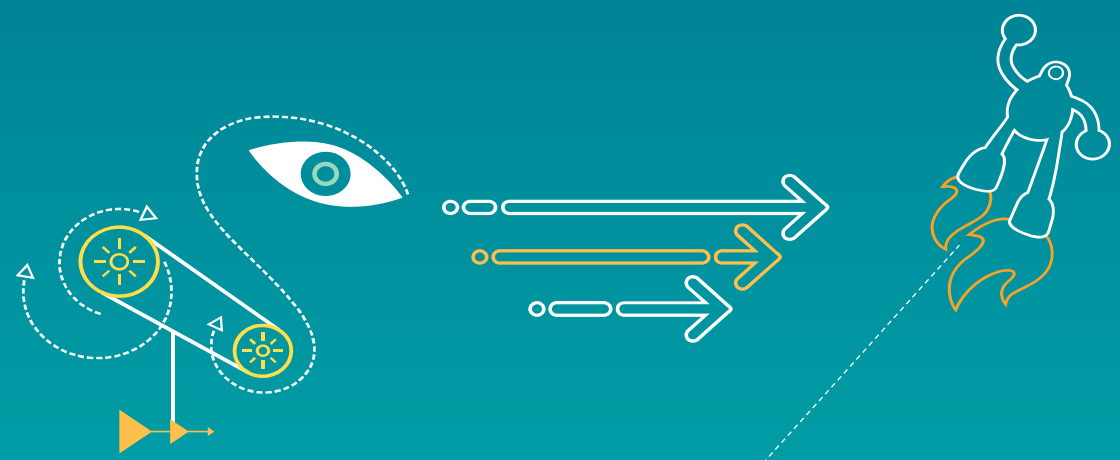

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This presentation includes a discussion of "non-GAAP financial measures" as that term is defined in Regulation G. The most directly comparable GAAP financial measures
and information reconciling these non-GAAP financial measures to the Company's financial results prepared in accordance with GAAP have been included at the end of this presentation.

Throughout today's presentations we refer to "Qualcomm" for ease of reference. However, please recall that in connection with our Fiscal 2013 reorganization, Qualcomm Incorporated continues to operate QTL and own the vast majority of our patent portfolio, while Qualcomm Technologies, Inc., its wholly-owned subsidiary, now operates, along with its subsidiaries, substantially all of our products and services businesses, including QCT, and substantially all of our research and development functions.

Market Drivers

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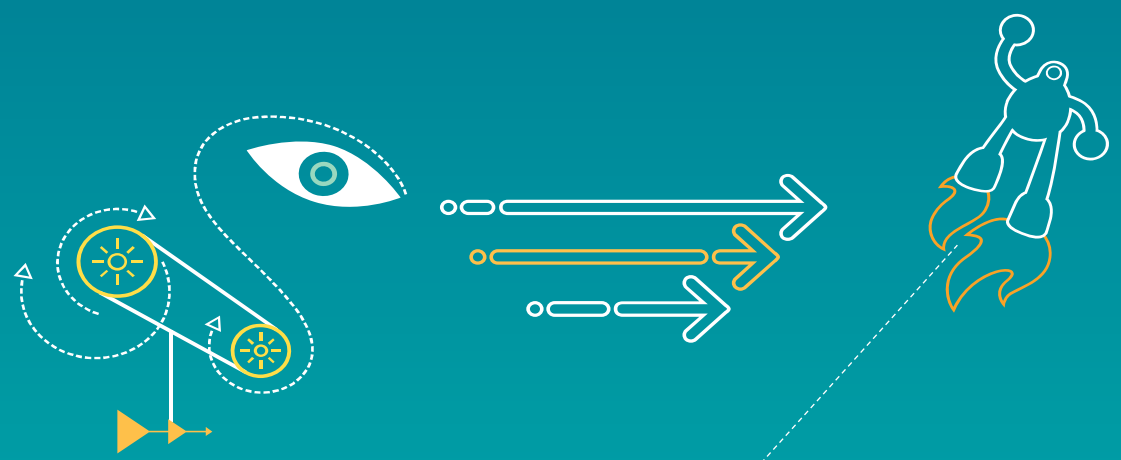
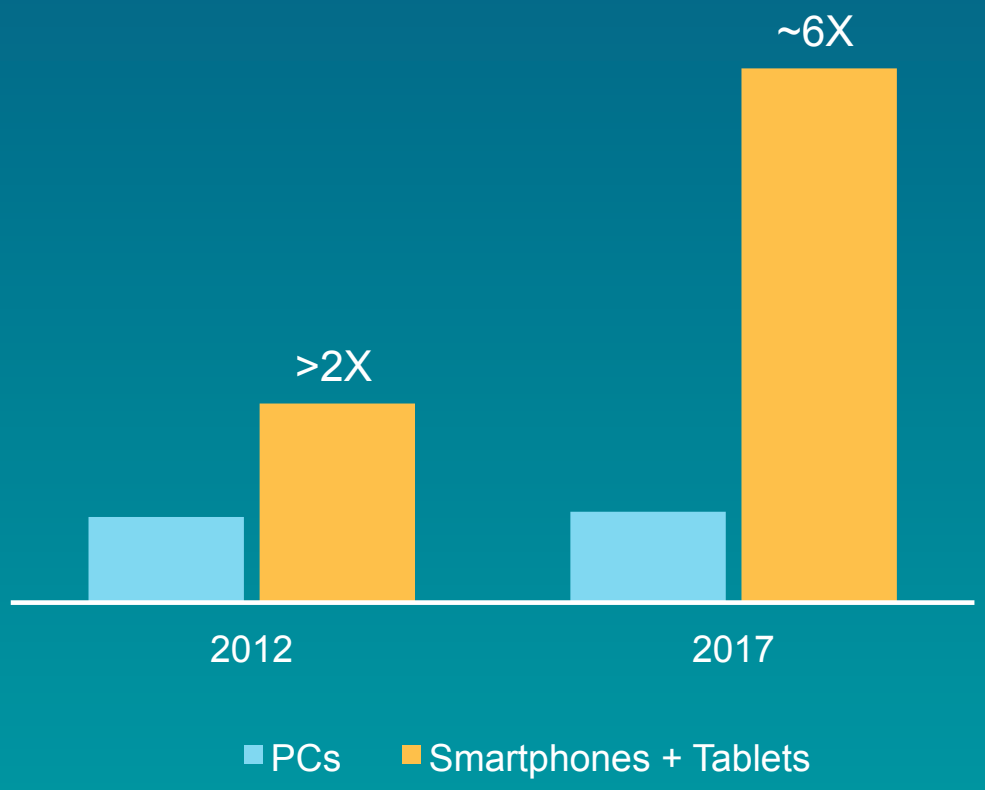


A new era: mobile drives growth and innovation in computing (and packaging)

Device shipments



Semiconductor revenues

$51B — 2012 — $68B

$56B — 2016 — $90B

PCs

Mobile devices

Source: Smartphones units: Gartner, Mar-13; Tablet units: Avg of Gartner, Mar-13 & SA, Apr-13; PC units (desktop + portable): Avg of Gartner, Mar-13 & IDC, Feb13; Semiconductor revenue: Gartner, Dec. '12; Mobile devices include mobile phones and tablets.

Continued smartphone momentum

~20% CAGR for smartphone unit shipments expected between 2012-2017

~7B

Cumulative smartphone unit shipments forecast between 2013-2017

Source: Gartner, Sept '13

Smartphone: our most personal device

~106
Avg. number of daily app launches by US Android users

~75%
18-24 year olds reach for it immediately after waking up

~94%
Use their device to look for local information

~79%
Watch video on their device

Sources: comScore custom research avg. over Q3'13, IDC Mar '13, Google May '13

Technology Requirements

- Performance, Features and Industrial Design (ID)
- New materials and constructions

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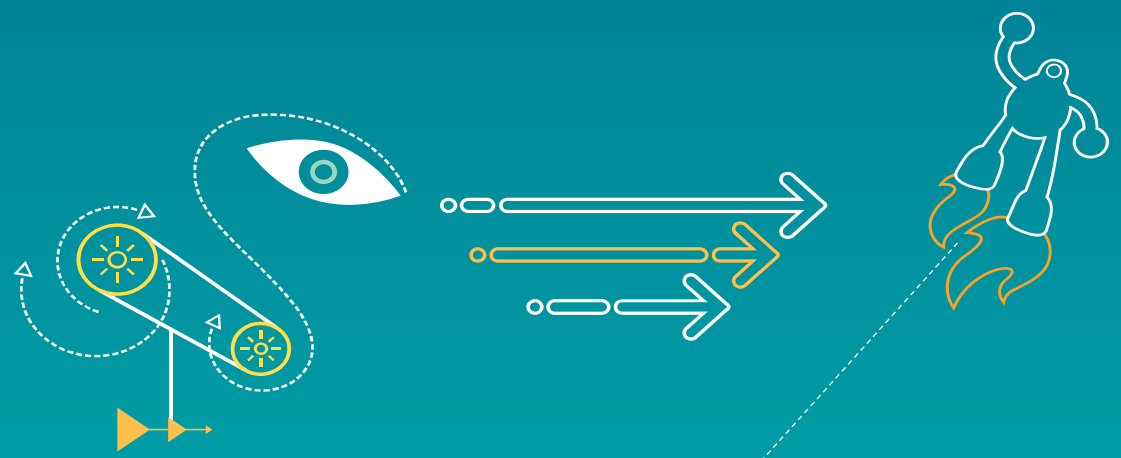


Technical Challenges for Mobile Applications

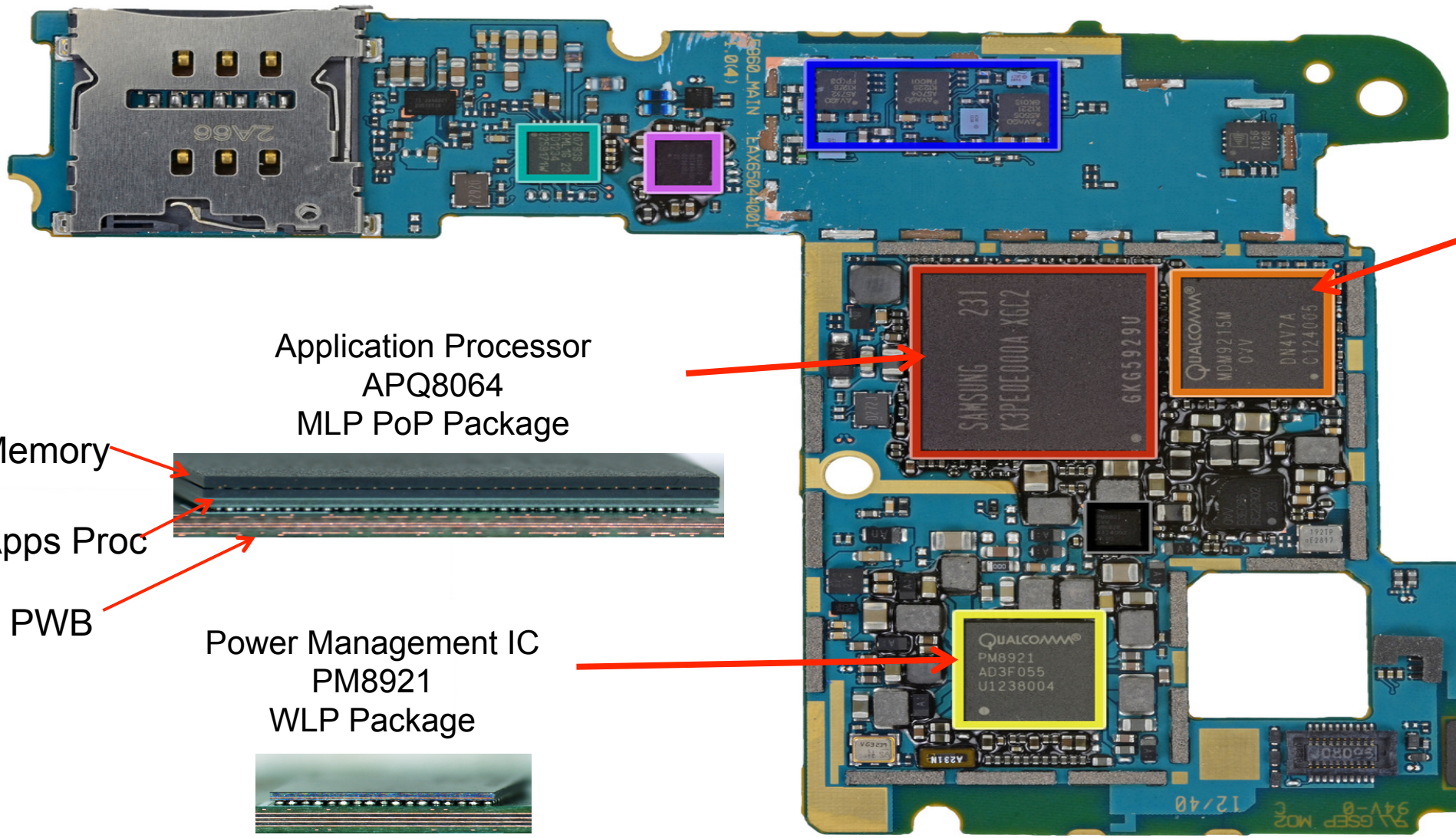
Materials and Processes
- Low K and Lower K dielectrics
- Fine pitch Cu Pillars/uBumps (<100um pitch)
- Low CTE, High Modulus Substrate Materials
- High CTE Mold Materials

Mechanical Challenges
- Ultra thin die (<150um)
- CTE mismatch
- Warpage Control
- Preserving Si Strain Eng. And E. Perf. (eCPI)

Thermal Challenges
- Higher Tj (>100C°)
- Poor thermal paths
- No air flow, Closed system
- 3D integration

Electrical Challenges
- Signal Integrity
- Power Distribution Network
- Functional Partitioning

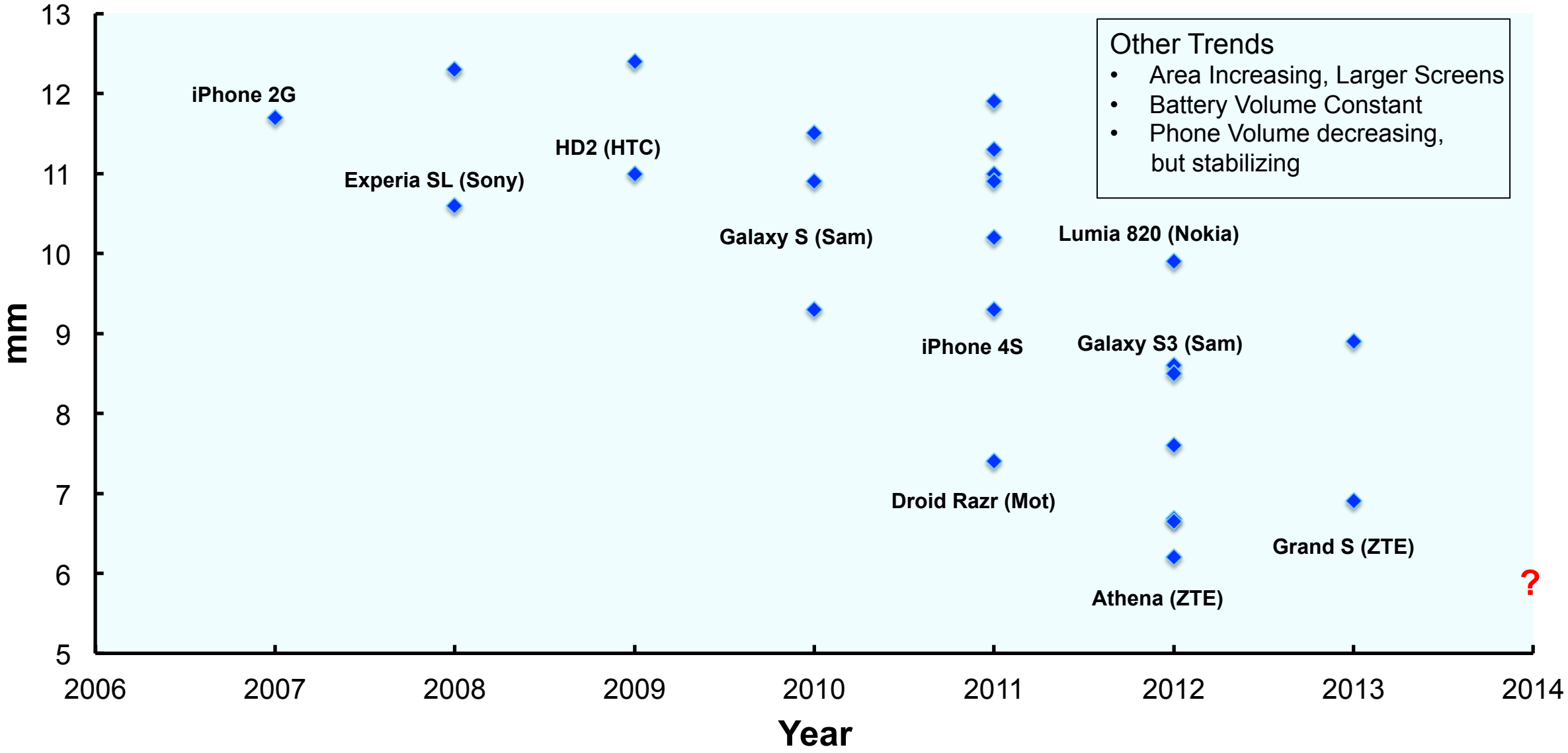
Mobile package styles (Nexus 4 Phone Board)



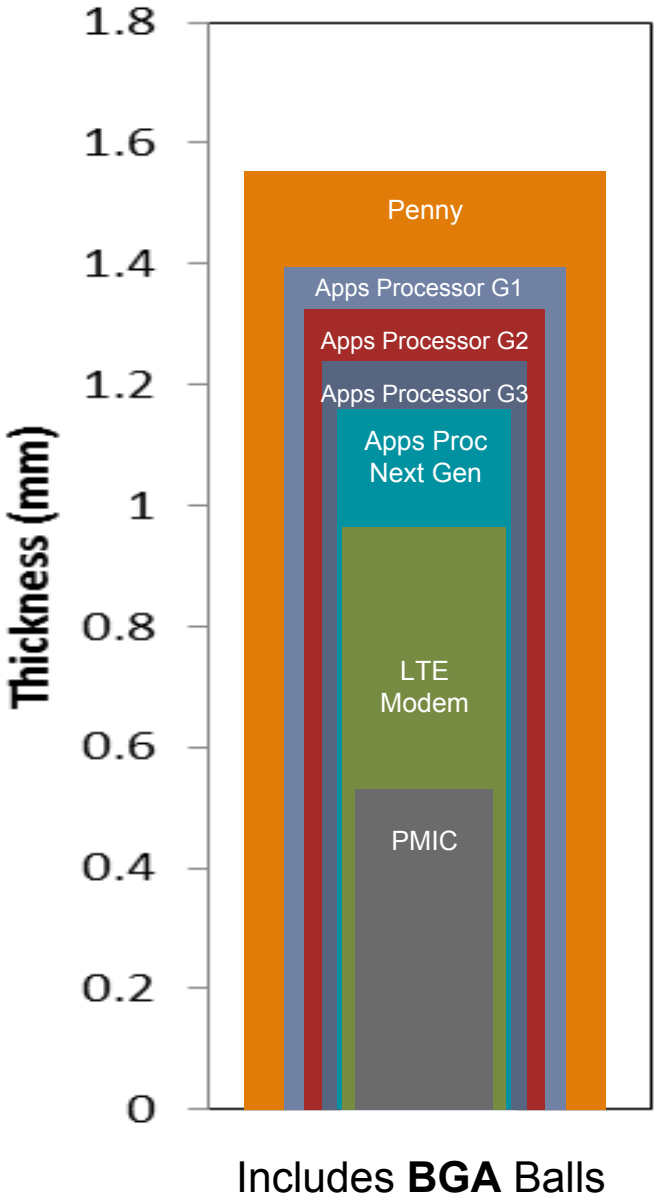
Fine Pitch Packages (≤0.4mm BGA pitch, up to 1000 I/O, in <15mm package)

iFixit

Handset Thickness Decreasing Over Time - where will it stop?

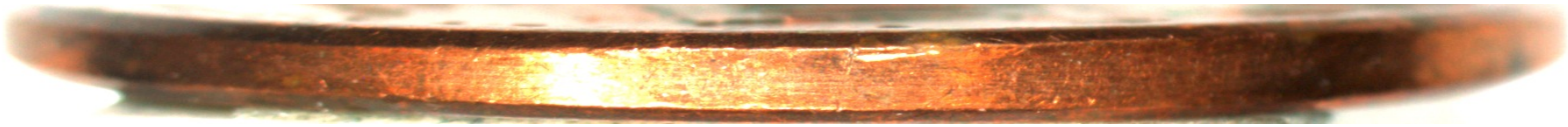


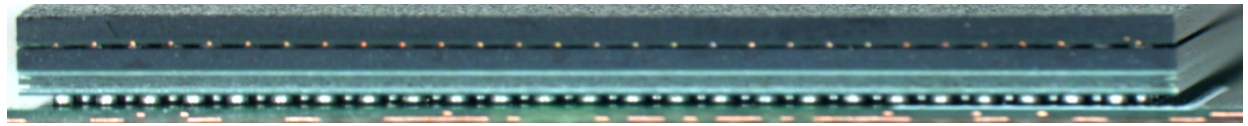
Thickness Comparison of Qualcomm Mobile Packages



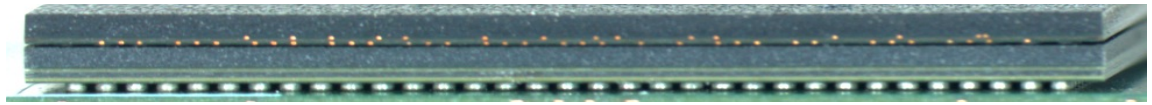
Includes **BGA** Balls

Standard issue US Penny

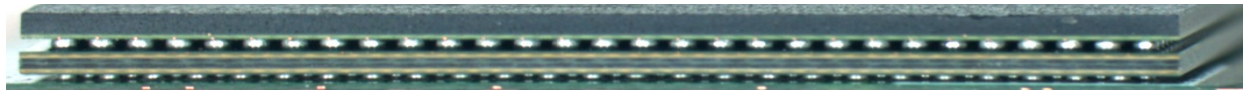




Apps Proc Molded Laser PoP*

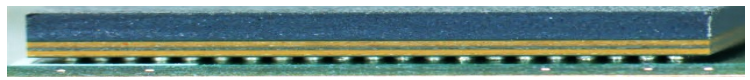


Apps Proc Molded Laser PoP*



Apps Proc Bare Die PoP*

Apps Proc Next Gen PoP*

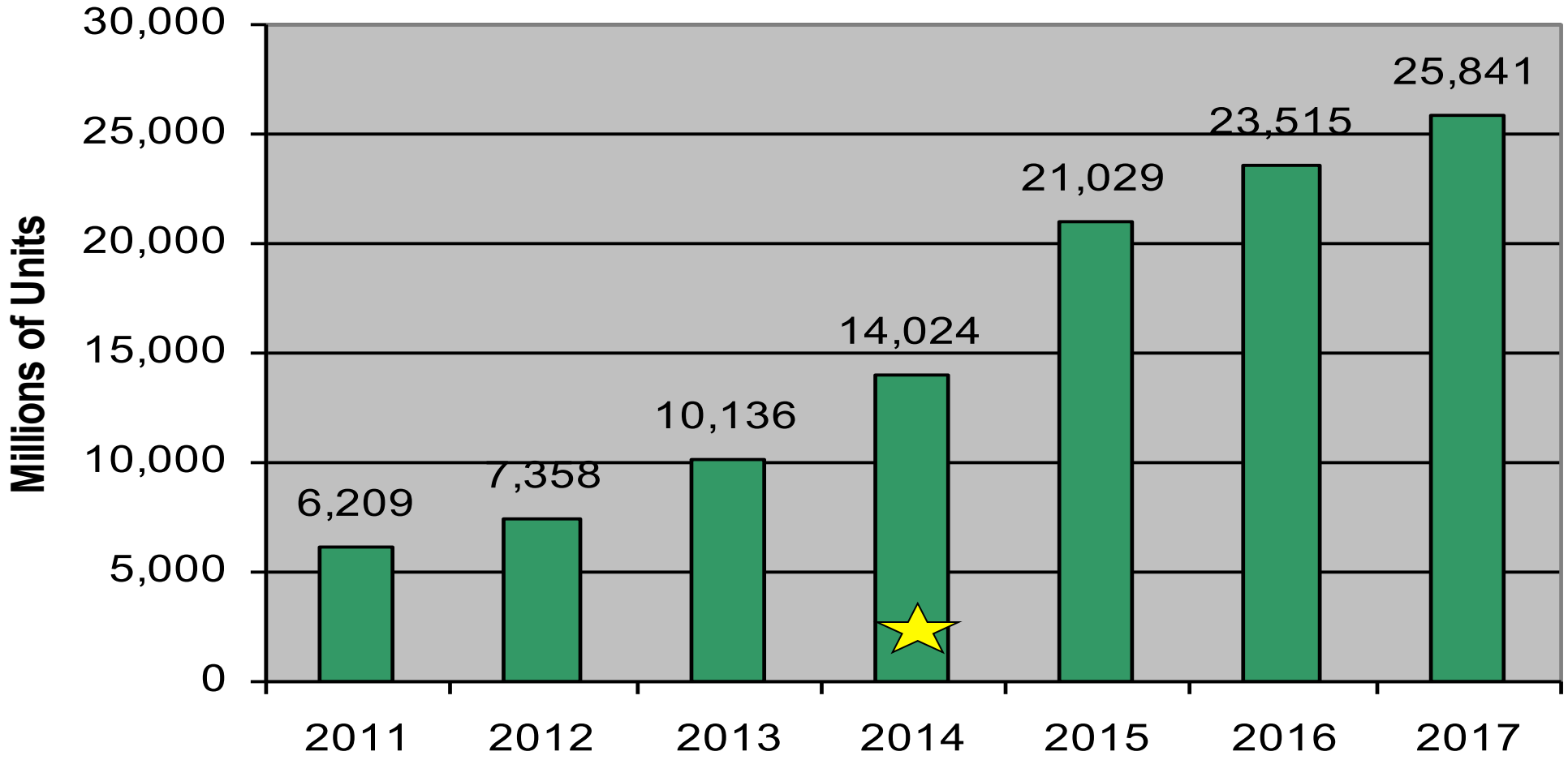


LTE Modem Hybrid (FC & WB)

PMIC WLP

*PoP Package thickness includes memory

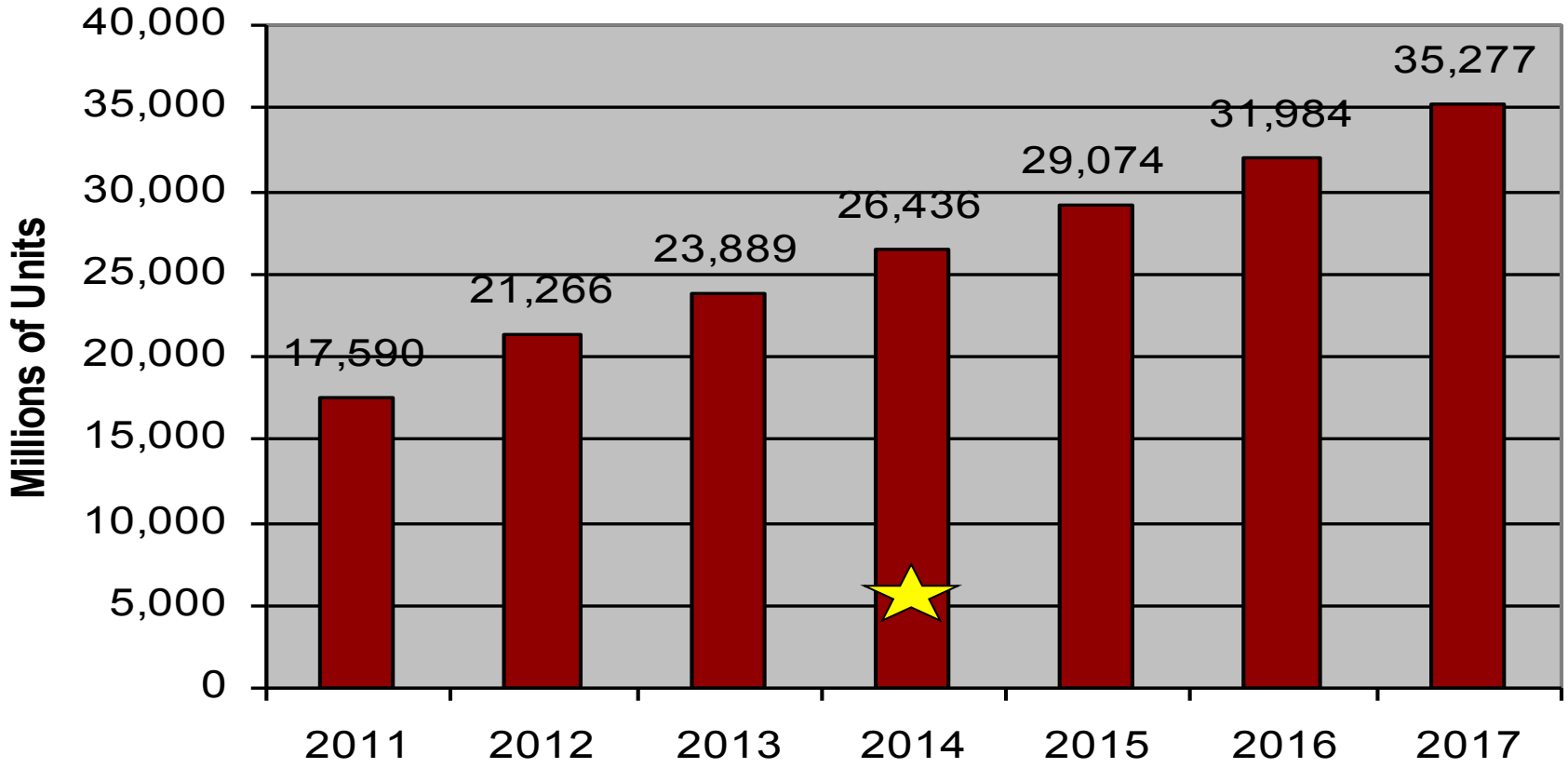
Projected Demand for Flip Chip in Package



- CAGR of 22%is projected 2014 to 2017

Source: TechSearch International, Inc.

Projected Demand for WLP



- Demand for WLPs remains driven by growth in mobile phone shipments
- CAGR of 10% is projected for 2014-2017

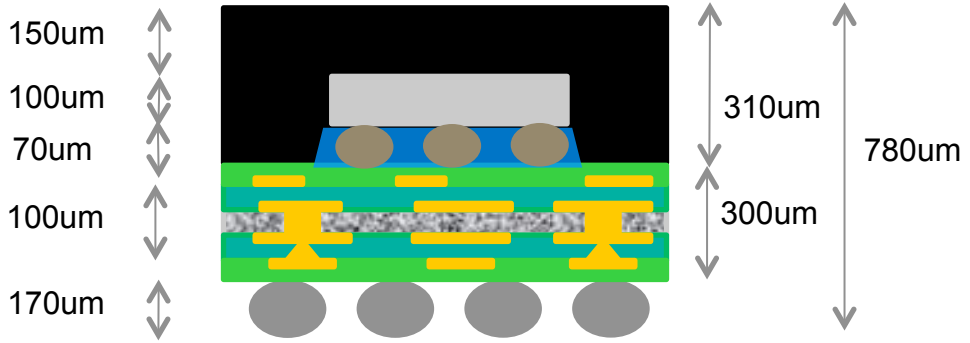
Source: TechSearch International, Inc.

FC CSP Package Structure

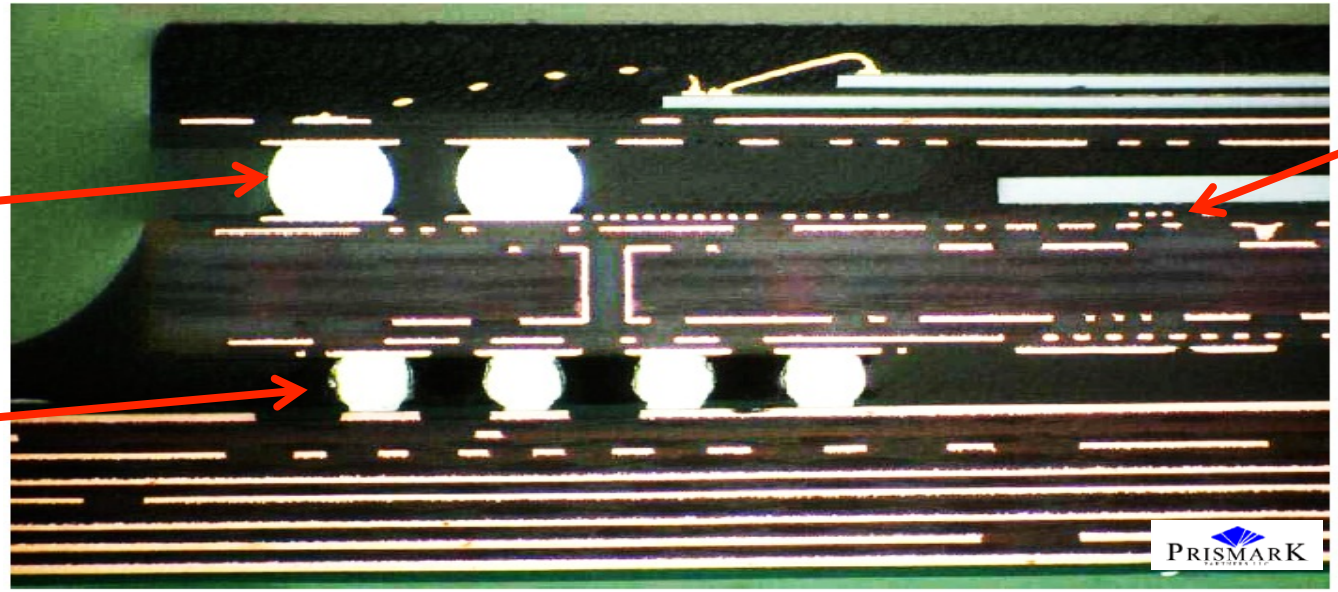
FC CSP

- Warpage difficult to control in thin pkgs.
  - Substrate core thickness and CTE
  - Mold thickness over die
  - Die thickness (ratio of Si/EMC)

- Solder balls are a significant fraction of the total package height



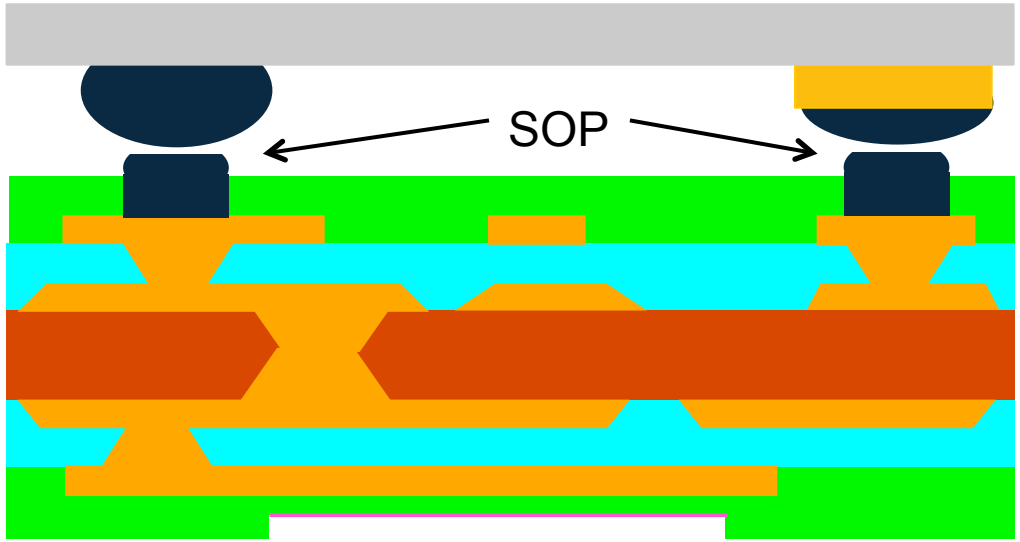
Not to Scale
Typical Dimensions



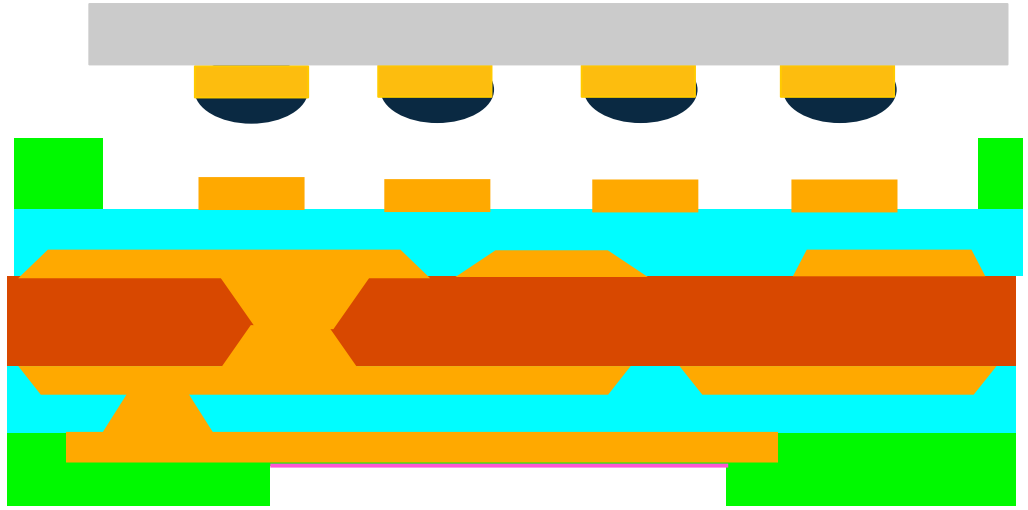
Bare die FC PoP package with stacked memory

Fine Pitch Flip Chip Interconnect Trends for Mobile Packages

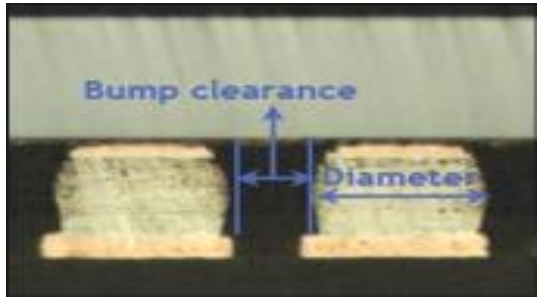
FC Interconnect using SOP

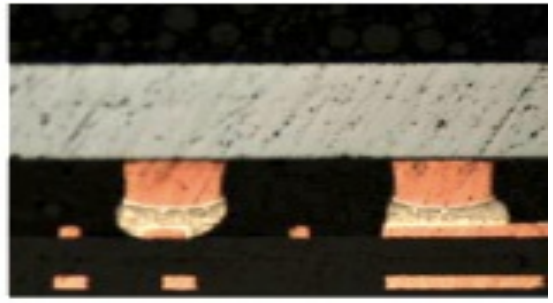


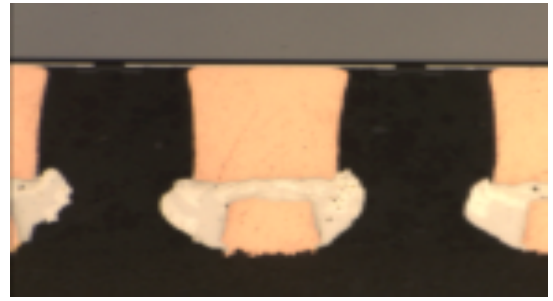
Fine Pitch FC used in mobile devices



Mass Reflow (MR) FC (≥140 um) | CuBOL(≥100 um) | TCFC (≤80 um)





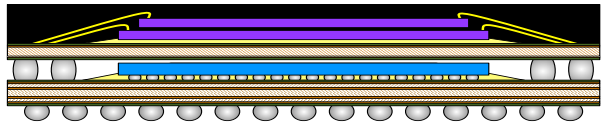


- Conventional solder bump flip chip

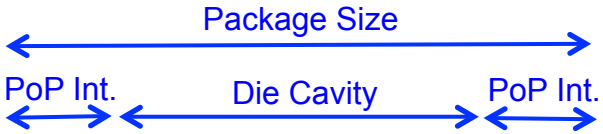
- Substrate uses narrow bond leads instead of flip chip pads, and die uses Cu pillars w/ SnAg solder cap
  - CuBOL: Cu pillar bond on lead mass reflow chip attach
  - TCFC: thermo-compression flip chip attach

FCCSP PoP package structure thickness trends

Current POP packages

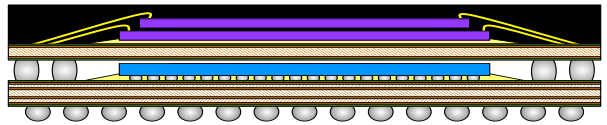


FC Bare Die PoP

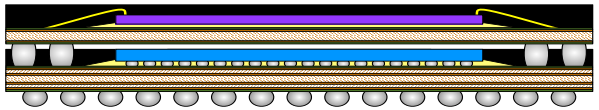


Molded Laser PoP (MLP)

Thinner POP packages

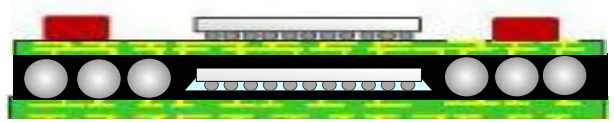


Thin core or coreless
Bare Die



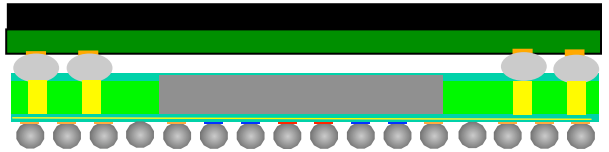
Exposed Die
Molded Laser PoP

Pseudo-Embedded POP packages



MCeP
(Shinko)

Embedded POP packages



3D eWLB
(STATSChipac)

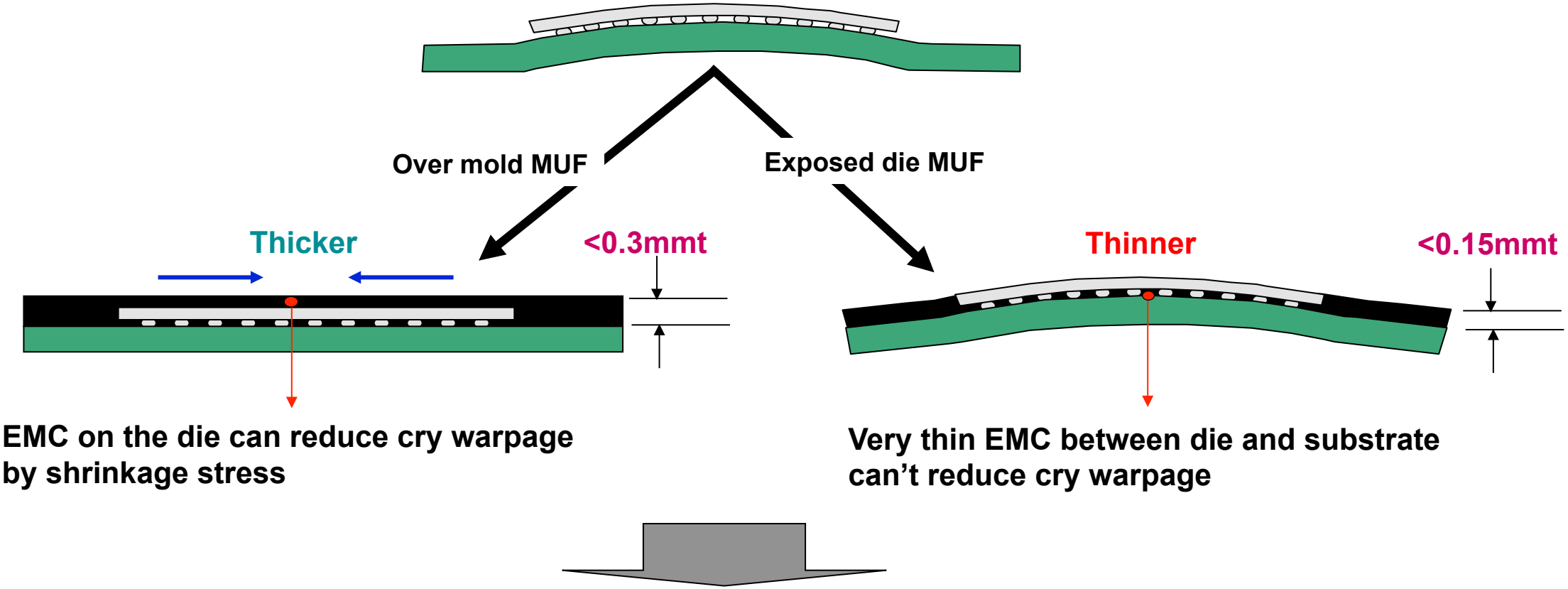
Thinner

Warpage control more difficult

Warpage control easier

Using EMC Shrinkage to Control Warpage

- Large warpage of large & thin exposed die FCCSP



- Direction of EMC property for low cry warpage

  High Mold shrinkage
  High Modulus for large shrinkage stress

Courtesy of Masashi Nakamura – Panasonic Corp.

Controlling Warpage Through Substrate CTE and Modulus (Simulation)

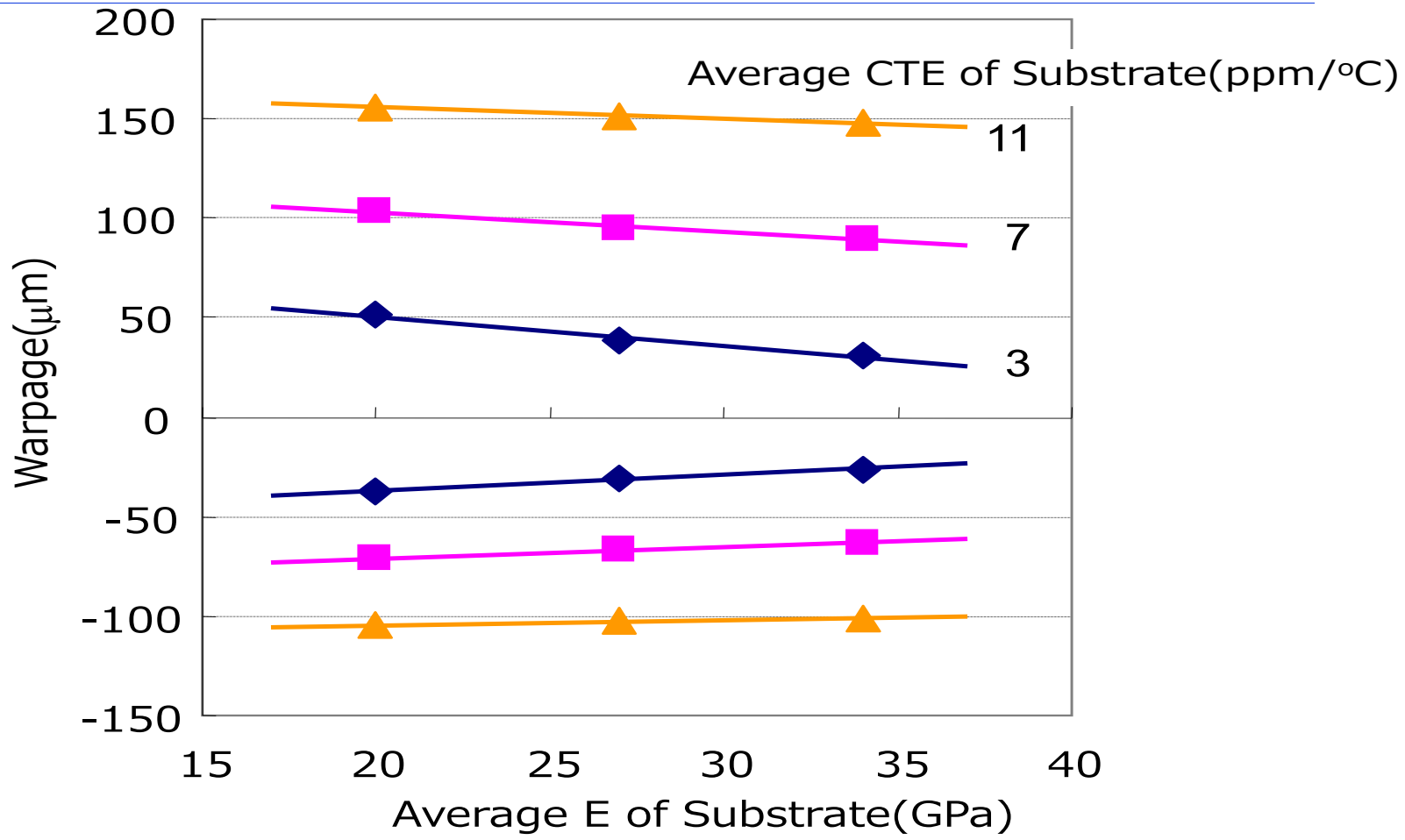
*Warpage

@25°C

(+) : convex

@260°C

(-) : Concave



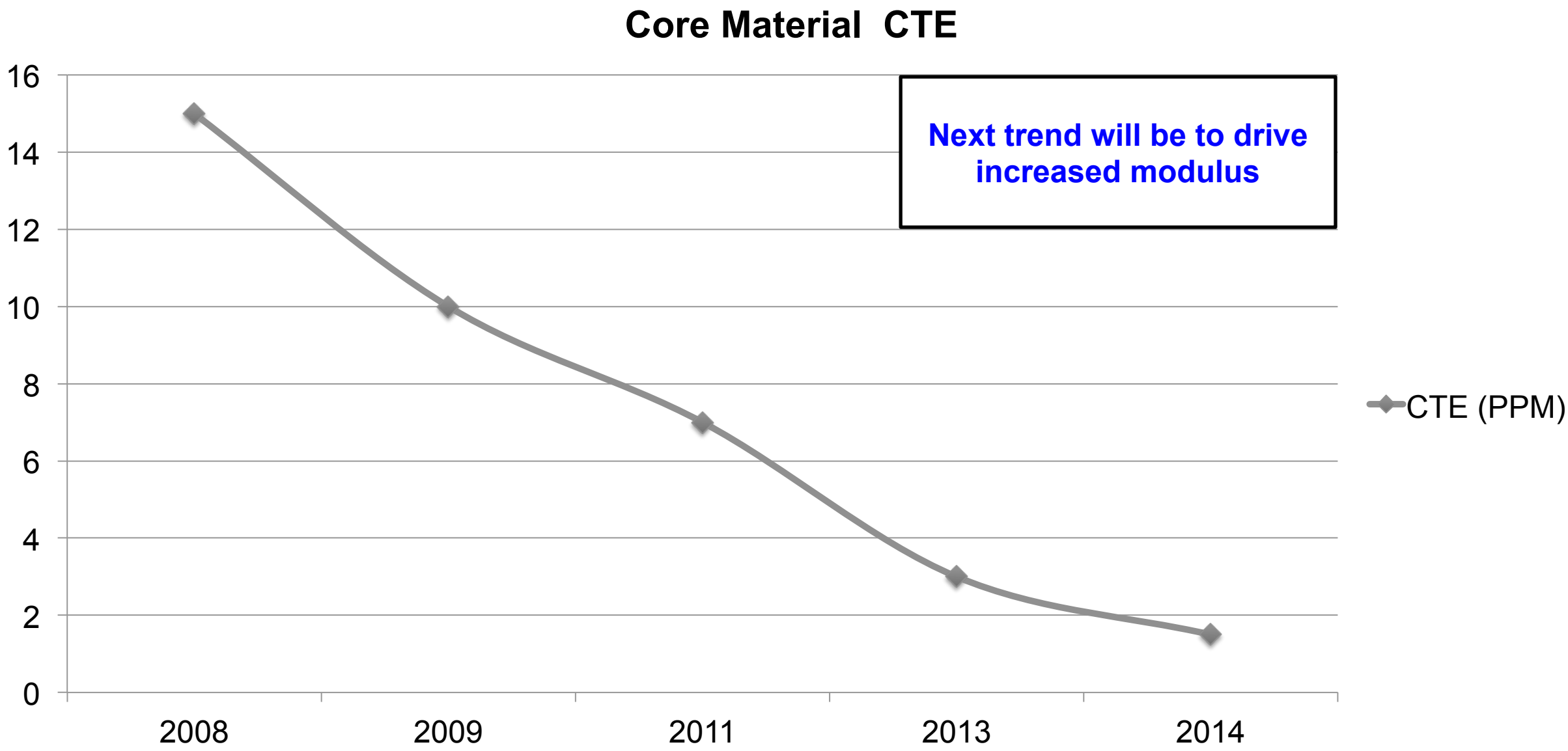
Low CTE and High Modulus are effective for controlling warpage

Courtesy of Takahiro Tanabe – Hitachi Chemical

Substrate manufacturing trends – Strip based

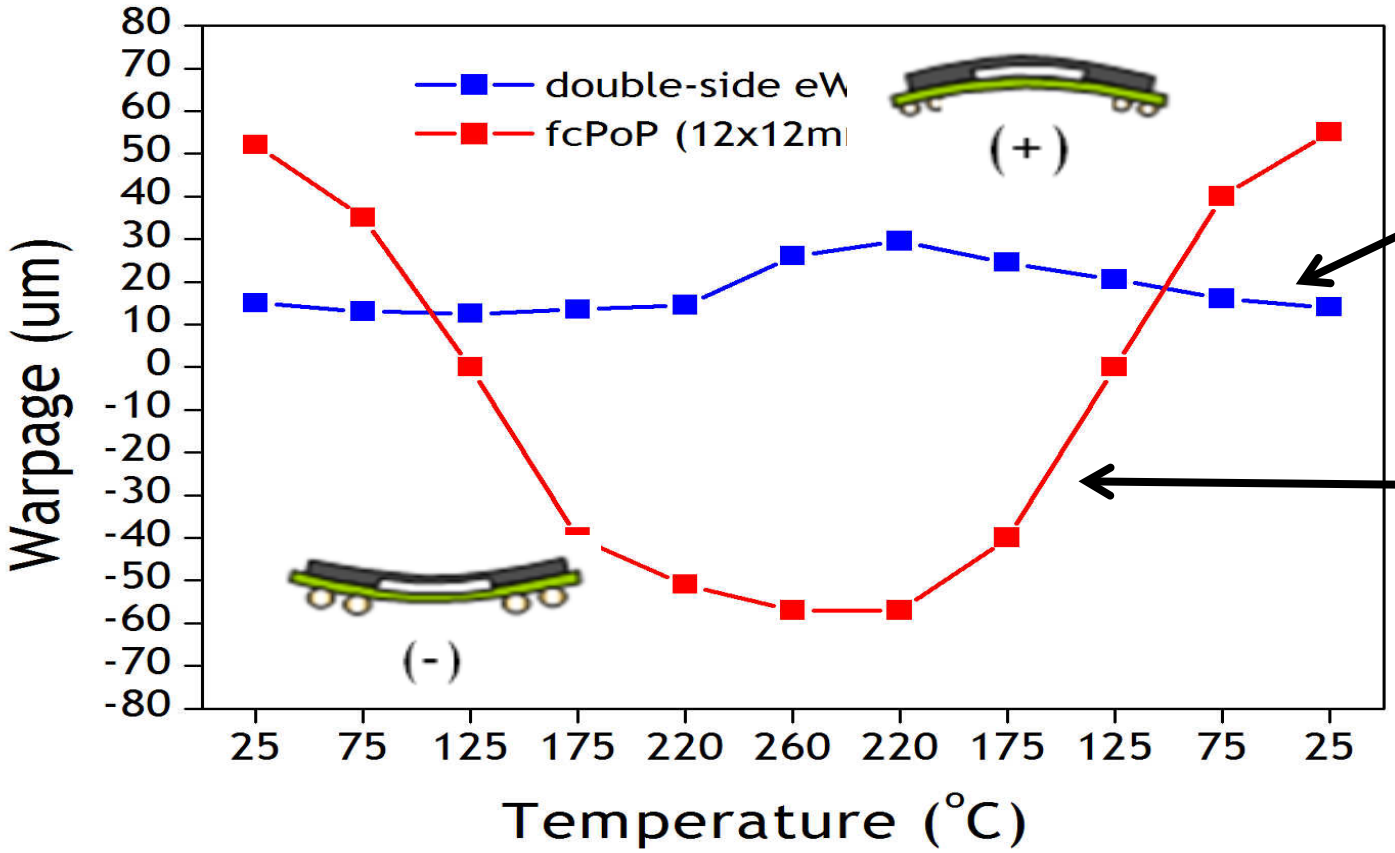
	2008 HVM	Current 2014 HVM
Patterning Method (um)	mSAP (30/30)	SAP (15/15)
Min FC Pitch (um)	150	40/80
Core material CTE (ppm)	15	3
Via count per panel	1x	2x
Layer count	2L & 4L	2L, 4L & 6L
# of Mfg Steps	1x (2L)	3x (6L)
Decoupling solution	None	Embedded Capacitors
Buildup dielectric	Prepreg	Prepreg, ABF
Coreless	No	Prepreg, ETS

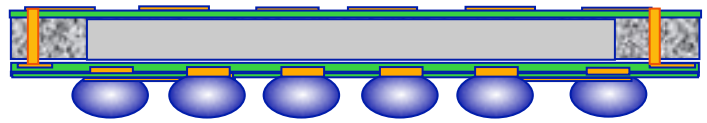
Substrate Core CTE changes in last 5 years to control package warpage



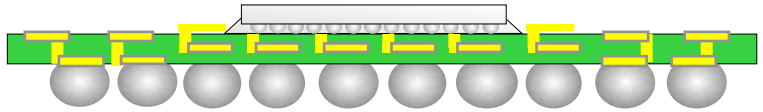
Warpage Control using package construction – 3D eWLB

Double sided eWLB





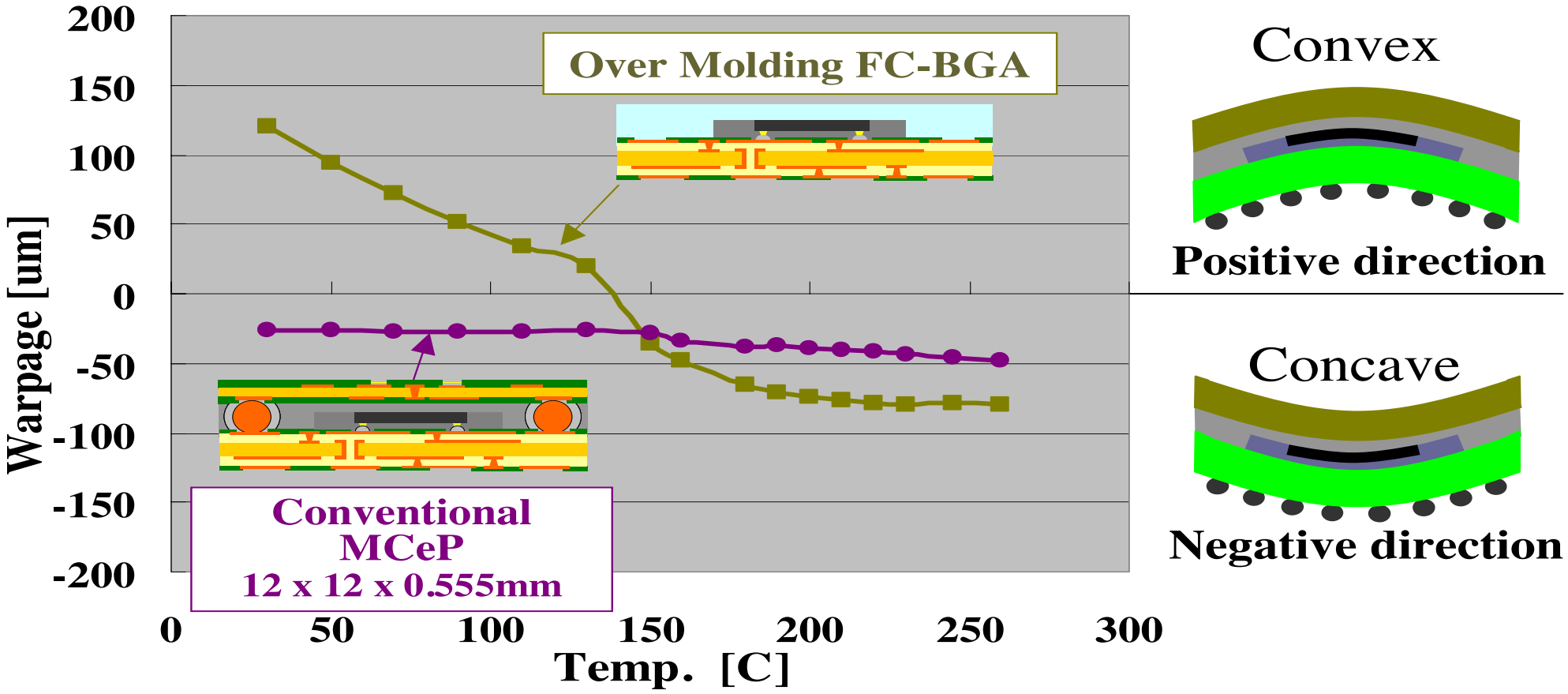
eWLB 12x12mm, 396I/O
PKG height 0.7 mm



fcFBGA-PoP-b,12x12mm, 516I/O
Substrate thickness 0.43 mm
Die 9 x 9.2mm

Courtesy of Hamid Eslampour – STATSChipPac

Warpage control inherent in MCeP package construction

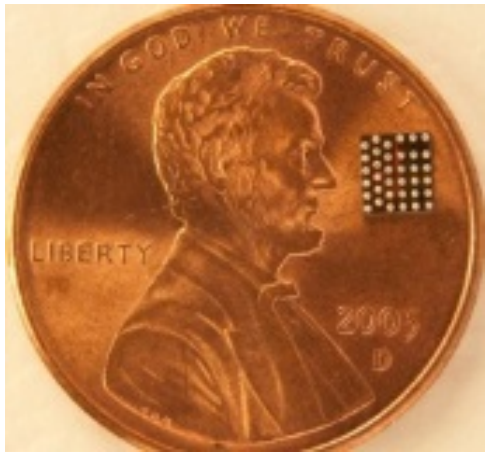


Courtesy of Mitsuharu Shimizu- Shinko

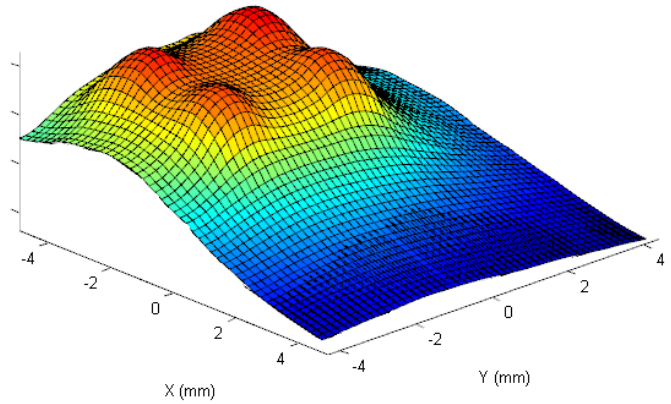
Thermal Issues

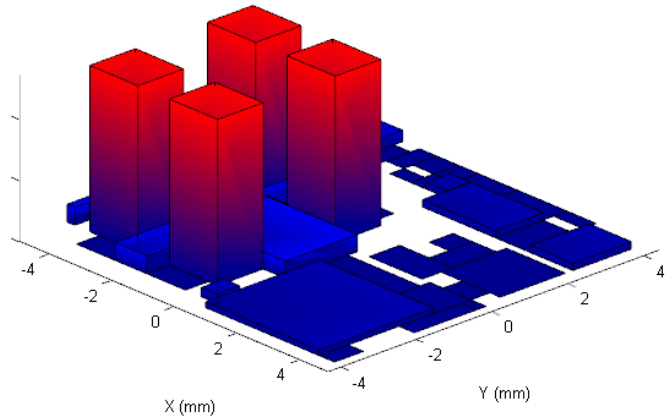
- None of the Trends in Mobile Space is in Favorable for Thermal Management

- Rapid integration at silicon level and silicon node shrink is increasing the heat density
  - Doubling up transistor count at each node at constant die size
  - Packages as small as 4mm^2 performing sophisticated functions such as RF and power mgmt.



≈ 2x2mm WLP package





Heat density plots of a quad-core package

Future Technologies:
2.5, 3D, Modules, ?

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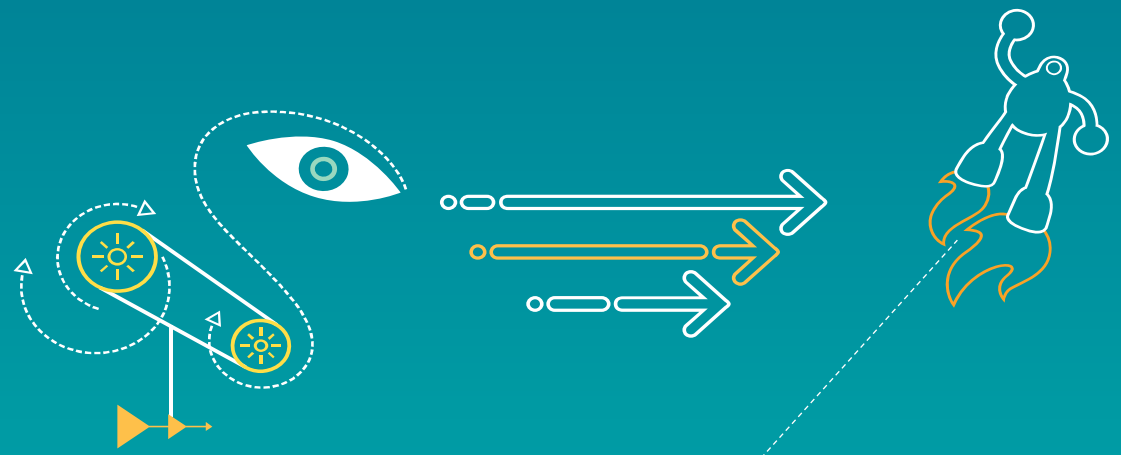
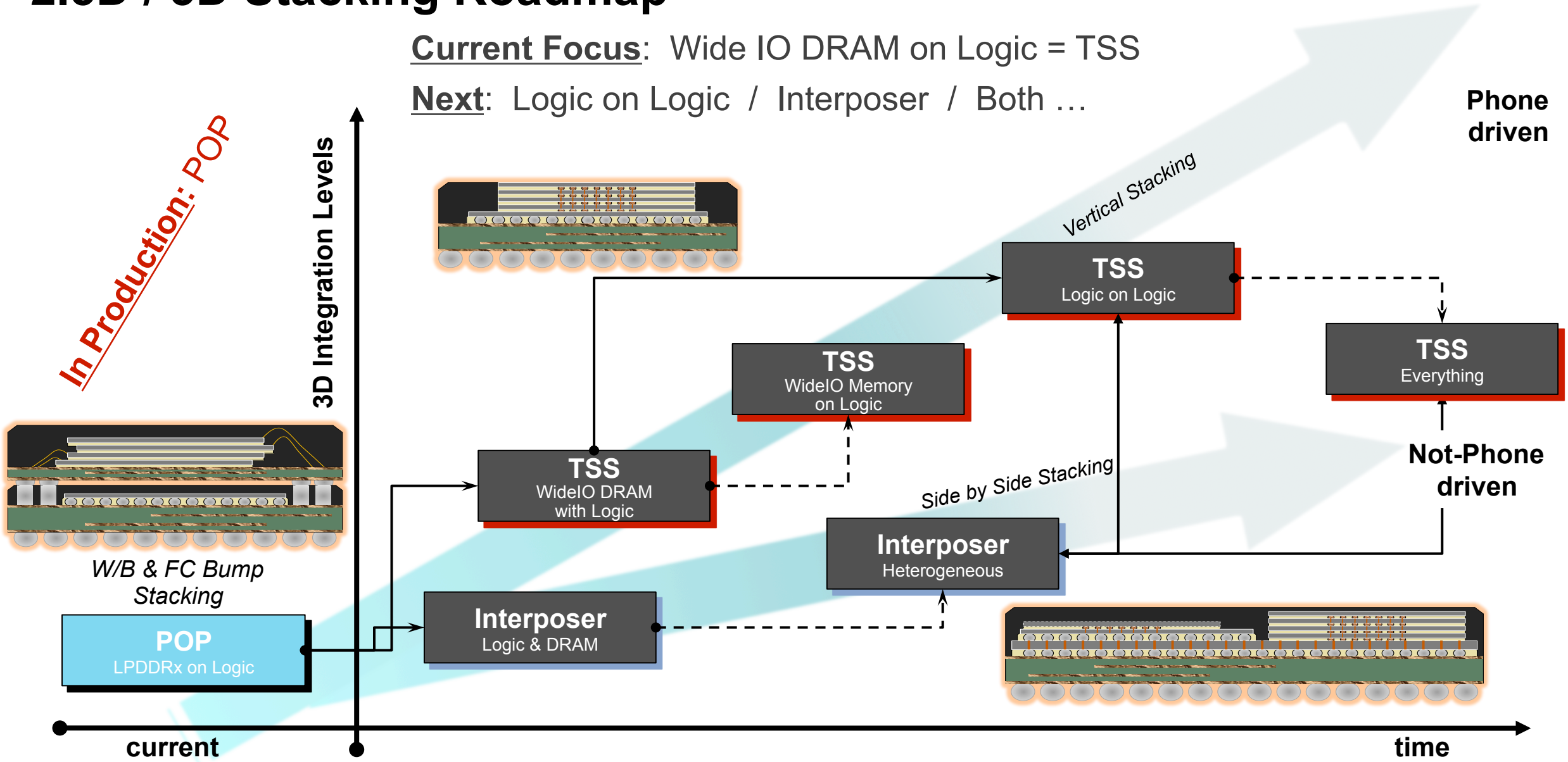


2.5D / 3D Stacking Roadmap

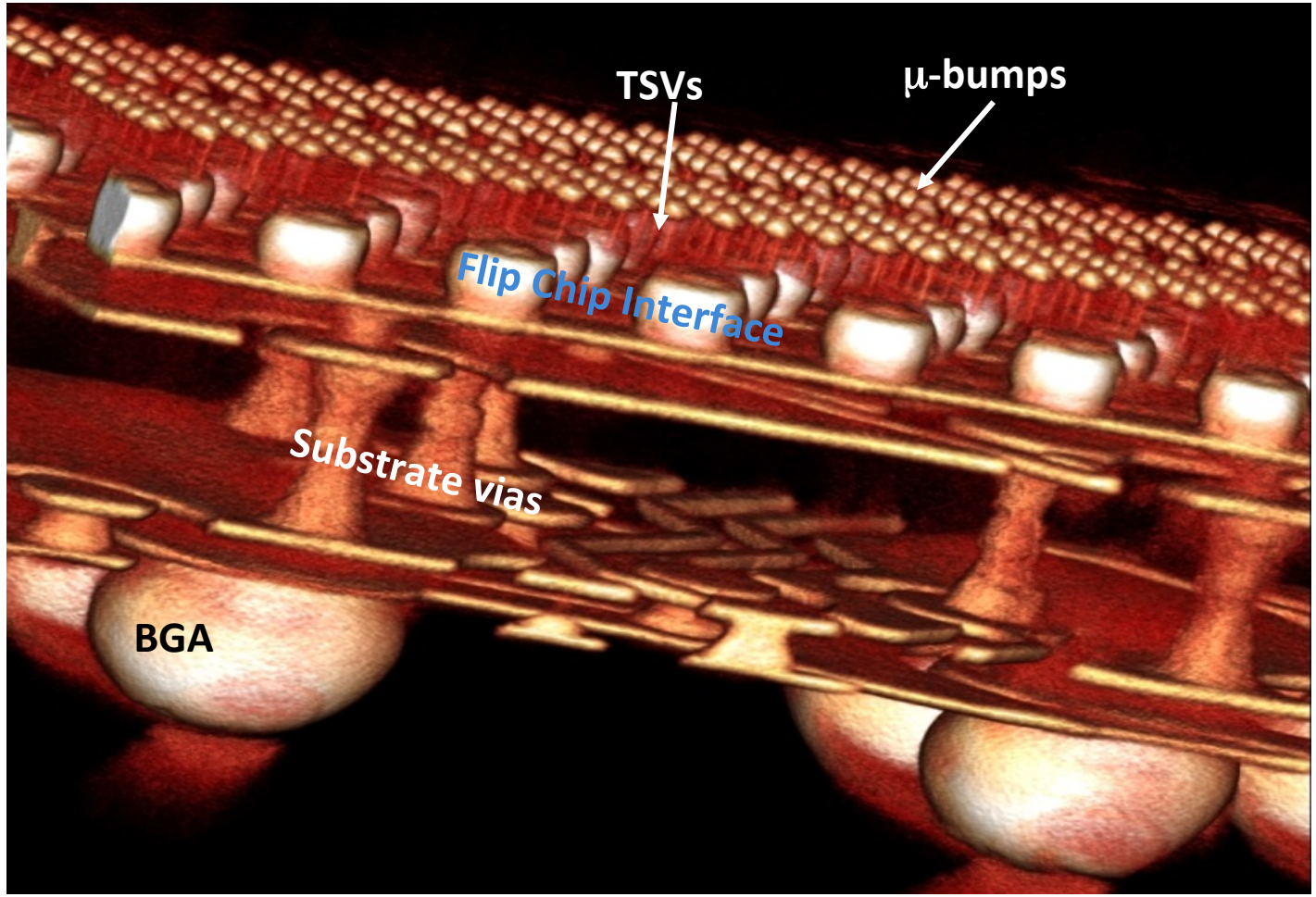
Current Focus: Wide IO DRAM on Logic = TSS

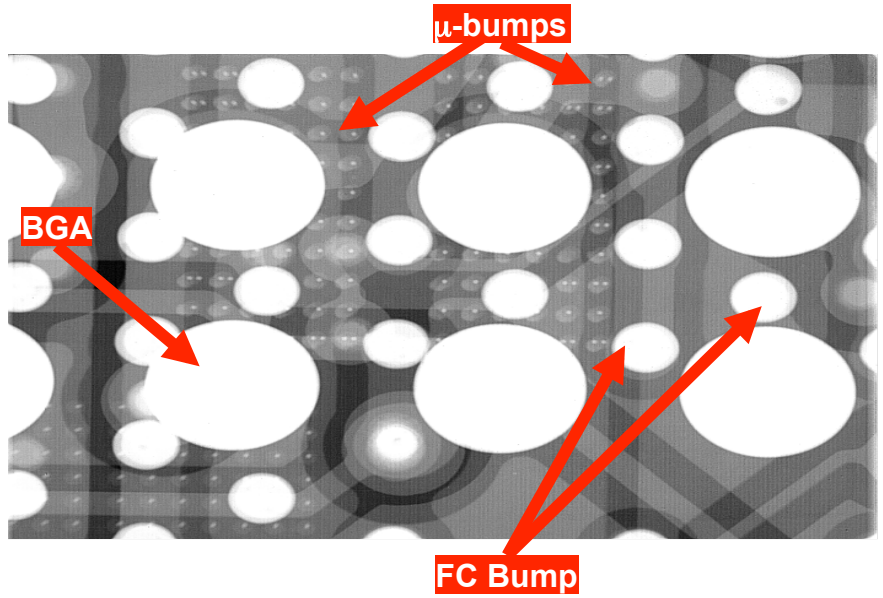
Next: Logic on Logic / Interposer / Both …



3D X-Ray Image of TSS

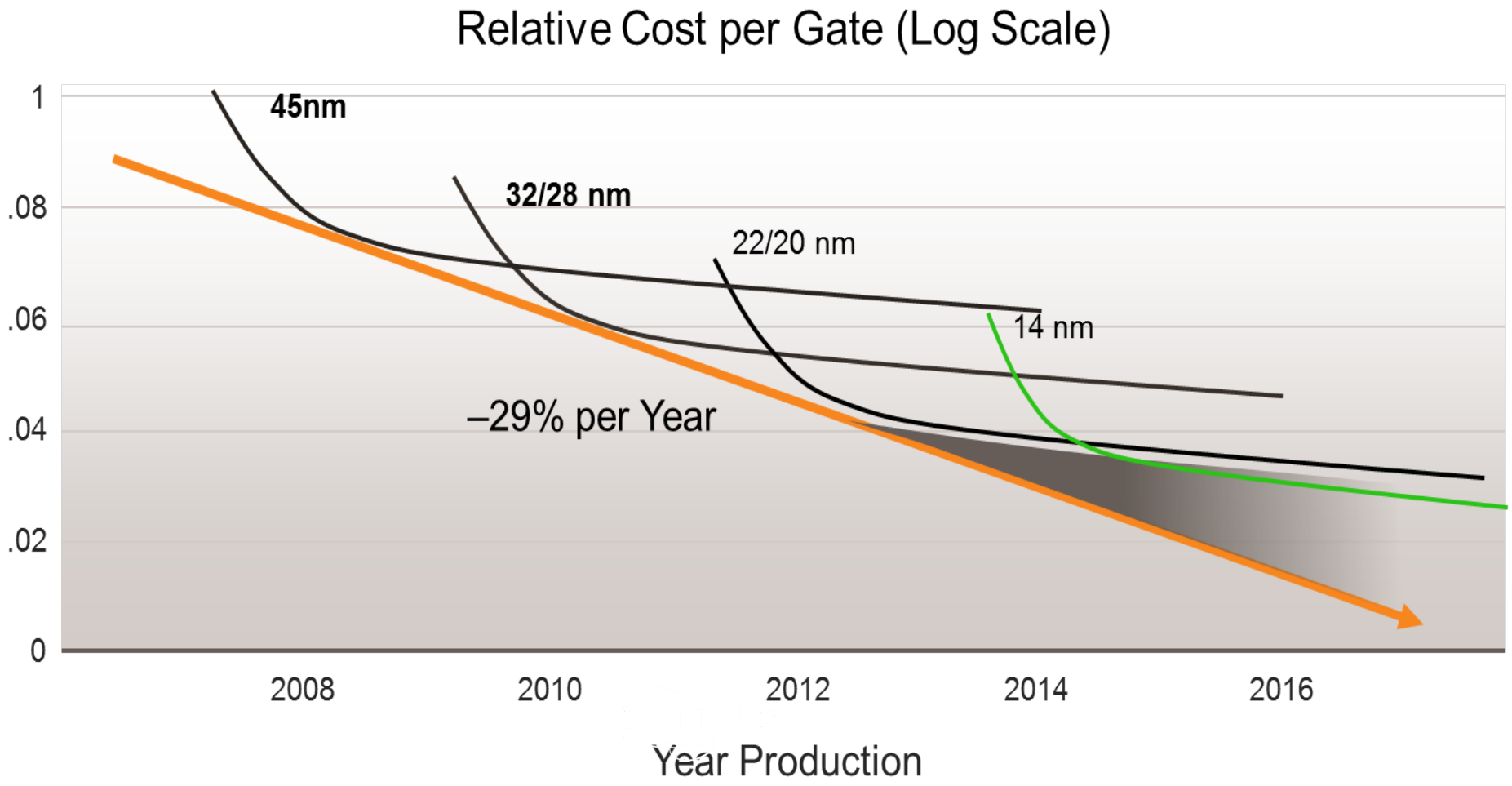
- X-Ray Tomographic images show well-formed features



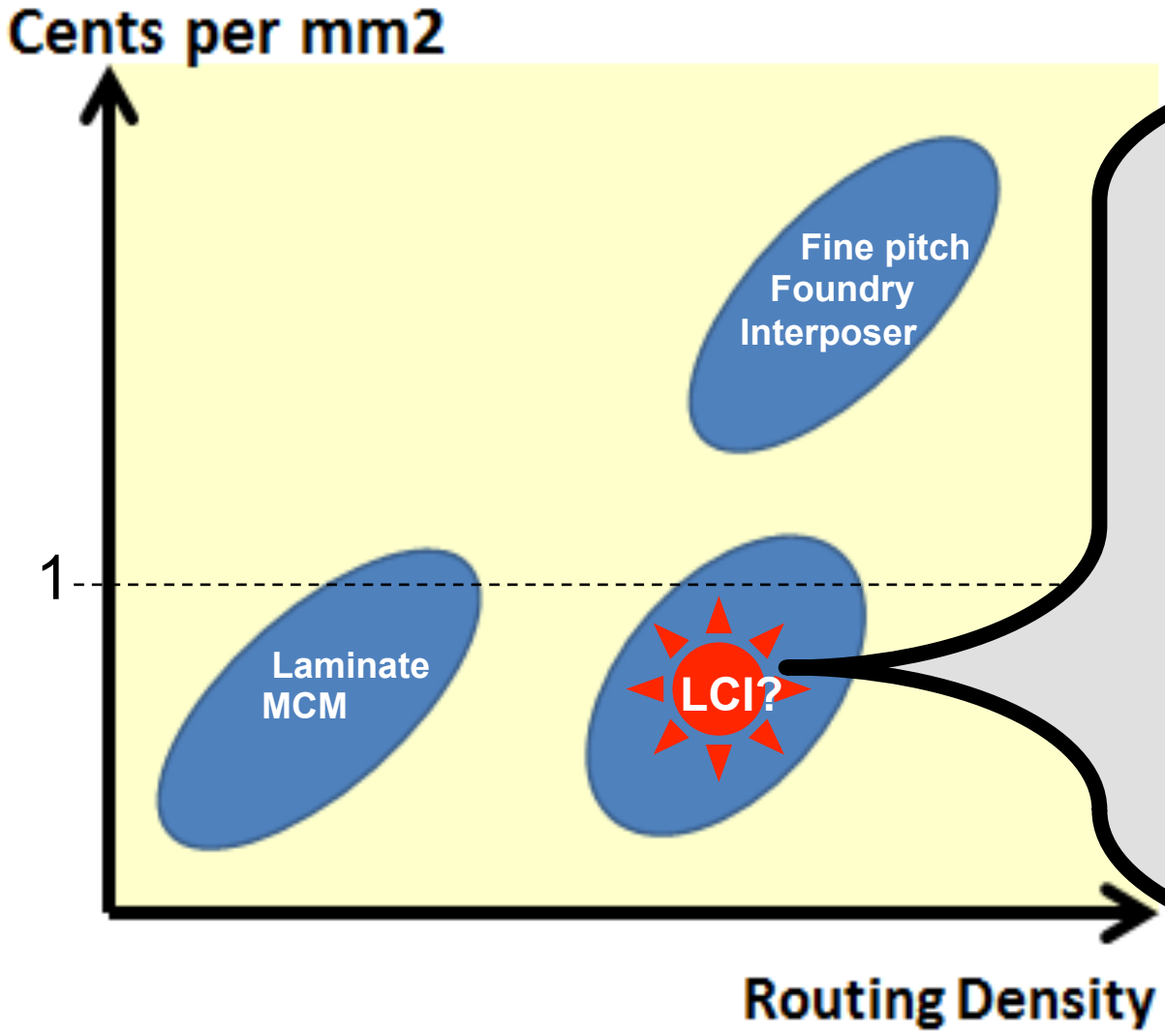


TSV Logic on Logic and LCI: Motivation

- **Semiconductor future will be a series of disruptive technology changes**
  - End of conventional CMOS scaling but continue Moore's law with new devices (finfets, etc.)
  - Diminishing of the traditional 29% per year cost reduction megatrend



What's Next? -- Low Cost Interposer (LCI)



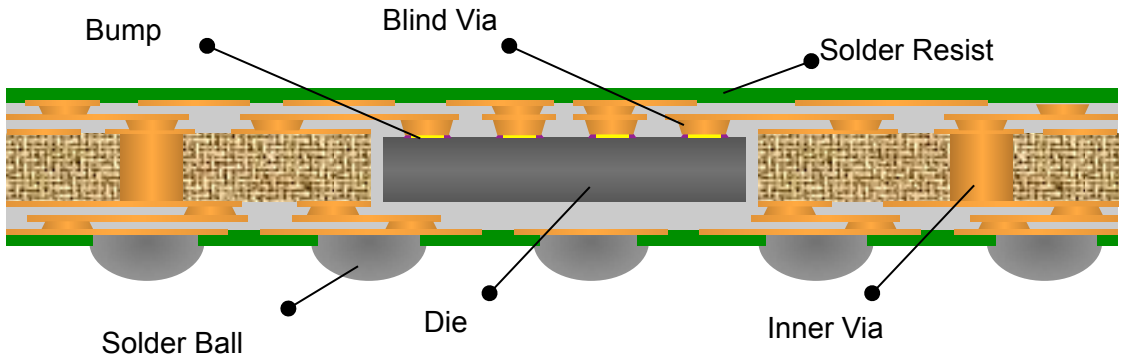
Format:

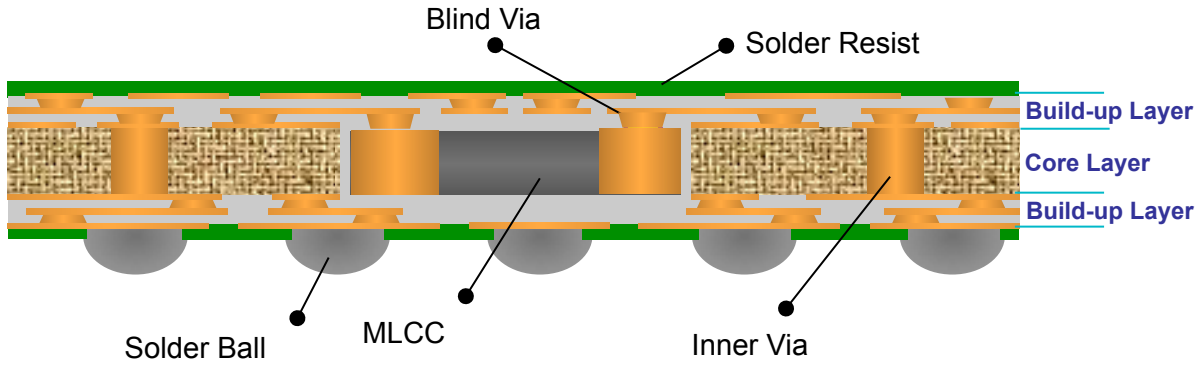
- *c-Si*
- *p-Si*
- *glass*
- *advanced laminate*
- *wafer, panel,…?*

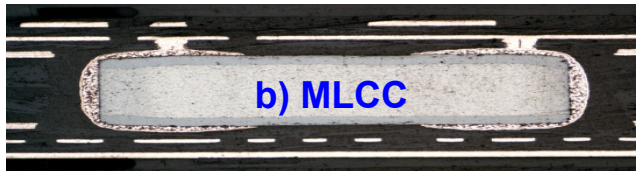
Supply Chain:

- *Wafer foundry*
- *OSAT*
- *display*
- *PV*
- *PCB, …?*

Embedded Substrate Description







Key Features

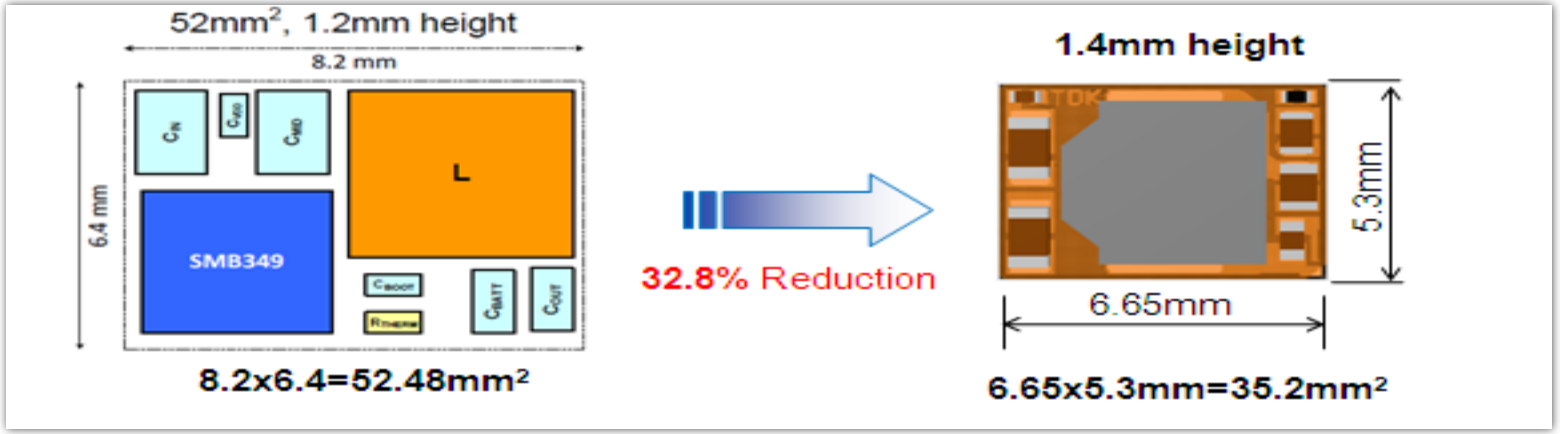
- ☞ **Component placed at the center of the thickness direction of substrate**
  - → Warpage resistive
  - → Good compatibility with conventional PCB process (lamination and laser via process)
- ☞ **No special equipment or foreign adhesive material inside the structure**
  - → Conventional SMT machine or FC bonder modified for large working and thin panel
  - → No adhesive resin used but only PCB resin is filled in the space (simple and highly reliable)
- ☞ **Enhanced power stability using both side interconnection of blind via (figure c)**

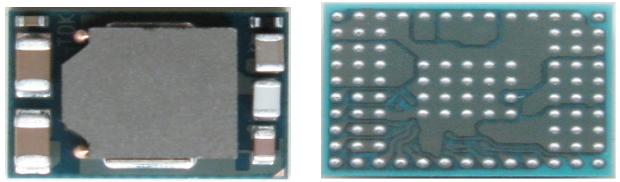
Courtesy of SEMCO (ACI group)

TDK SESUB Battery Charging Module

- Charge/input current: up to 4A
- Input voltage range: 3.7V to 15V
- Automatic DC Input evaluation
  - Automatic Power Source Detection
  - Automatic Input Voltage Detection
  - Automatic Input Current Limit
- Can support QuickCharge2.0 for 75% faster charging time
- Automatic float voltage compensation

Term	Description
APSD	Automatic Power Source Detection (USB BC1.2)
AICL	Automatic Input Current Limit
AFVC	Automatic Float Voltage Control
AIVD	Automatic Input Voltage Detection
HVDCP	High Voltage Dedicated Charging Port





User pad: 0.5mm pitch
13x10 matrix
94pads

Courtesy of TDK

Challenges and Directions for Mobile IC Packaging

- Tremendous growth in mobile devices worldwide
  - Drives need for innovation
  - Funds innovation
- IC Packaging is Challenged to meet form factor and bandwidth requirements
  - X, Y, and Z reductions
  - New Materials and package constructions need to be continually developed
  - Thermal management and solutions are significant issues for passively cooled closed systems
    - Can an effective low cost active solution be developed?
  - Low cost versions implementations of 2.5 and 3D required
  - Modules (higher integration) allow for size reduction
  - Consumer space is extremely cost sensitive
  - Conversion of CSP to WLP when possible
- Internet of Everything drives future growth moving forward
  - Everything connected
  - Bandwidth requirements projected need to grow by 1000X
- Must keep perceived constraints from stifling innovation
  - Balance the needs of all stakeholders

Thank You