ARM Dual Core Product Demonstration with 2.5D Through-Silicon-Via

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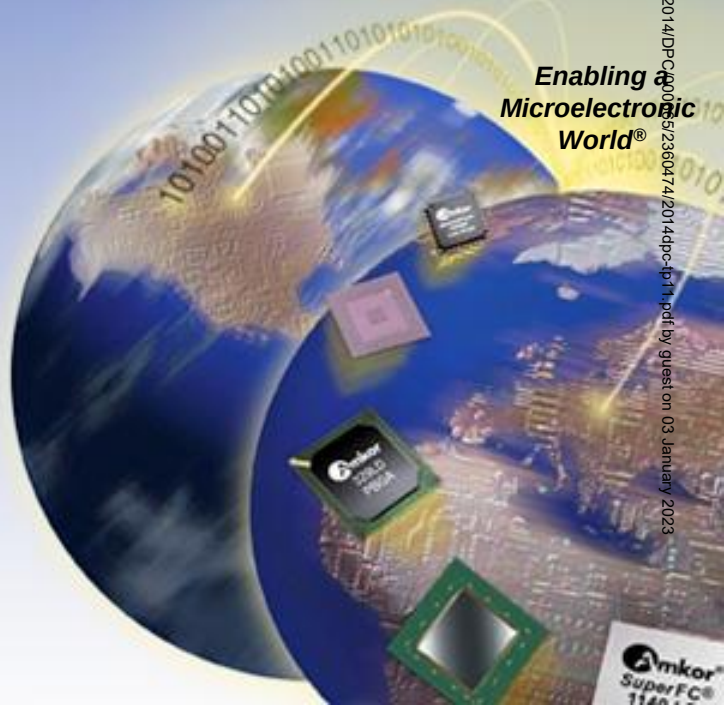

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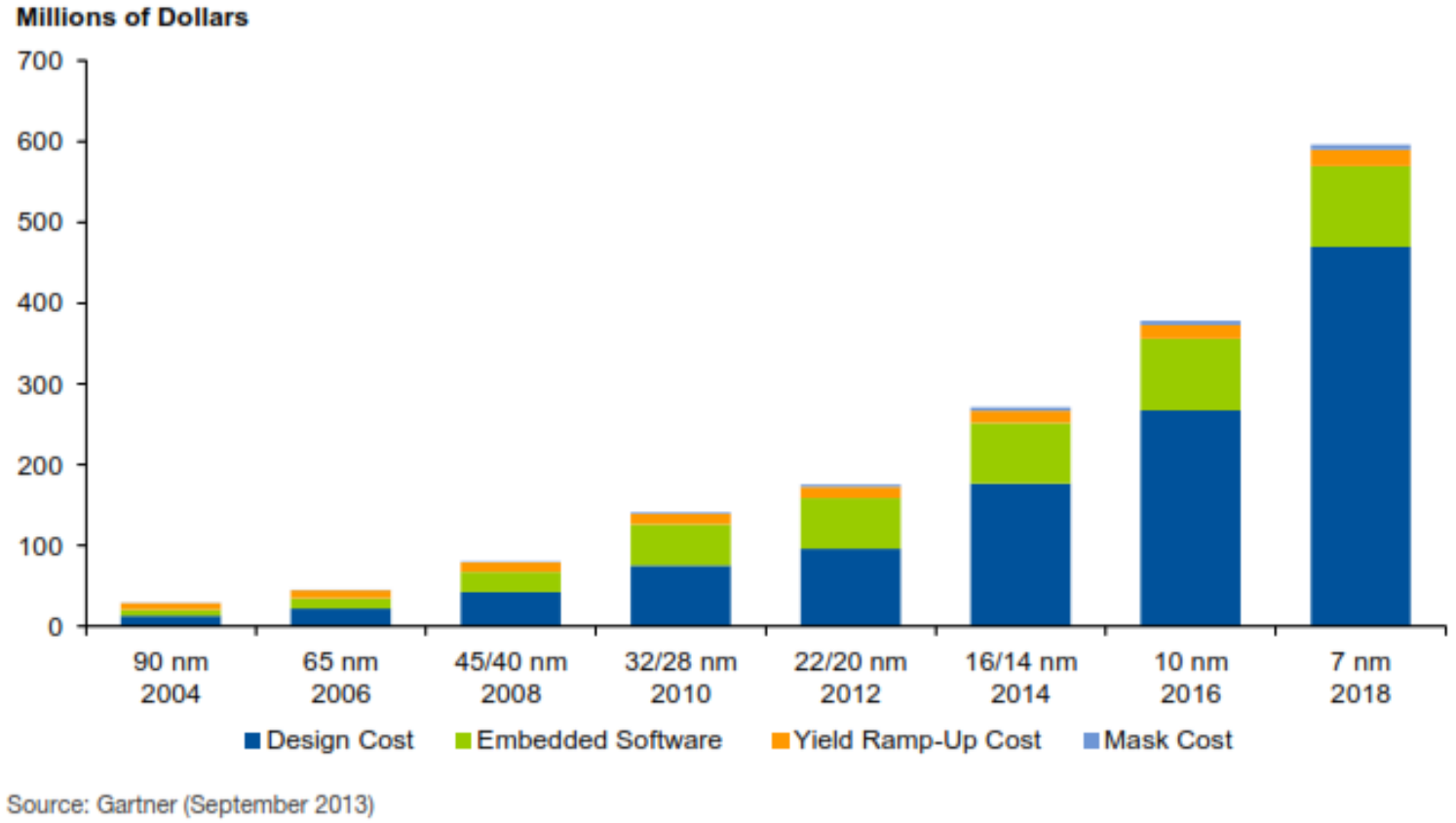
Overview

- **Industry Drivers for 2.5D TSV (Thru-Silicon Vias)**
- **Design & Functional Results from Demonstration Vehicle**
- **Assembly Results Update**

TSV Industry Drivers

Cost of Scaling is Rapidly Increasing

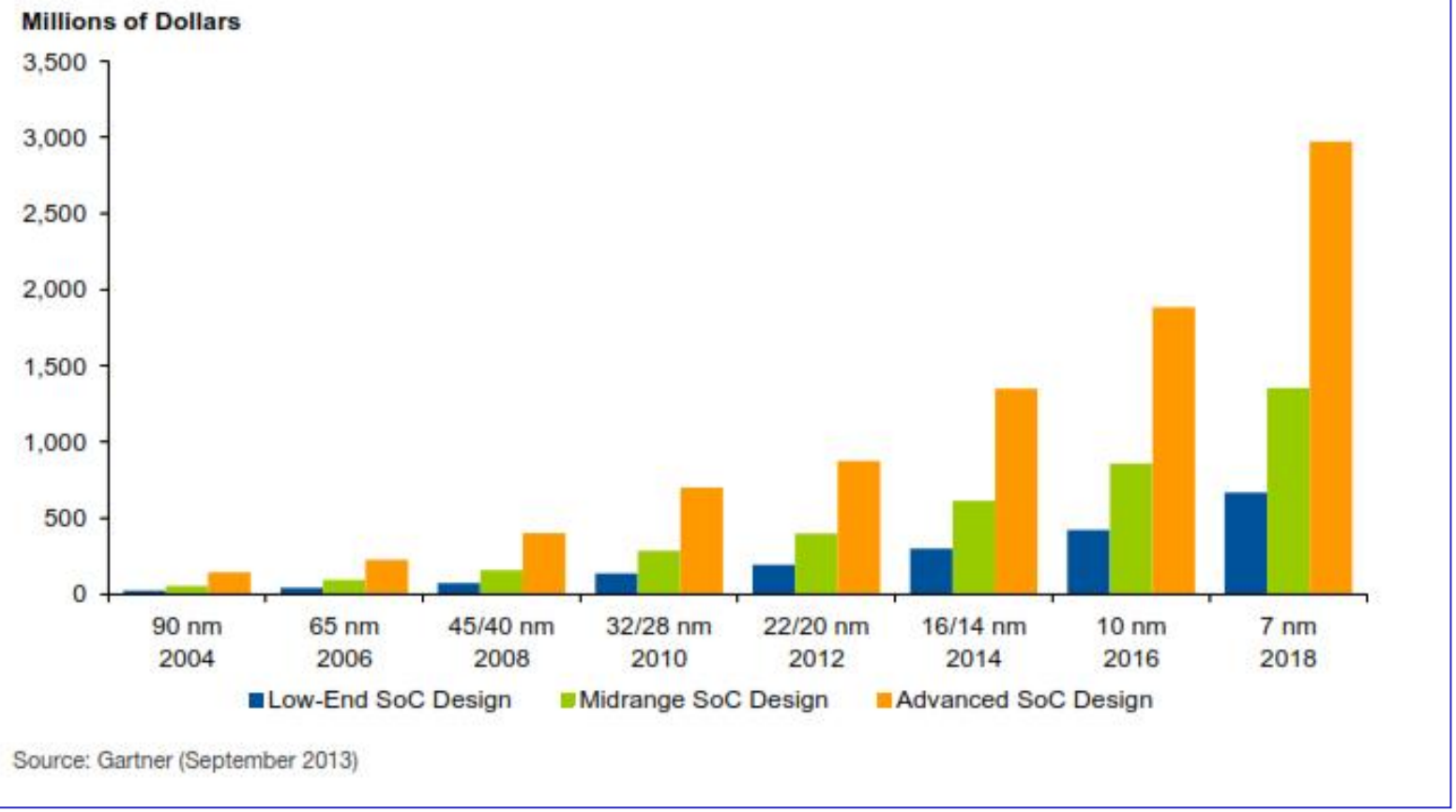
Estimated Development Costs for an Advanced SoC



- **Development cost for 10nm design will approach $400M**

Cost of Scaling is Too High

Minimum Lifetime Revenue Requirements for SoC Designs

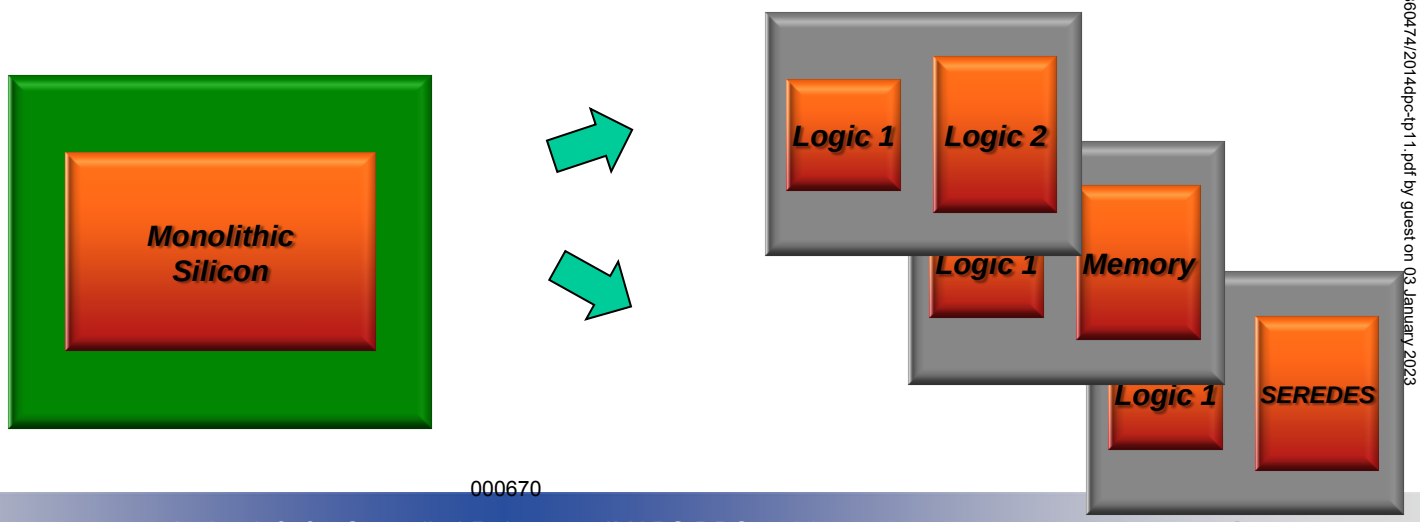


- **Requires multi-$B lifetime revenue to be economically feasible per design**
- **Must have other solutions**

Reduce the Impact of Scaling Costs

Partitioning the Monolithic SoC

- Separating functions reduces # of layers per device
- Higher yield enabled by smaller die size
- Enables use and re-use of lower cost nodes
- Lower CAPEX investment for Foundry
- Cost savings offset interposer cost
- Requires different I/O design, EDA software



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Power: Costly to Manage, and Limits Performance

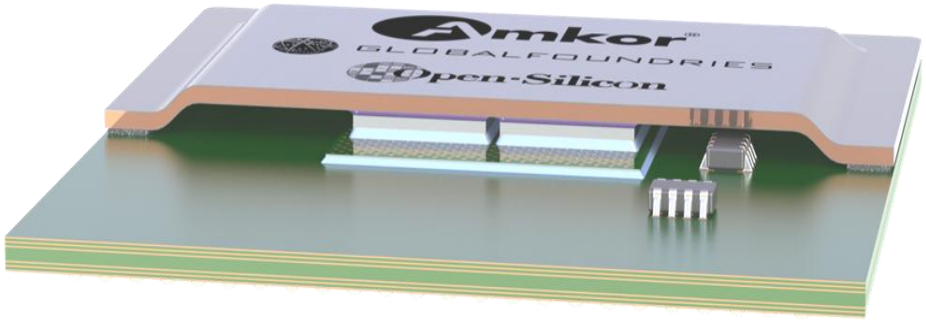
- Mobile: Maximum skin temperature in smart phones requires shutdown of cores
- Computing: Power required to drive off substrate memory reduces graphics or processor performance
- Networking: > 50% of data center cost is cooling
- Memory: T_j > 80C increases the required DRAM refresh rate, increasing power and heat
- High performance Memory: SerDes vs. Massively Parallel memory buses
  - SerDes: Reduces I/O density but higher power
  - Massively parallel I/O is lower power, but requires very dense routing capability (e.g. interposer)

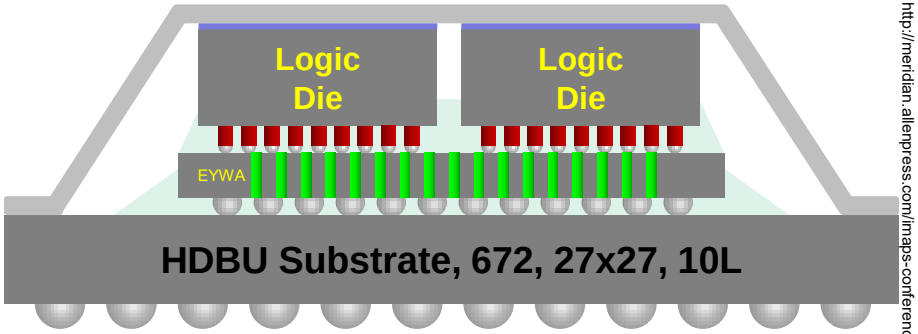
TV Design and Functional Results

Test Vehicle and Demonstration Objectives

- **Prove out custom low power die-to-die IO functionality**
  - Full development board
  - Memory, boot-ROM, and basic peripherals
  - Software execution on embedded dual-core ARM Cortex-A9 CPUs
- **Demonstrate EDA reference flow to address additional requirements of 2.5D Design**
  - Interposer complexity
  - Power planning with an interposer
- **Demonstrate Collaborative Supply Chain Approach**
  - Design
  - Foundry: Interposer Sourcing and design rules
  - Packaging
    - Assembly design rules
    - Package reliability (ongoing)
  - Provide a fully successful integration path

Demonstration Vehicle Structure





Package					
Body size	27.0 mm * 27.0 mm	**Ball Count**	672 ea	**Max Height**	2.78 mm
Top die					
Die size	4.5 mm * 4.5 mm	**Thickness**	0.600 mm	**Bump Height (Cu Pillar)**	0.04 mm
Bump pitch	40 um pitch				
Interposer					
Die size	10.6 mm x 7.1mm	**Thickness**	~100 um	**FS Bump Pitch**	0.040 mm
FS Bump Height	Ni /Au	**BS Bump Height, C4**	80 um	**BS Bump Pitch**	0.170 mm

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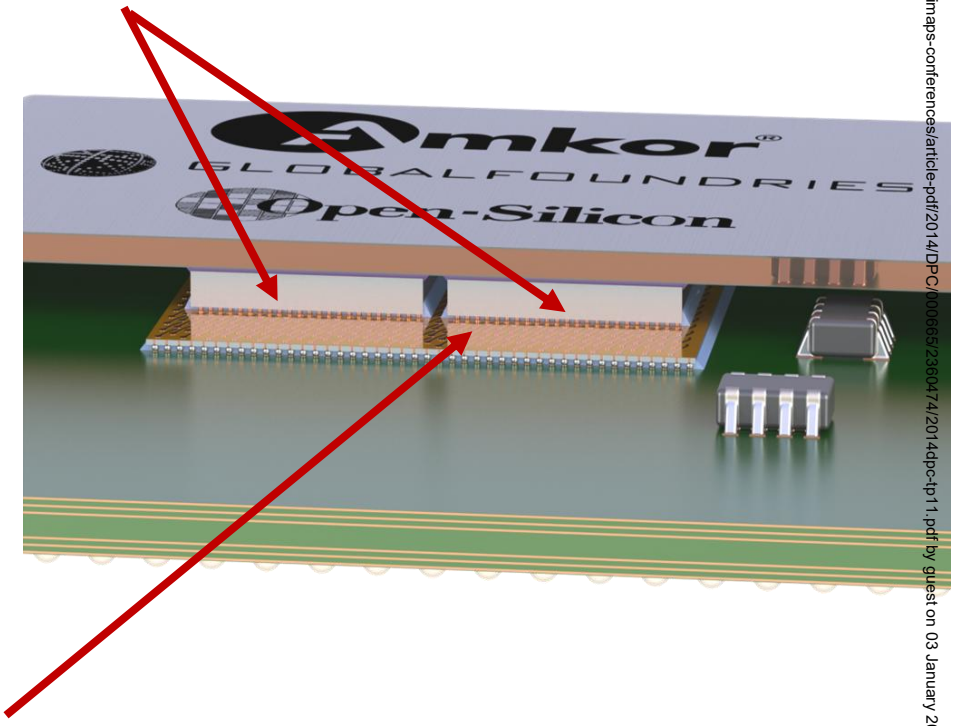
Development Vehicle Functional Description

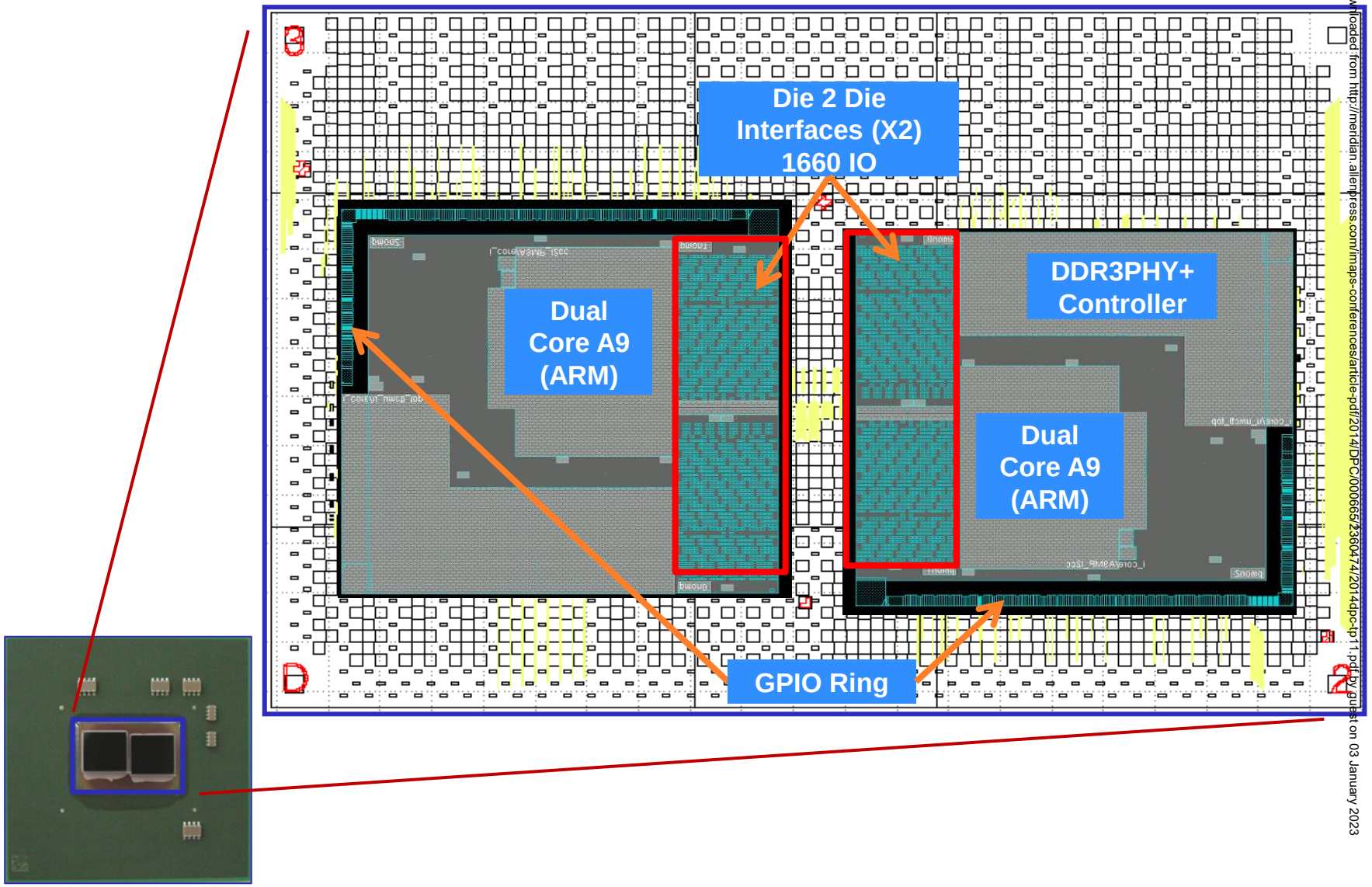
- **Two Logic die contain dual-core ARM Cortex-A9 CPU**
  - GLOBALFOUNDARIES 28nm SLP
  - Peripherals Support: DDR3, NOR Flash, UART, SPI, I2C, I2S
  - AXI bridge interfaces
  - (Open Silicon was awarded ARM TechCon 2013 “Best in Show” IC design)

- **Custom die-to-die IO Drivers**
  - Lower power
  - 16 GB/s full-duplex data-rate across the two die through the silicon interposer
    - 64 bit datapath @0.5GHz
    - 2 ports, bidirectional
  - Demonstrated ESD performance

- **Custom Interposer**
  - GLOBALFOUNDARIES 65nm Cu

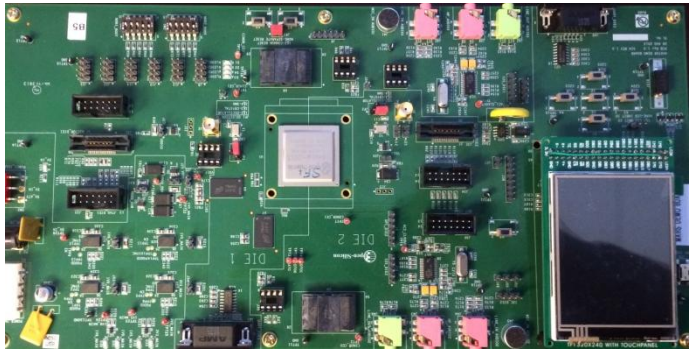


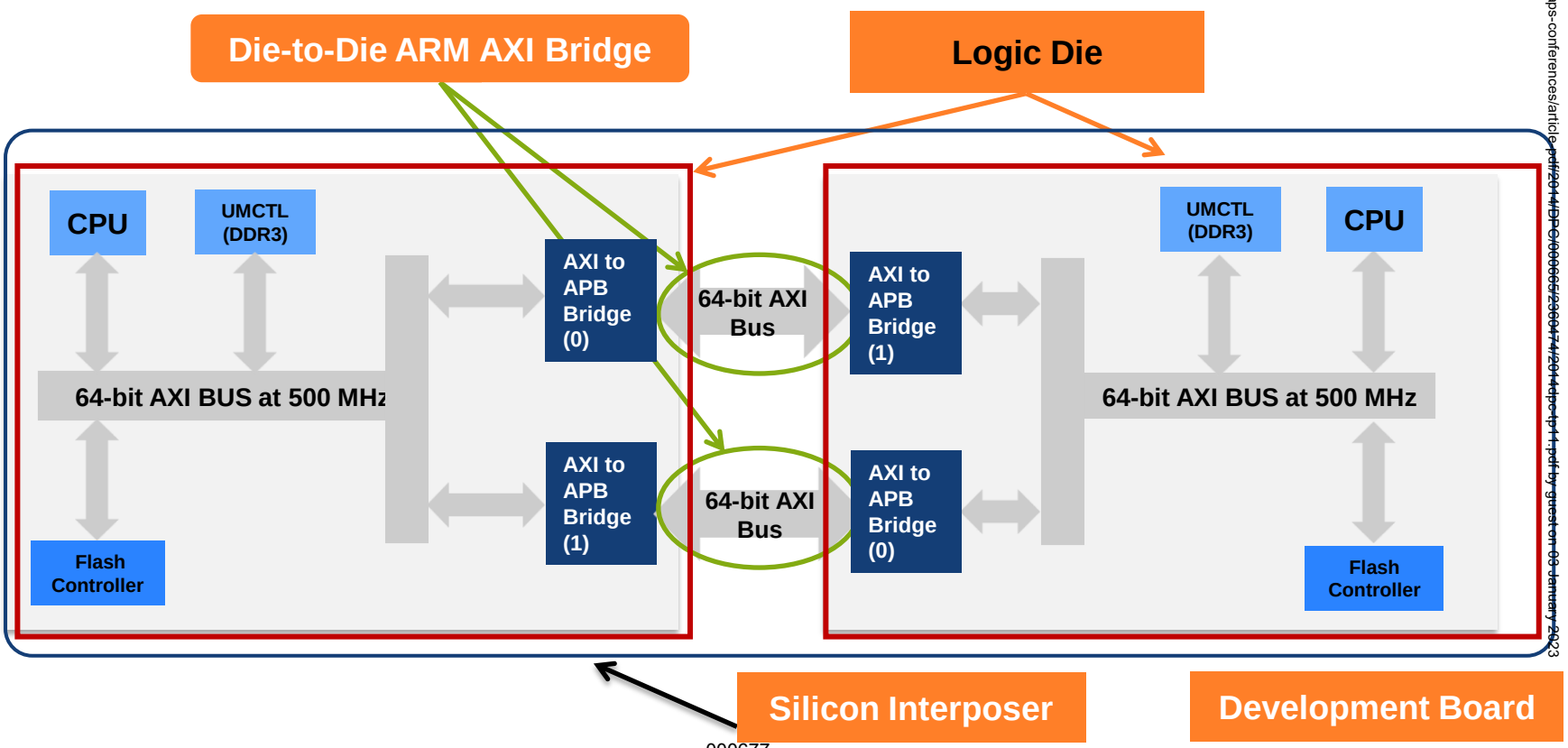
Interposer and Test Chips



Validation and Demonstration

- Development Board
- Two ARM CPU die
- 64 bit AXI bus between die
- Die to Die interface functionality tested through software running on the two CPUs





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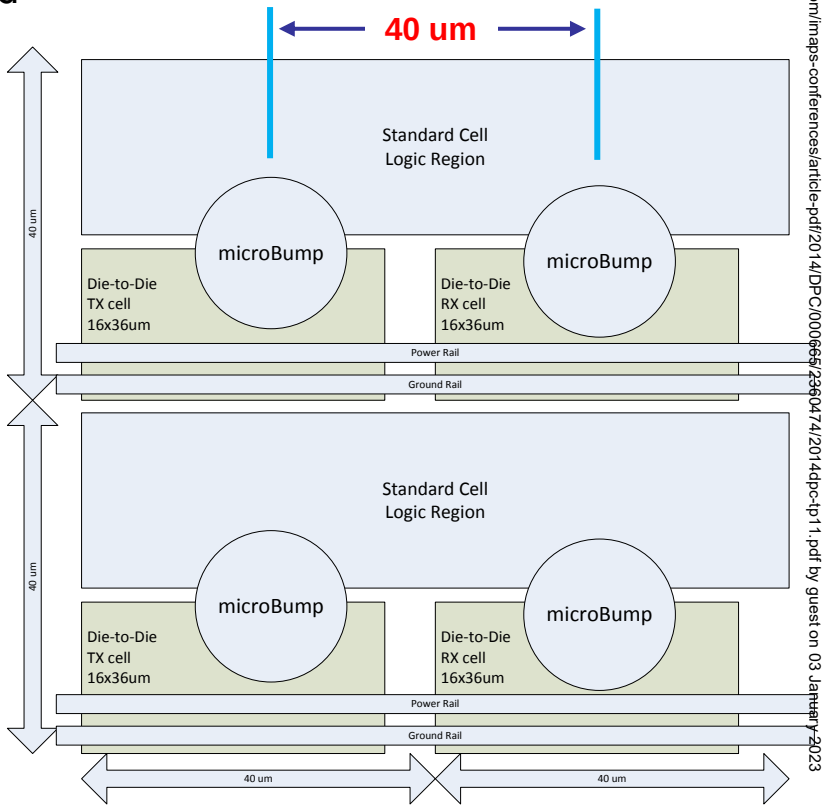
Die to Die IO

- **Custom Die-to-Die IO Bridge**
  - 40 um bump pitch micro copper pillar
  - 78% area reduction compared to equivalent GPIO IO size
  - Saved 50% of D2D bridge area
    - Smaller u-bump pitch could have been used
    - Die to die bridge area
  - 16 GB/s full-duplex data-rate across the two die through the silicon interposer

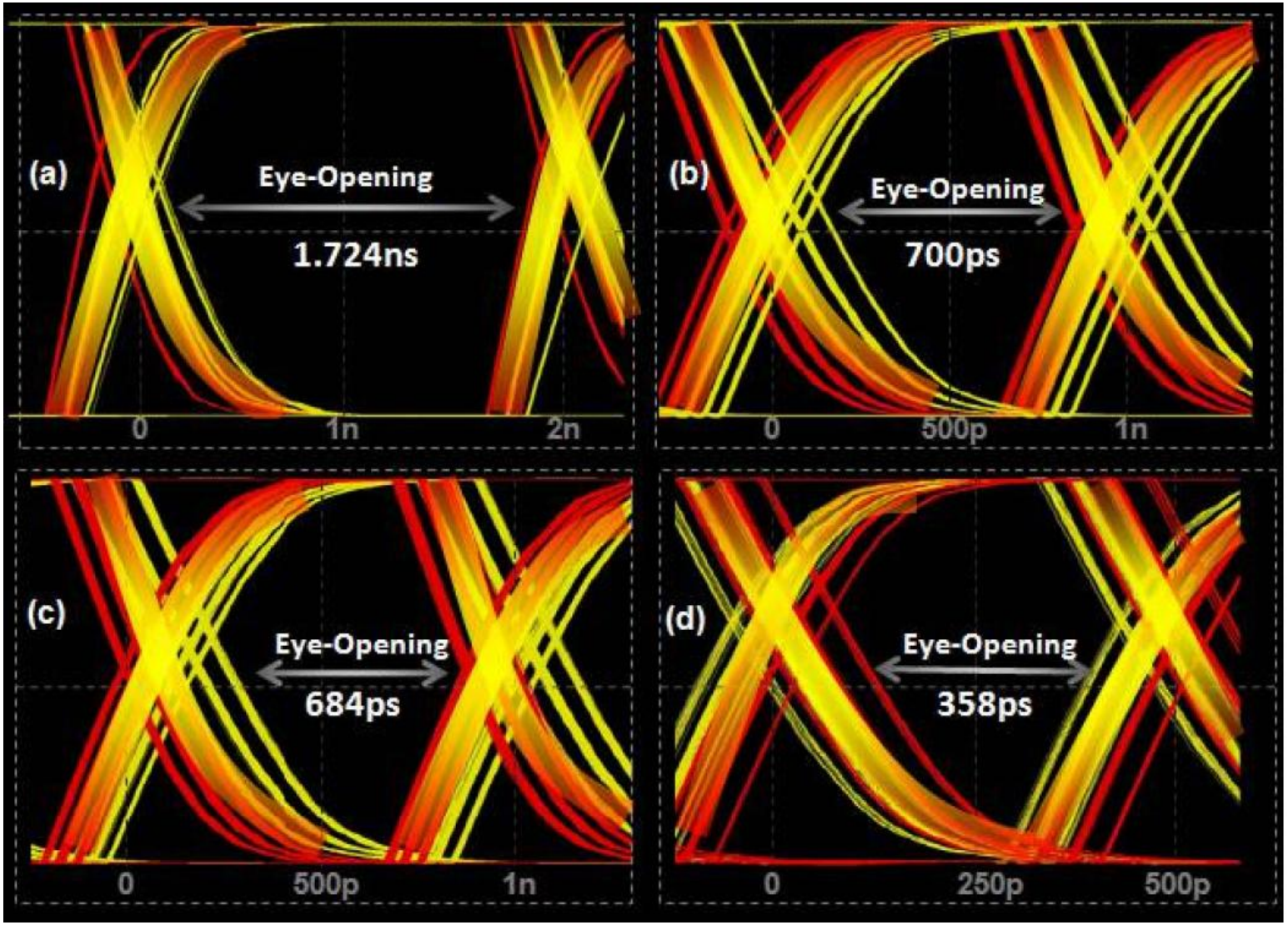
- Lower Power
  - ~0.5pJ/bit (average)
  - Off-die connections (>7.5pJ/bit)

- Achieved 100V CDM ESD protection
  - 4 ESD experiments were designed



Eye Diagrams (Simulated)

(a) 500 MHz, (b&c) 1 GHz (d) 2 GHz



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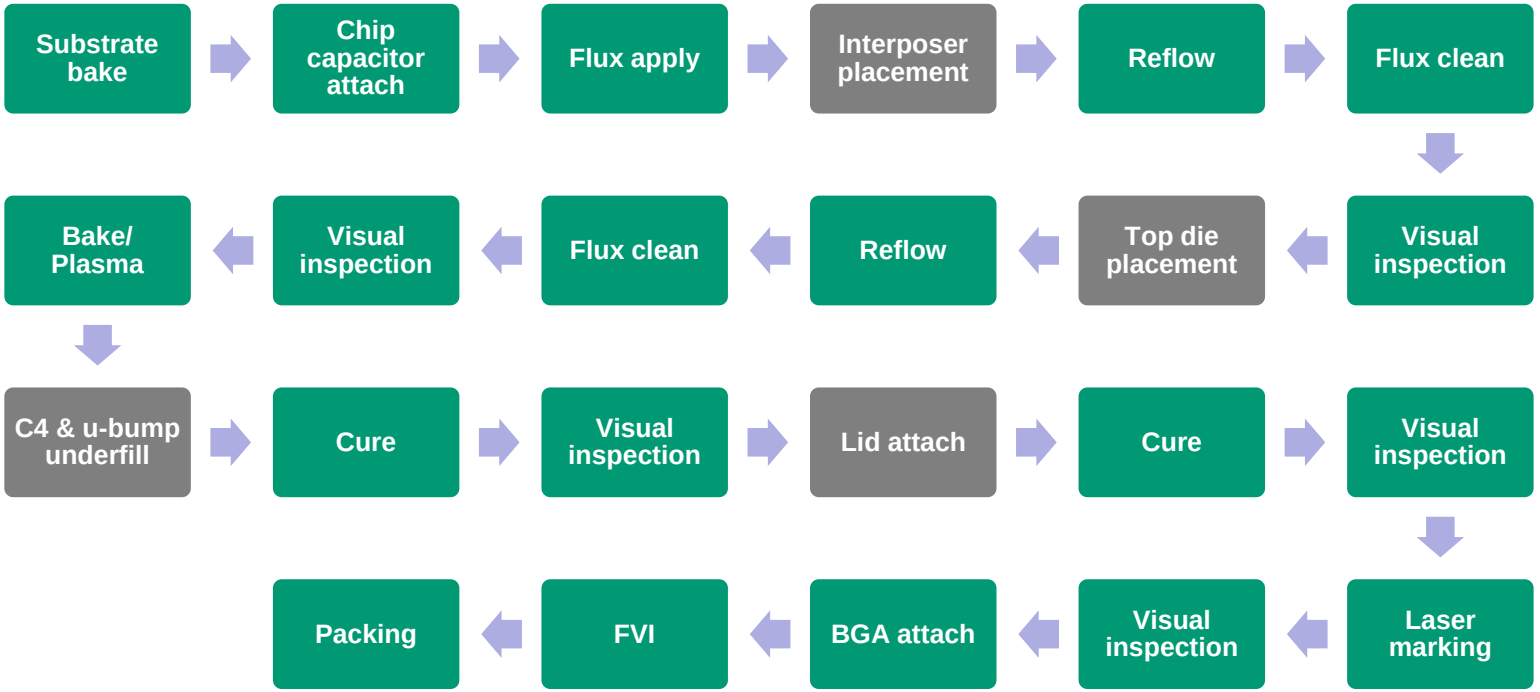
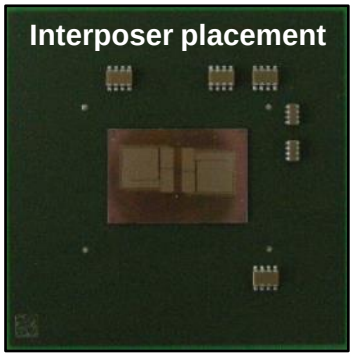
Summary Results from Electrical Testing

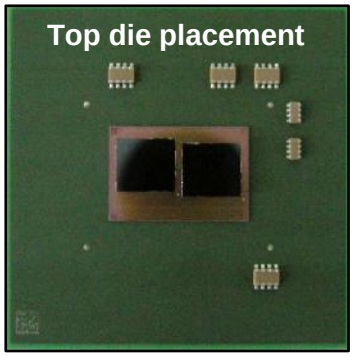
- **Functional die-to-die bridge was successfully demonstrated and characterized**
- **500 MHz performance good match with simulations**
- **2 GHz functionality expected**
  - Simulations show 2GHz is OK
- **Power planning**
  - Used Interposer to make robust power grid

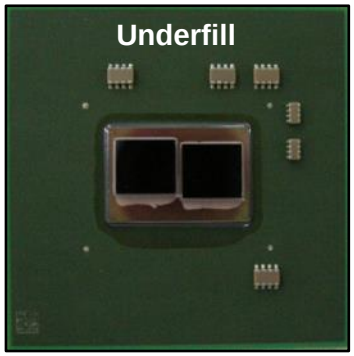
Assembly

ARM Demo TV Assembly Flow









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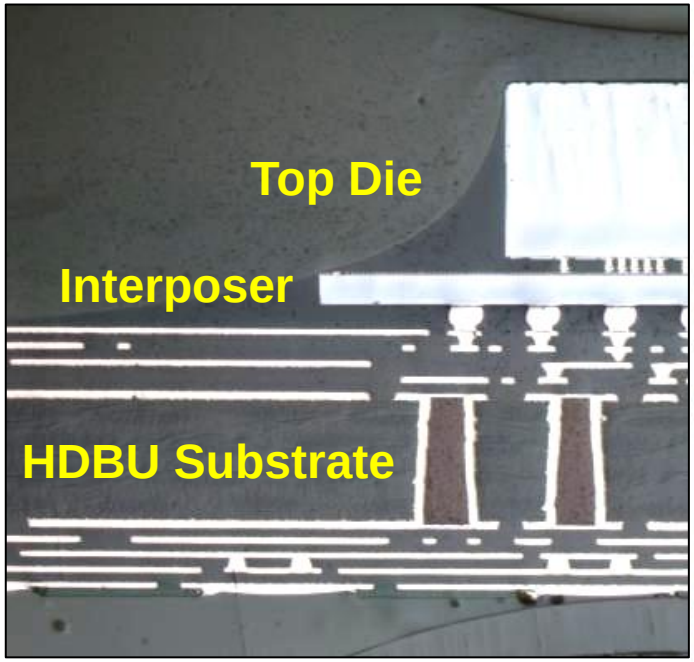
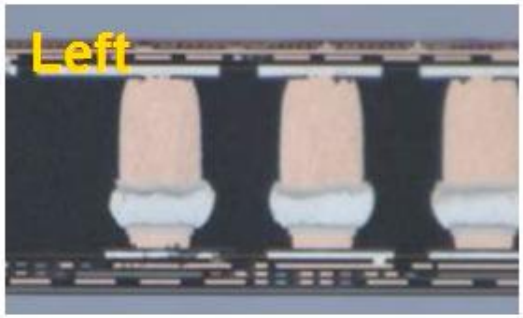
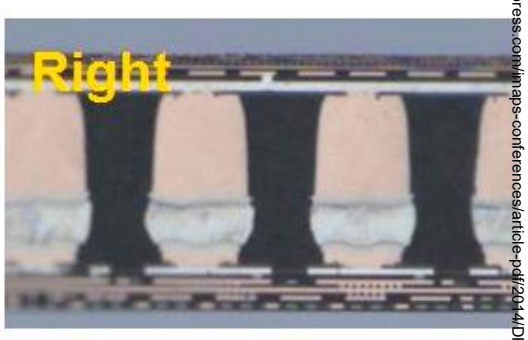
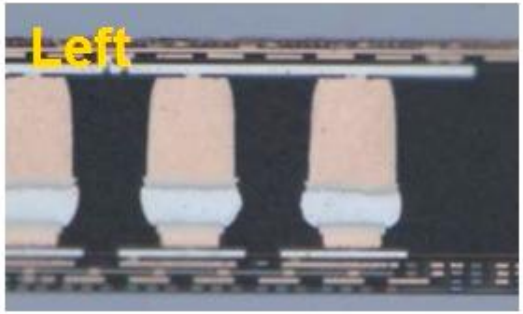
Assembly Typical Results

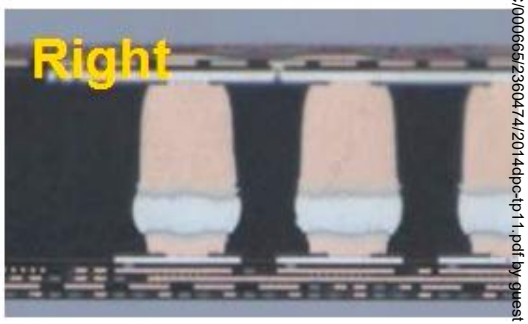
- POR Flux and UF materials
- Consistent C4 and Copper Pillar standoffs





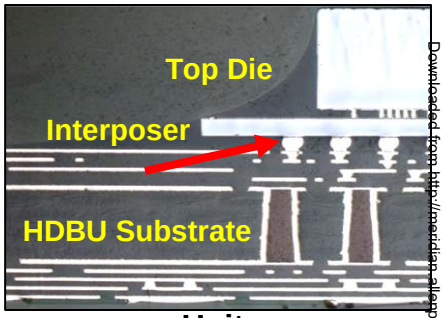






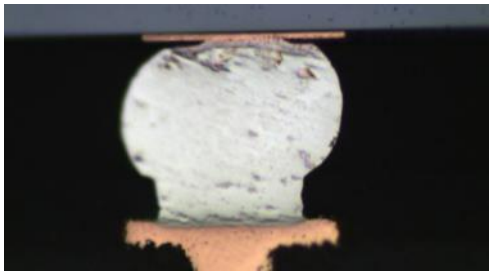
ARM Demo Interposer Attach To Substrate

- **C4 joint of Interposer processed with Tensil SiN film on the backside**



Unit: um

Position	Left	Center	Right	Min	Max	Range	Average
Top	66.4	75.0	65.2	65.2	75.5	**10.3**	70.7
Bottom	75.5	75.5	66.5				



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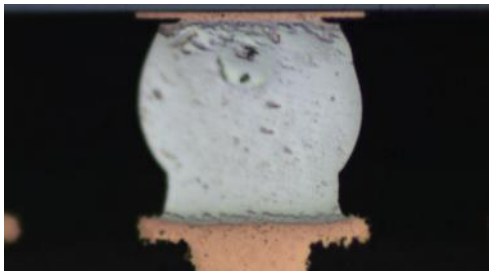

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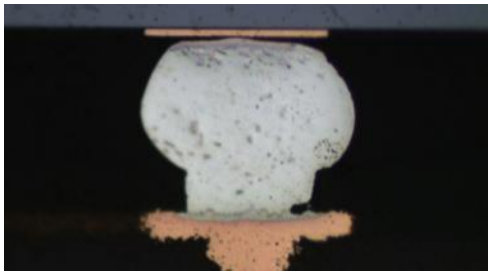

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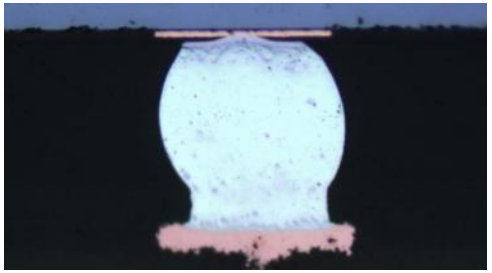

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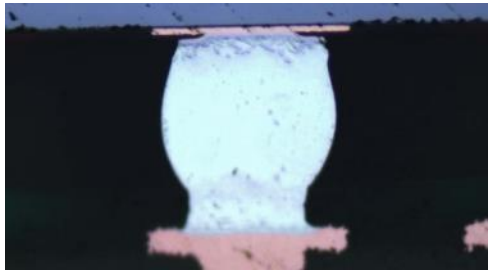

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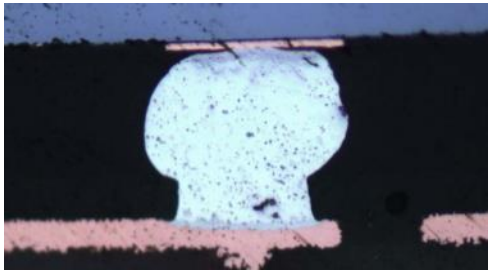

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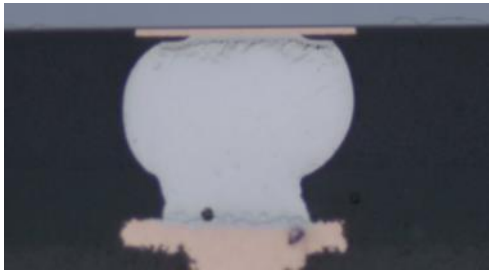
ARM Demo Interposer Attach To Substrate

- Interposer processed with Compressive SiN film on the backside
- Extensive library of BS film stress recipes

Unit: um

Position	Left	Center	Right	Min	Max	Range	Average
Top	63.4	66.0	64.5	63.4	66.0	2.6	64.5
Bottom	63.6	65.7	63.9				



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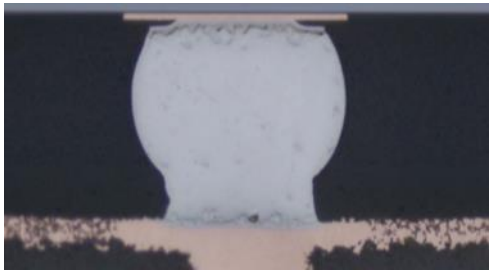

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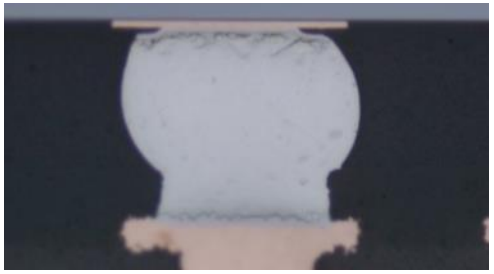

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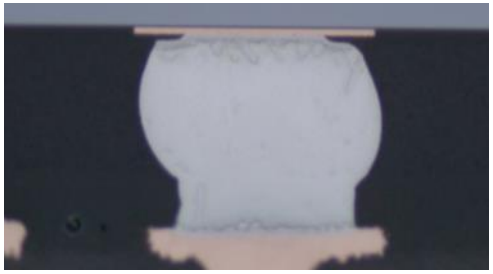

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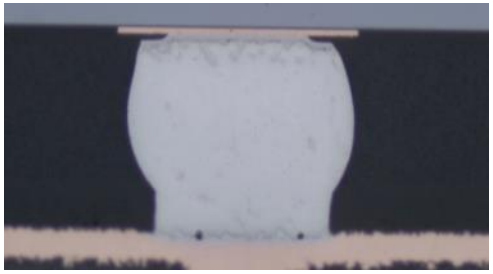

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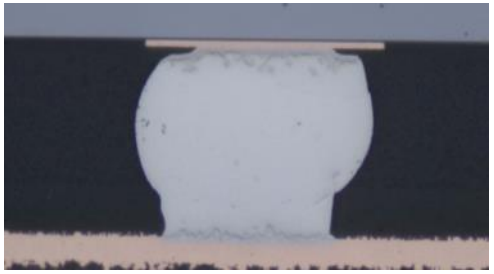

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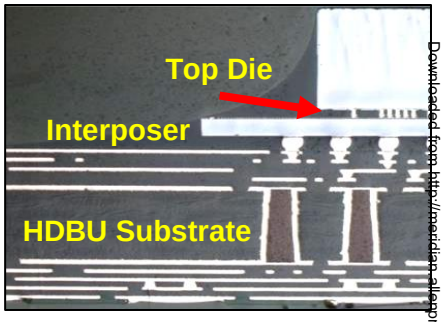
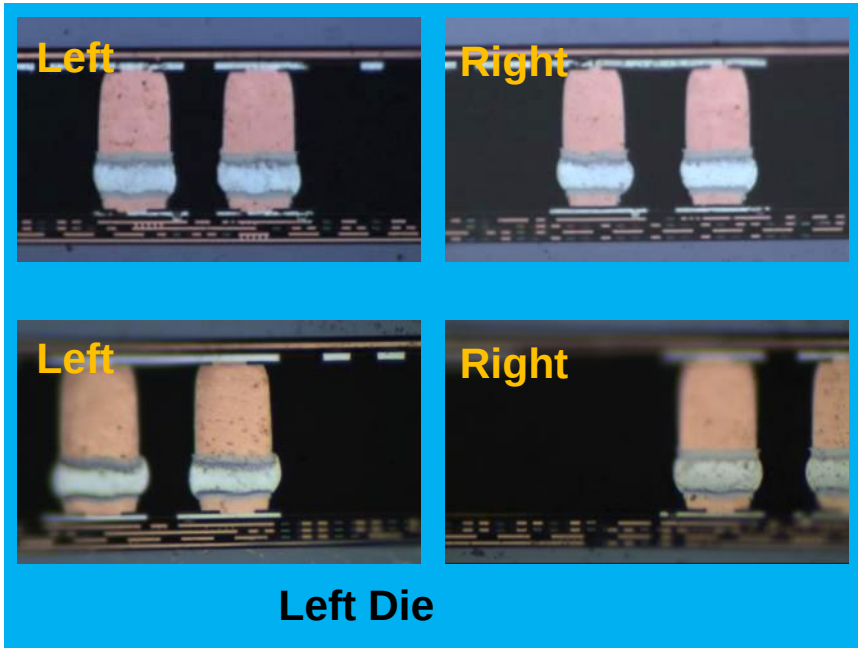
ARM Demo Die Attach to Interposer

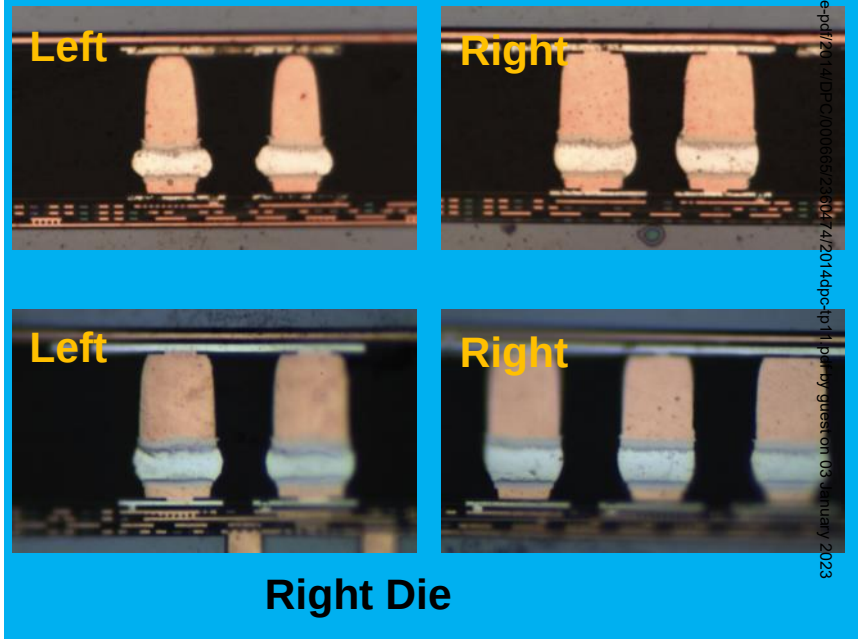
- **Top die Cu pillar u-bump joint with Tensile SiN Film**



Position	A1-Left	A1-Right	A2-Left	A2-Right	Min	Max	Range	Average
Top	45.0	43.7	44.4	43.9	43.7	45.5	1.8	44.5
Bottom	44.2	45.5	44.7	44.8				

Unit: um





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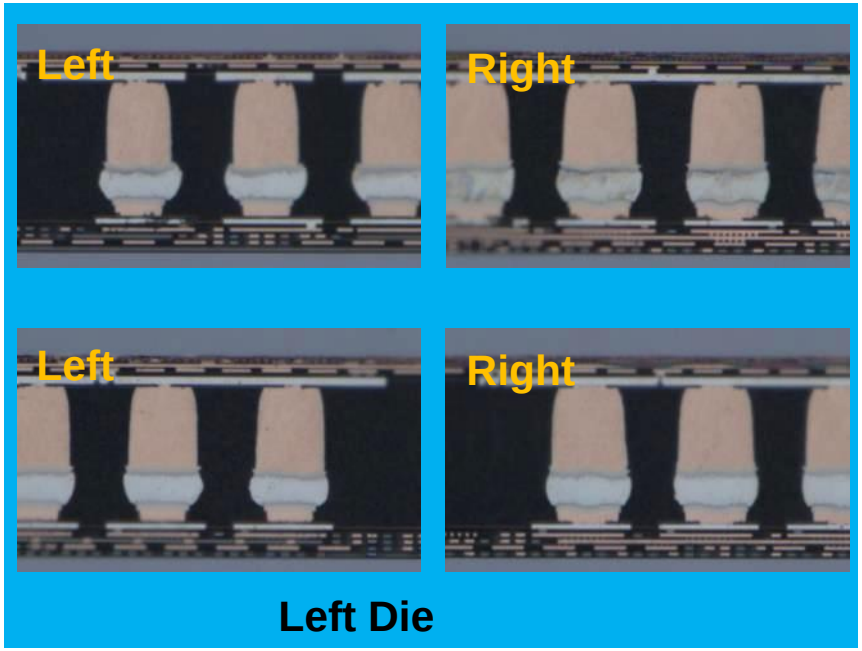
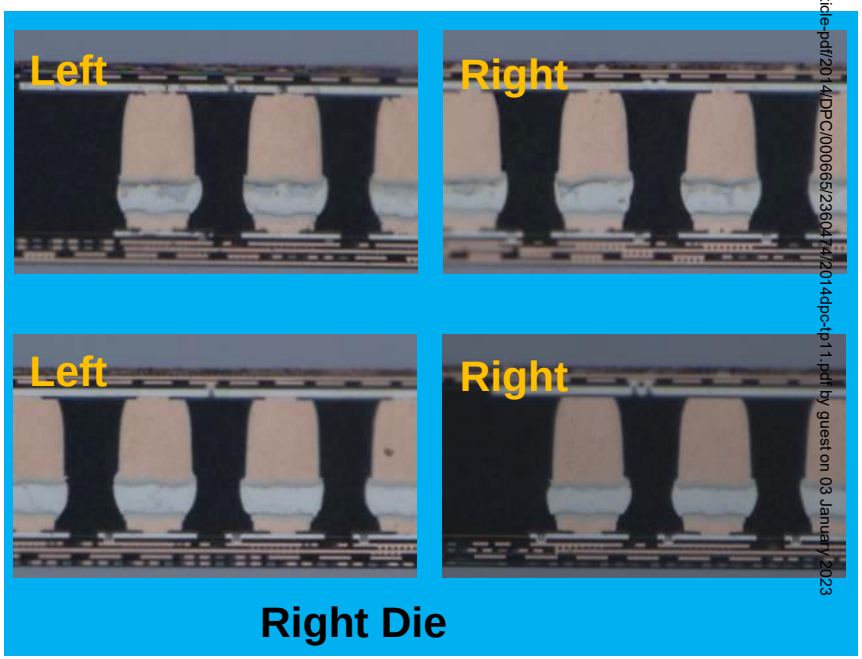
ARM Demo Die Attach to Interposer

- **Top die Cu pillar u-bump joint with Compressive SiN Film**

Position	A1-Left	A1-Right	A2-Left	A2-Right	Min	Max	Range	Average
Top	41.6	41.9	42.4	43.2	41.1	43.2	2.1	42.1
Bottom	42.0	42.2	41.1	42.2				

Unit: um





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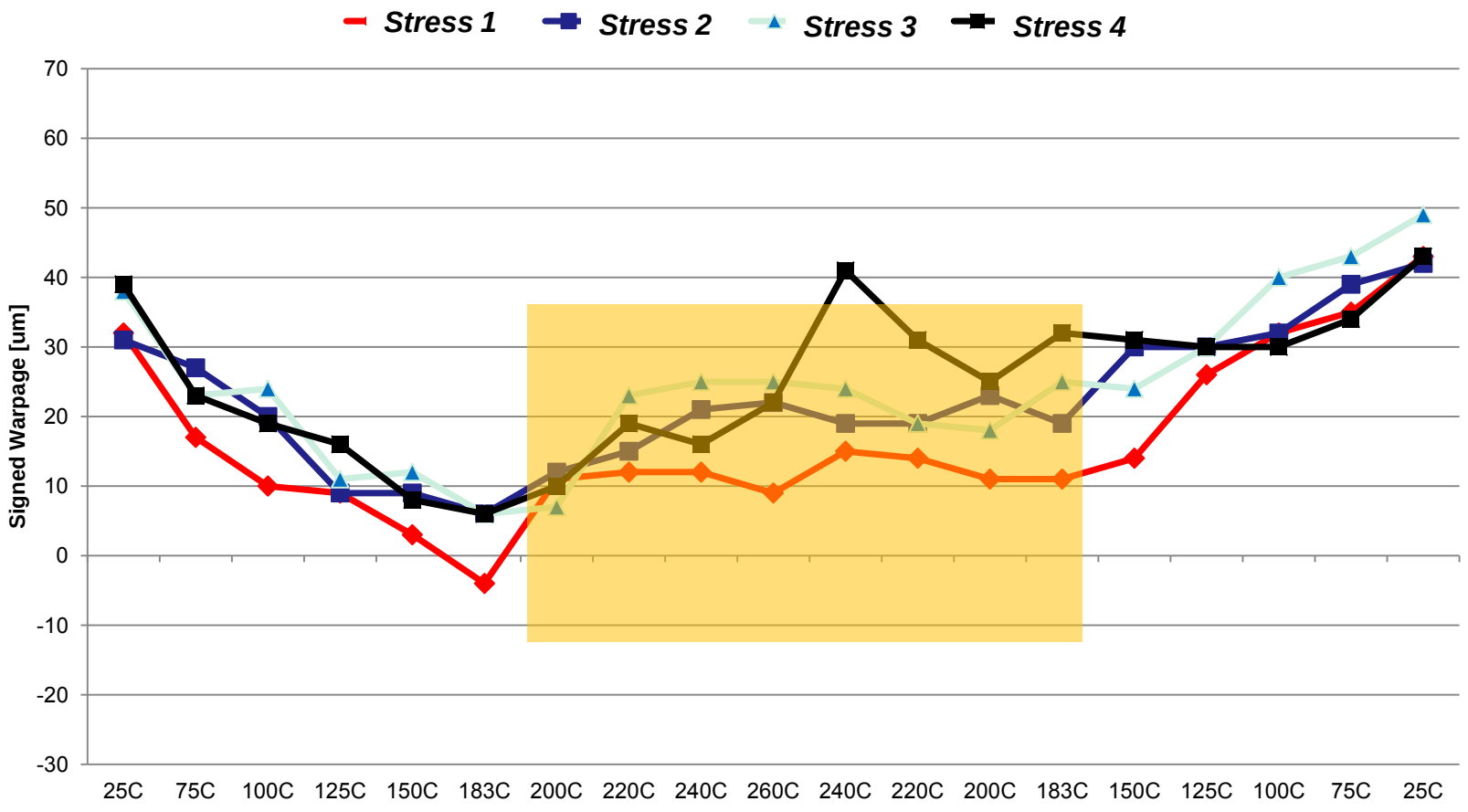
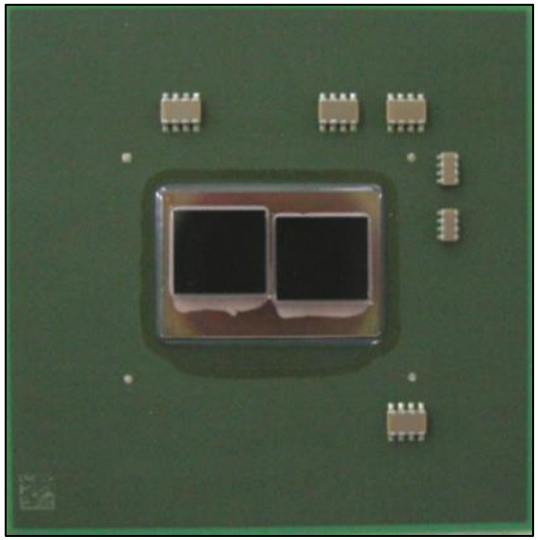
Warpage: Interposer attached to Substrate

- **Warpage tuning for optimum top die attachment**

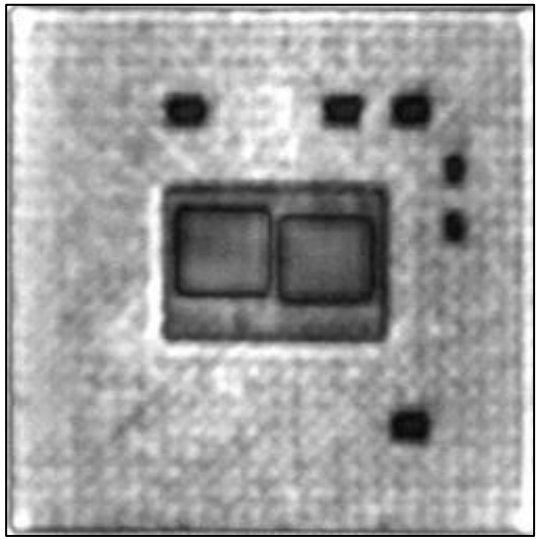


Underfill

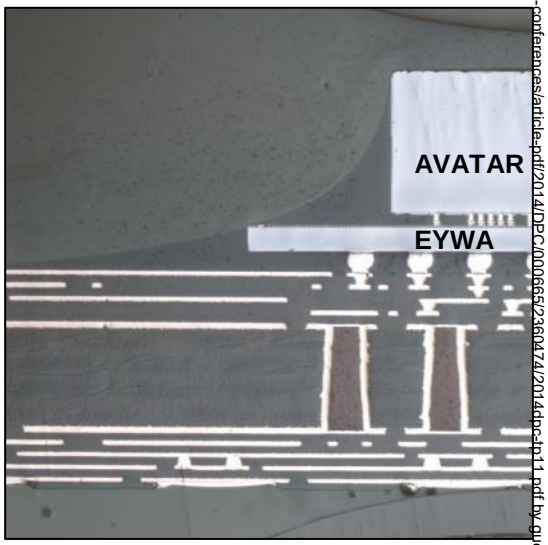
- SAM (Scanning Acoustic Microscopy) confirmed no underfill void
- Cross-section confirmation
- Extensive UF material development for u-bump pitches



Visual image

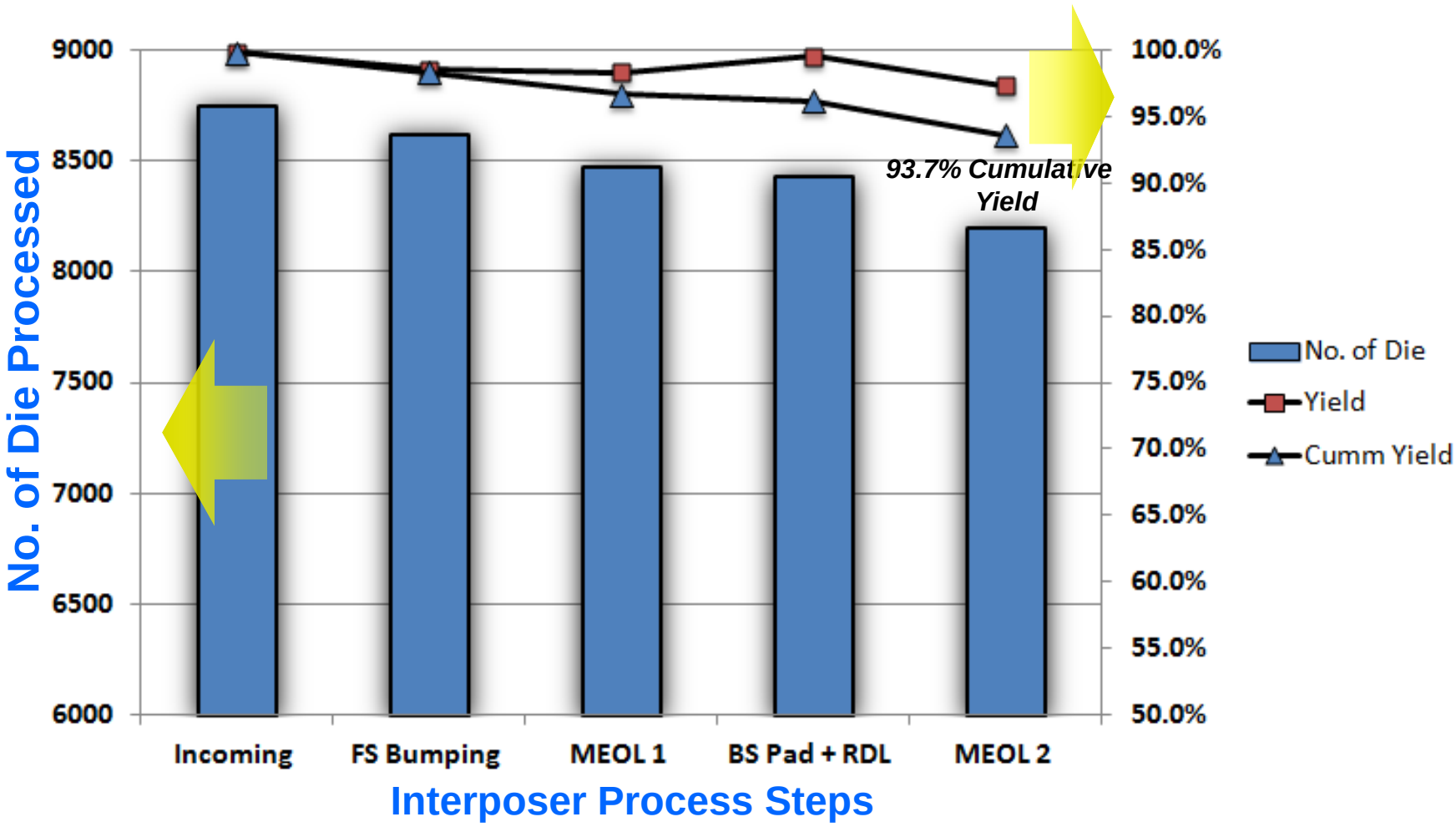


SAT image



X-section image

ARM Demo TV Interposer Yield Summary



Summary

- **Collaborative model works : Design, Foundry and OSAT.**
- **Die to die IO signaling performance met or exceeded expectations**
  - IO power reduced to 0.5pJ/bit
  - IO die area reduced to 22% of typical off chip IO (GPIO)
- **Interposer warpage tuning fully demonstrated**
- **High assembly yields**

Acknowledgements

Amkor Korea (ATK)

- **WonChul Do: R&D Director, 2.5D Packaging**
- **EunHo Park: R&D Manager, 2.5D Packaging**
- **YoungRae Kim: R&D Manager, 2.5D Packaging**
- **DongHoon Han: R&D Sr. Manager, Bumping**
- **YongJae Ko, R&D Manager, Bumping**

Thank You

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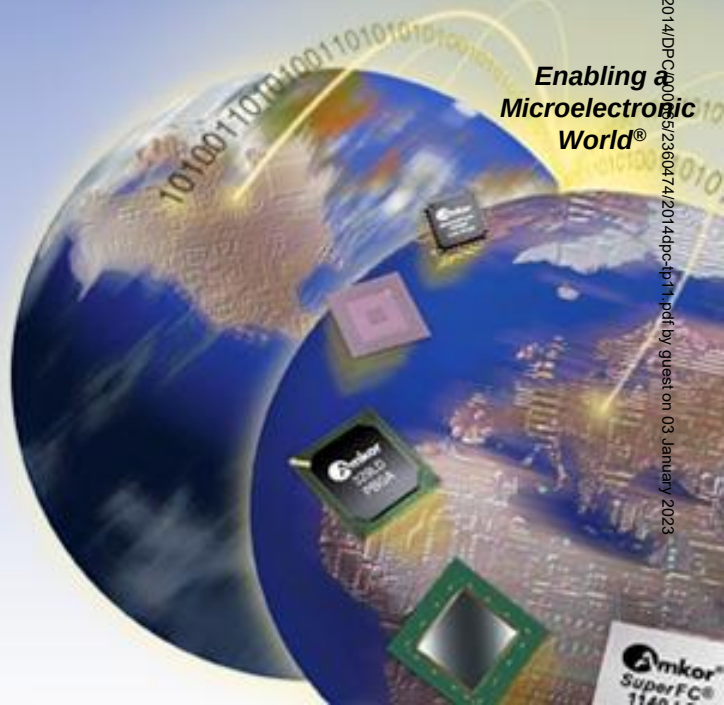

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