IMAPS 9th International Conference and Exhibition on Device Packaging

RELIABILITY & TRUST

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Effect of Layer Variation on Package Warpage

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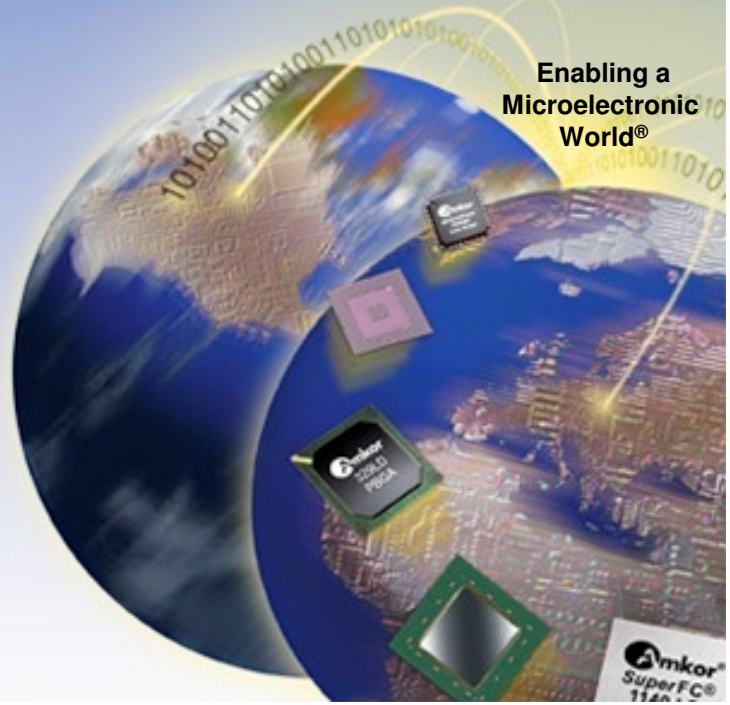


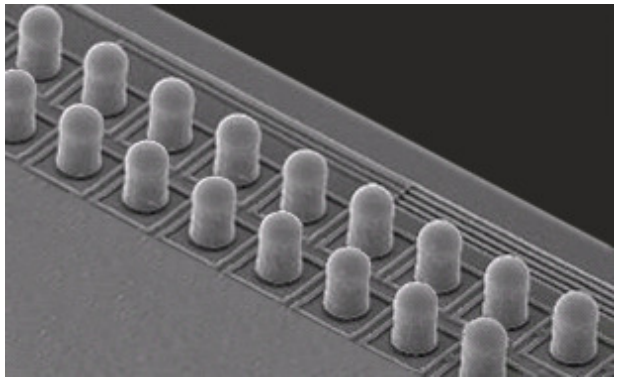
Amkor Technology®

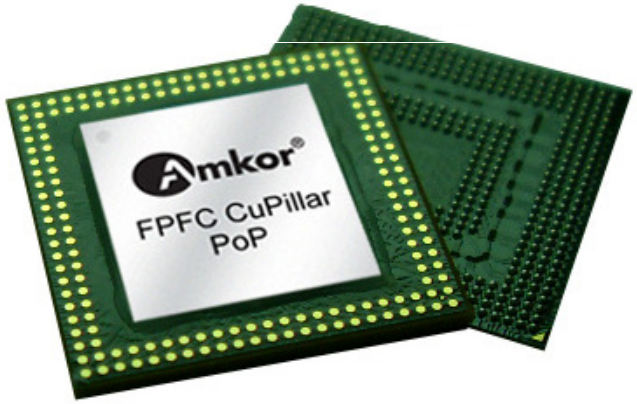
Contents

- Cu Pillar/PoP background
- Impetus for study
- Simulation method & results
- Trial build & results
- Discussion
- Conclusions & Next steps

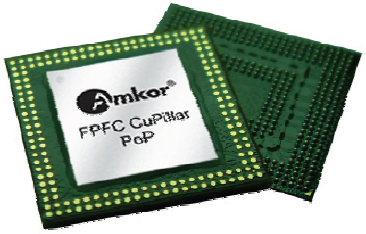
Fine Pitch Cu Pillar introduction

- **Amkor has qualified and shipped an industry-changing technology**
- **Current industry benchmark is traditional solder flip chip, which has significant technical limitations to pitch reduction**
- **This technology provides a true fine pitch, low cost and environmentally friendly solution**
  - Enables bump pitches of 50um and less, is cost competitive to wire bond and is lead free
- **New packaging platform enables reduced semiconductor chip size and cost while boosting performance**
- **Ideal for handheld, high performance, low power applications**

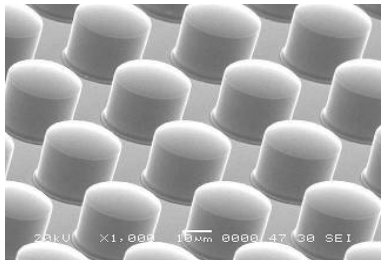


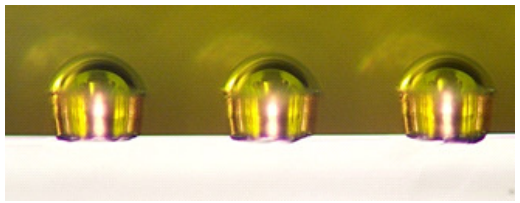


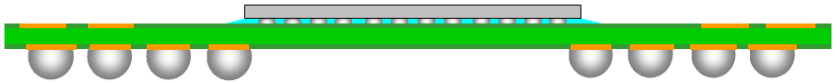
Fine Pitch Cu Pillar introduction



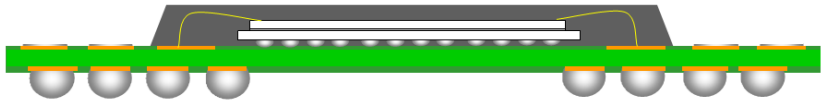
- **Amkor fine pitch Cu pillar technology**
- **Advantages**
  - Potential cost reduction with layer count reduction on substrate
  - Better electrical performance since no need for fan-in at die level metallization
  - Larger die in a given body size
- **HVM since Q2 2010**
- **Main Application : Mobile processor devices**







Bare die FPFC- CSP or PoP

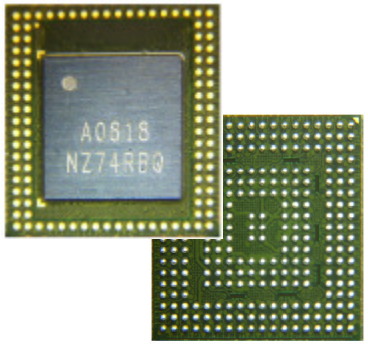


FPFC- FlipStack™ or TMV PoP

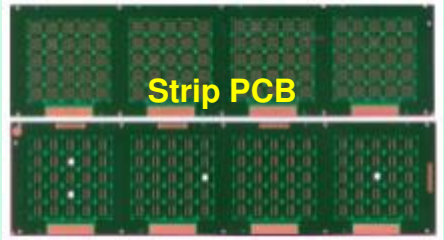
Amkor Package on Package (PoP) Introduction

- **Cu Pillar CSP families Diversity**

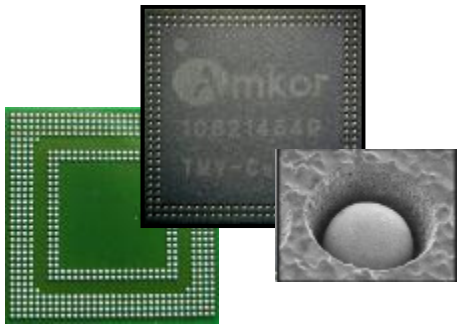
fcCSP



fcPoP



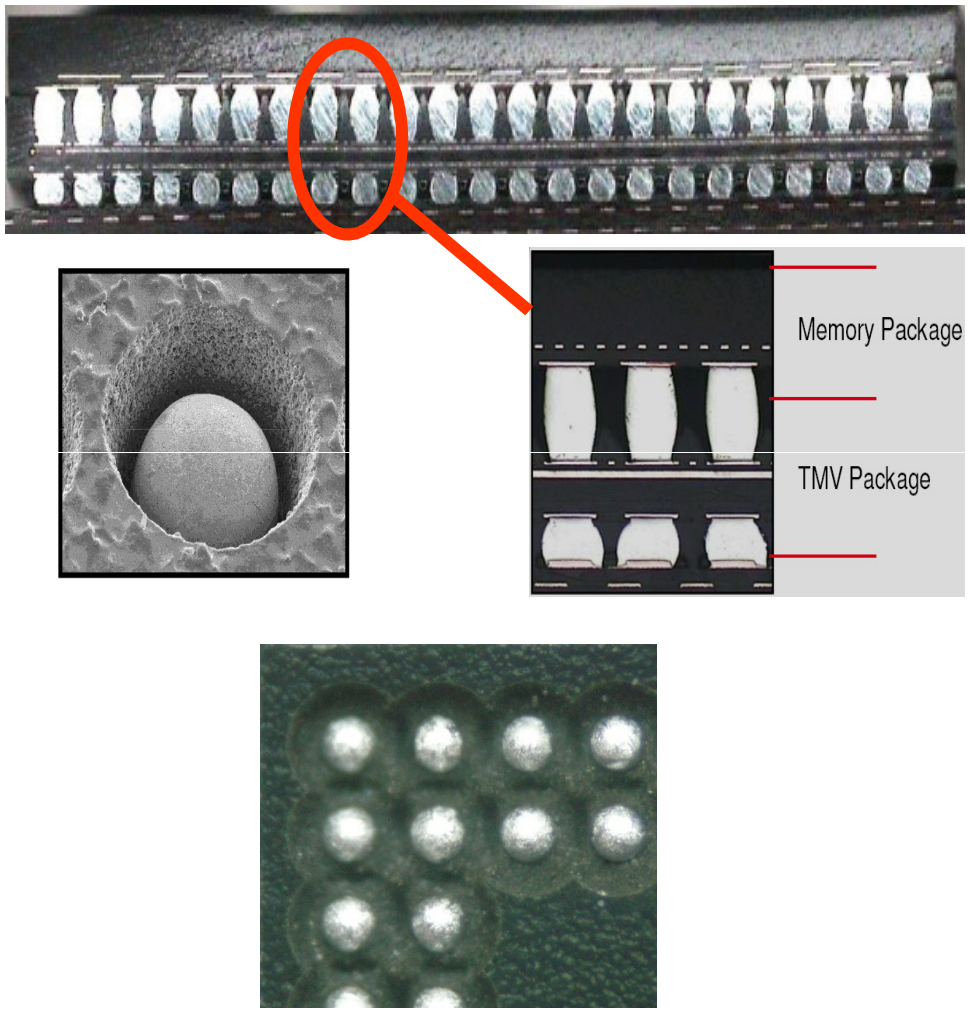
Bare die fcCSP



TMV®

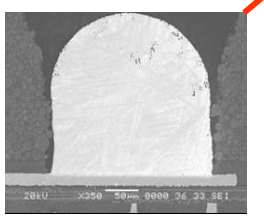
What is TMV® (Thru Mold Via) Technology?

- **Amkor's Through Mold Via (TMV®) technology is a processing step applied to several bottom PoP package types.**
- **TMV® is an ablation method to allow solderable connections thru a mold cap.**
- **TMV® is applied to wirebond, stacked die, flip chip devices (both area array solder and fine pitch Cu Pillar) and packages with discrete components embedded. TMV® could also be applied to FlipStack® (combo FC+WB) devices.**



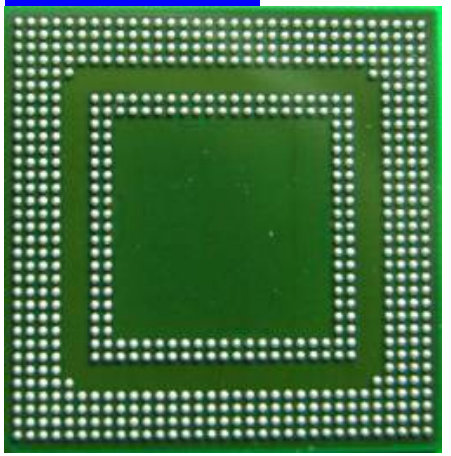
Amkor TMV® PoP Benefits

- **Enabling technology for next generation PoP requirements**
  - Improve warpage control and bottom package thickness
  - Improve SMT process window and BLR expected
  - Improve bottlenecks associated with memory interface
  - Increase die to package size ratio
  - Supports Wirebond, FC, stacked die and passive integration
  - Associated with JEDEC Standards (JC-11)



Top view

Bottom view



Impetus for study

- Mobile & other markets require thinner profile PoP package solutions
- Thinner packages require thin substrates
- Board level workability & reliability become an issue when warpage is too high
- Thin substrates in bottom package can have an impact on overall package warpage
- The goal: Reduce package warpage by all available means

Ways to reduce warpage

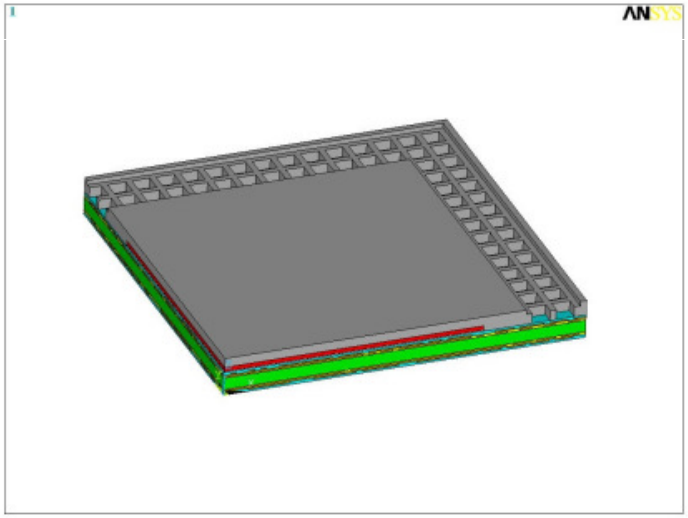
- **Substrate BOM choices**
  - Lower CTE materials in the substrate to reduce mismatch with Silicon
  - Core material is of particular focus due to its large contribution to overall substrate & package thickness
  - New core materials being continuously developed & deployed

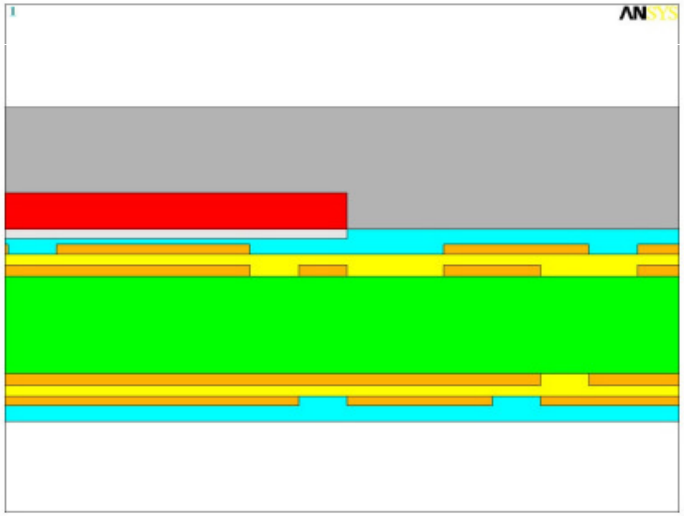
- **Package design**
  - Mold cap height
  - Mold cap material
  - Die thickness
  - Die size

- **Substrate layer thickness**
  - This study

Simulated package

- **Package construction**
  - 1-2-1package with Cu Pillar & TMV®
  - Pkg ~12x12mm, Die ~8x8mm
  - All package attributes chosen to coincide with package used in trial build

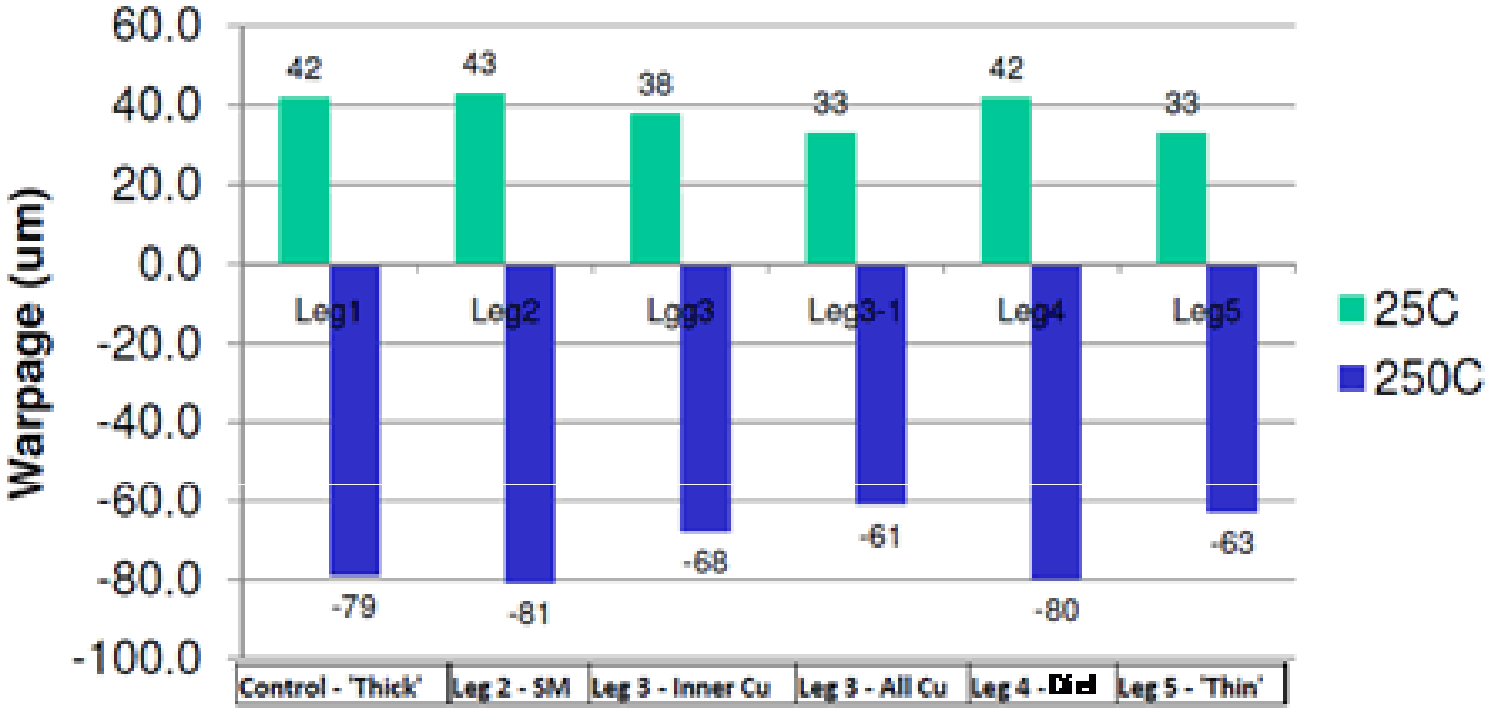




Simulation matrix

Units: µm	Control - 'Thick'	Leg 2 - SM	Leg 3		Leg 4 - Dieletric	Leg 5 - 'Thin'
			Inner Cu	All Cu		
Soldermask	33	17	33	33	33	17
L1 Cu layer	20	20	20	10	20	10
Dielectric	22	22	22	22	18	18
L2 Cu layer	24	24	10	10	24	10
Core	200	200	200	200	200	200
L3 Cu layer	24	24	10	10	24	10
Dieletric	22	22	22	22	18	18
L4 Cu layer	20	20	20	10	20	10
Soldermask	33	17	33	33	33	17
Total thk	398	366	370	350	390	310

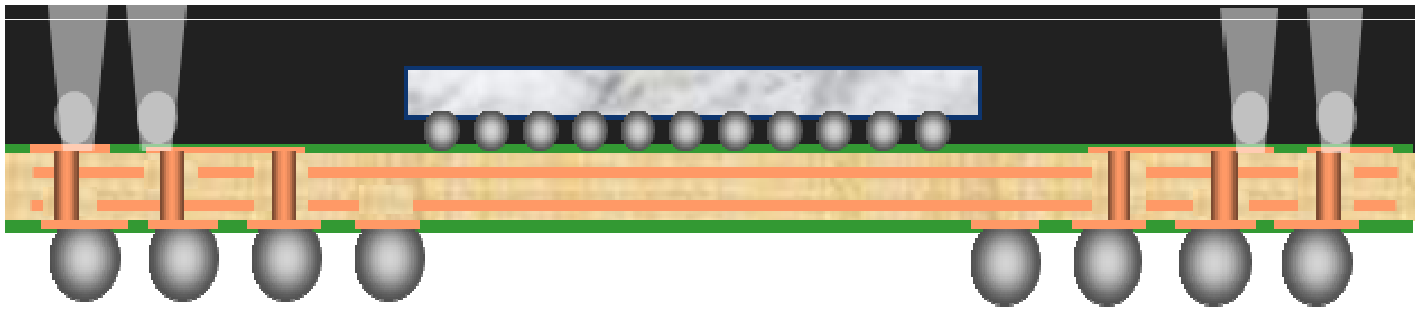
Simulation results



- **Largest impact on EOL package warpage**
  - Cu thickness, especially on inner layers (core)
- **No impact**
  - Dielectric thickness
  - Solder mask thickness

Trial build

- **Package construction**
  - 1-2-1 fcCSP with Cu Pillar & TMV®
  - Pkg: ~12x12mm, Die: ~8x8mm



Trial build matrix

Units: um	Leg 1 - Thicker	Leg 2+3 – SM + Inner Cu	Leg 5 – 'Thin'
Solder mask	26.6	21	23
L1 Cu layer	17.3	18.44	16.96
Dielectric	19.4	21.2	18.6
L2 Cu layer	21.2	17.42	18.16
Core	198	193	199.6
L3 Cu layer	21.88	17.24	18.8
Dieletric	21.4	22	17.8
L4 Cu layer	19.04	17.48	17.6
Solder mask	26.8	20.4	20.8
Total thk	371.62	348.18	351.32

Trial build results

Leg 1		LT	HT
Warpage, µm	Min	19.0	-94.0
	Max	68.0	-69.0
	Avg	37.5	-77.9
	Std dev, σ	11.6	5.9
	3σ	34.9	17.6
	Avg+3σ	72.4	-95.5

Control leg

Leg 2+3		LT	HT
Warpage, µm	Min	18.0	-87.0
	Max	47.0	-69.0
	Avg	29.4	-78.0
	Std dev, σ	7.4	3.7
	3σ	22.2	11.2
	Avg+3σ	51.7	-89.2

Thin solder mask & inner Cu

Leg 5		LT	HT
Warpage, µm	Min	34.0	-77.0
	Max	64.0	-59.0
	Avg	49.4	-67.5
	Std dev, σ	7.0	5.6
	3σ	21.0	16.7
	Avg+3σ	70.4	-84.2

All layers thinner than Leg 1 (except core)

Trial build results (cont.)

EOL warpage at high temperatures

Units: µm	Leg 1 - Thicker	Leg 2+3 – SM + Inner Cu	Leg 5 – 'Thin'
Avg HT Wpg	-77.9	-78.0	-67.5
Std Dev, σ	5.9	3.7	5.6
Avg + 3σ	-95.5	-89.2	-84.2

- **Leg 1 & Leg 2+3 have similar warpage**
- **Leg 5 warpage reduced**
- **Leg 2+3 standard deviation reduced**

Discussion

- **Leg 2+3 data almost identical to Control**
  - Possible reasons for non-alignment with Simulation
    - Magnitude of layer thickness variation
      - Simulation inner-layer Cu thickness variation from Control = 2x
      - Trial build inner-layer Cu thickness variation from Control = 18-22%
    - Core is 2.5% thinner than Control
      - Well known that core thickness has impact on EOL warpage
    - Layer 1 Cu thickness > Control
      - Decreases any gains from thinning inner-layer Cu
- **Leg 5 does not suffer same drawbacks**
  - Core thickness is nearly same as Control
  - Layer 1 Cu thickness < Control
  - Still does not reach full gains as Simulation Leg 5
    - Inner layer Cu thickness not decreased as much as in Simulation

Discussion (cont.)

- **Leg 5 results align most closely with Simulation**
  - Simulation: 61um
  - Trial build: 67.5um

- **Standard deviation considerations**
  - Leg 5 sample size 1/3 smaller, so not discussed
  - Leg 2+3 standard deviation 37% lower than Control
  - Substrate process parameter changed for Leg 2+3 to lower Cu thickness
    - Thinner Cu spec may lead to better process stability & consistency across units (sampling data used)
  - Most warpage specs codified as (W+3σ)
    - Process stability can affect go/no-go when BOM/process changes are not available

Conclusions & Next steps

- **Correlation between layer thickness & EOL warpage studied**
- **Small changes in inner-layer Cu thickness alone may have a small effect on warpage (Leg 2+3)**
- **In combination with core thickness increases and other layer thickness decreases (Leg 5), warpage can be drastically decreased**
- **Thinner Cu thickness may correlate with substrate manufacturing stability**
  - Possibly a tool for hitting EOL warpage specs when BOM/process changes are unavailable
- **Next steps**
  - More trial build data
    - Larger thickness variations (non-core layers)
    - Smaller core thickness variations
  - Study impact of Cu density on EOL warpage

Thank you

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