Thermal & mechanical challenges for 3DIC integration

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Agenda

- 3DIC context
- Thermal challenges
- Mechanical challenges
- Conclusion & Prospects

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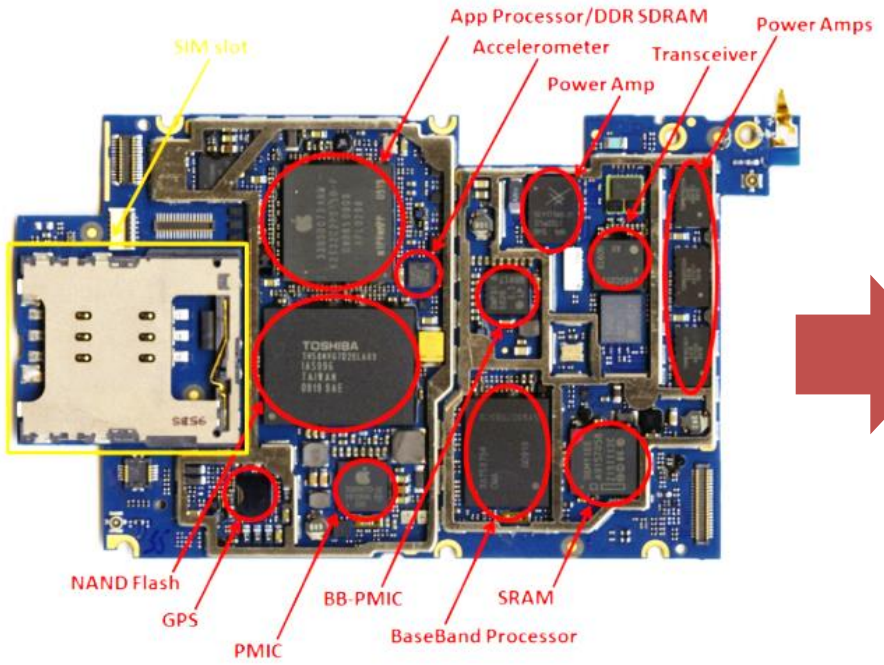
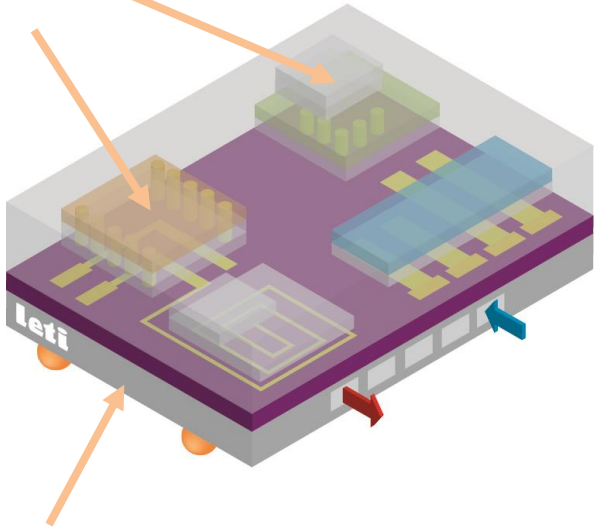
Why 3D integration?

To integrate complex electronic systems on silicon



System on board
(Smatphone PCB)

3D ICs

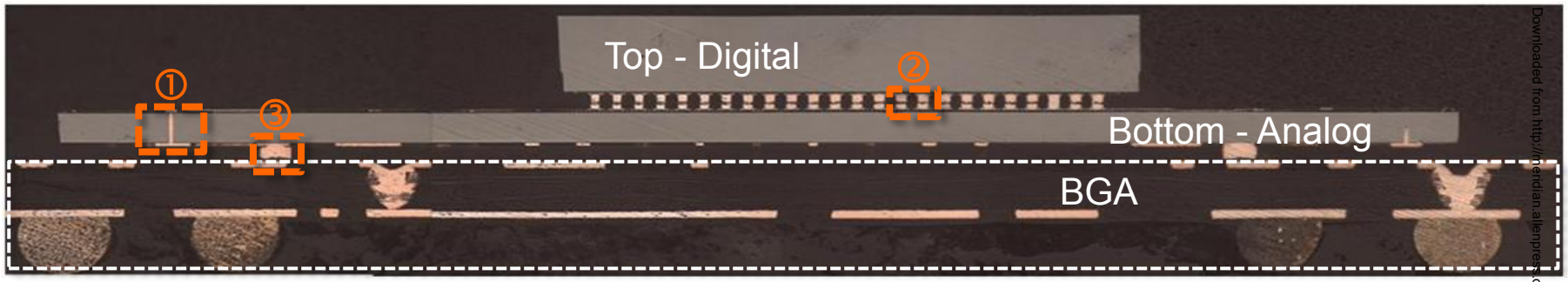


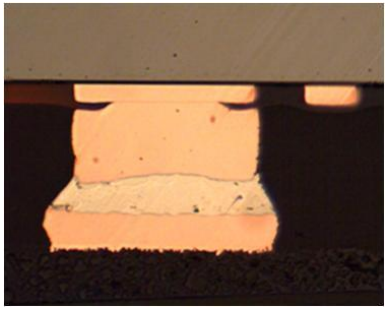
A silicon interposer

With very heterogeneous dice on it (various substrates, various technologies co-existing, various chip makers…).

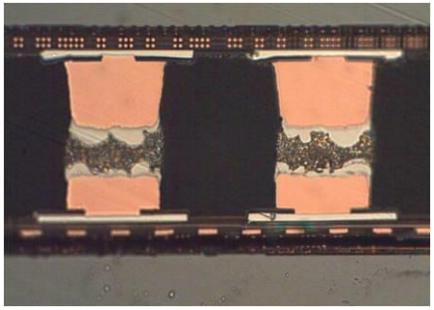
Smaller, more functionality, higher performance

3D @ Léti: Digital – Analog partitionning

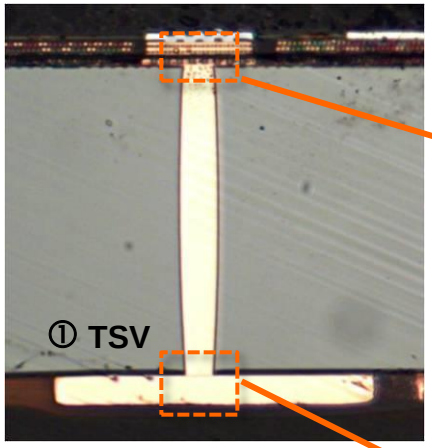


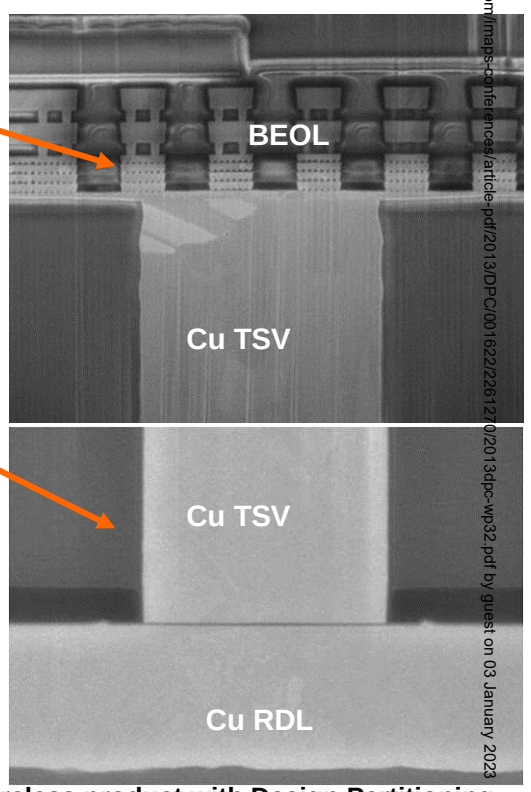


③ Die - BGA connection



② Die - die connection

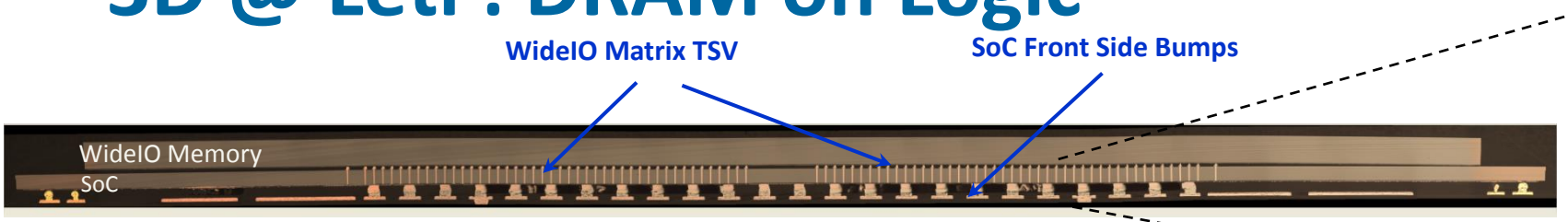


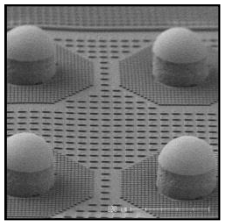


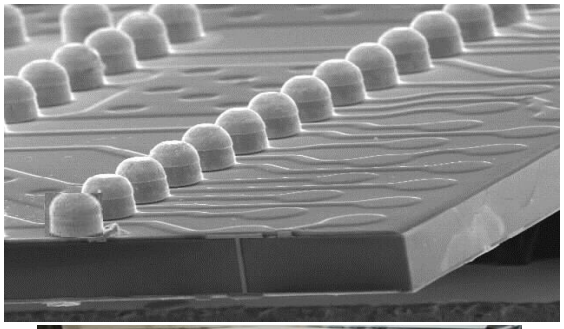
- Wireless application
  - High definition video transmitter, >1GHz
  - Integration technology proven and concept demonstrated
    - TSV + 7 metal layers, 65nm technology

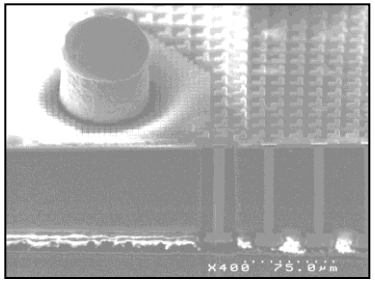
3D Integration of a Wireless product with Design Partitioning
G. Druais et al., 3DIC 2011

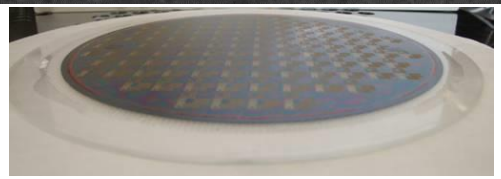
3D @ Leti : DRAM on Logic

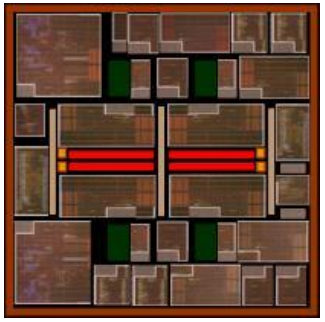










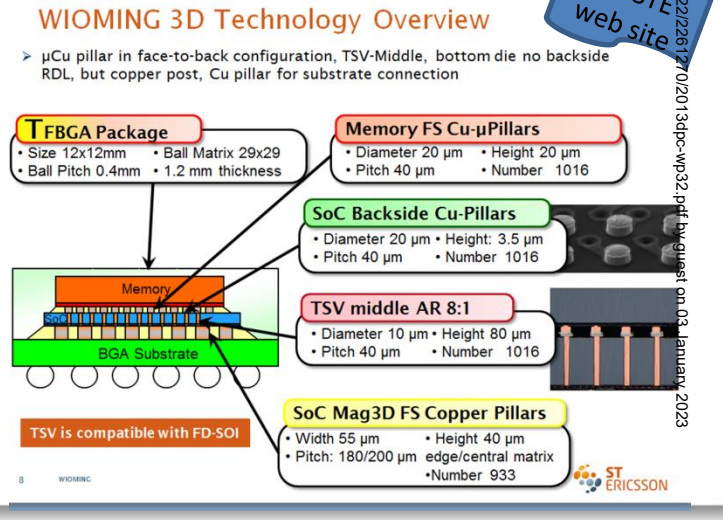


In collaboration with

ST ERICSSON

On STE web site

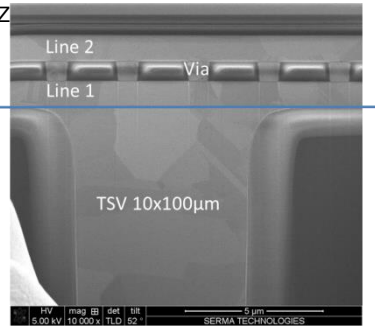
Memory type	LPDDR2	LPDDR3	WideIO
Package	PoP	Pop/Discrete	3D-IC
Bandwidth (Gbyte/s)	8.5	12.8	12.8
Power efficiency (mW/Gbps)	9.75	5.88	**2.86**

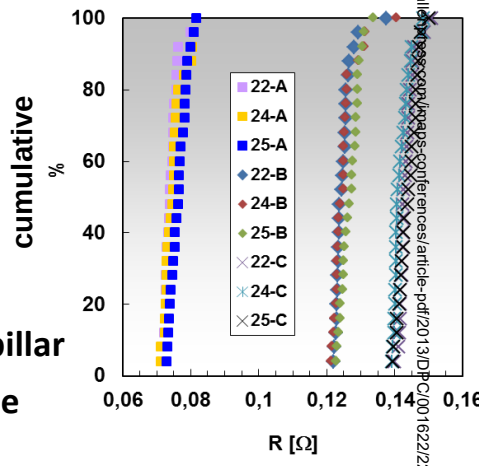


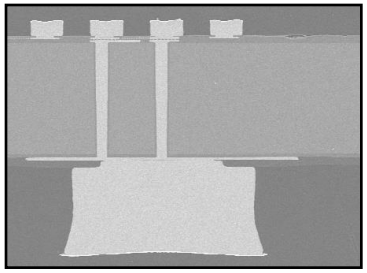
200mm & 300mm processes & characterization for face to back flow chart for Wide I/O, *S. Chéramy & Al, 8th International Conference and Exhibition on Device Packaging (2012)*

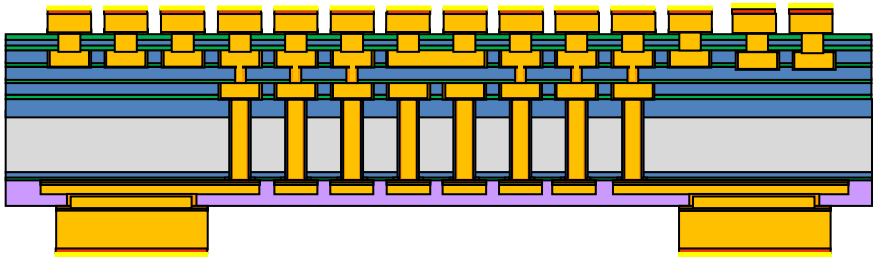
3D @ Léti: Silicon Interposer

- **Interposer size**: 26x26mm² (warp management required)
- **TSV**: 10x80µm and 10*100µm
- **Cu damascene routing** : Metal1-Via1-Metal2, **0.5µm line/0.5µm space**
- **Micro copper pillars**: Pitch 50µm, **100 000/interposer**
- TSV exposure
- **RDL and passivation**: 10µm Line / Space, one level
- **Large copper pillar**: pitch 500µm, height 70µm









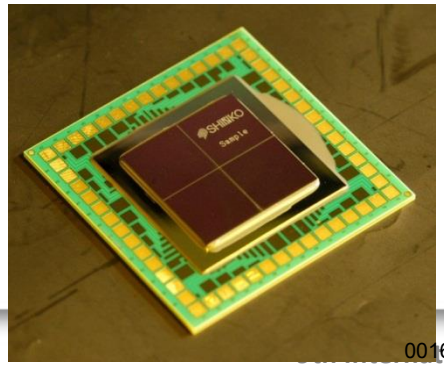
Micro Cu pillar

Damascene

TSV

RDL and Passivation

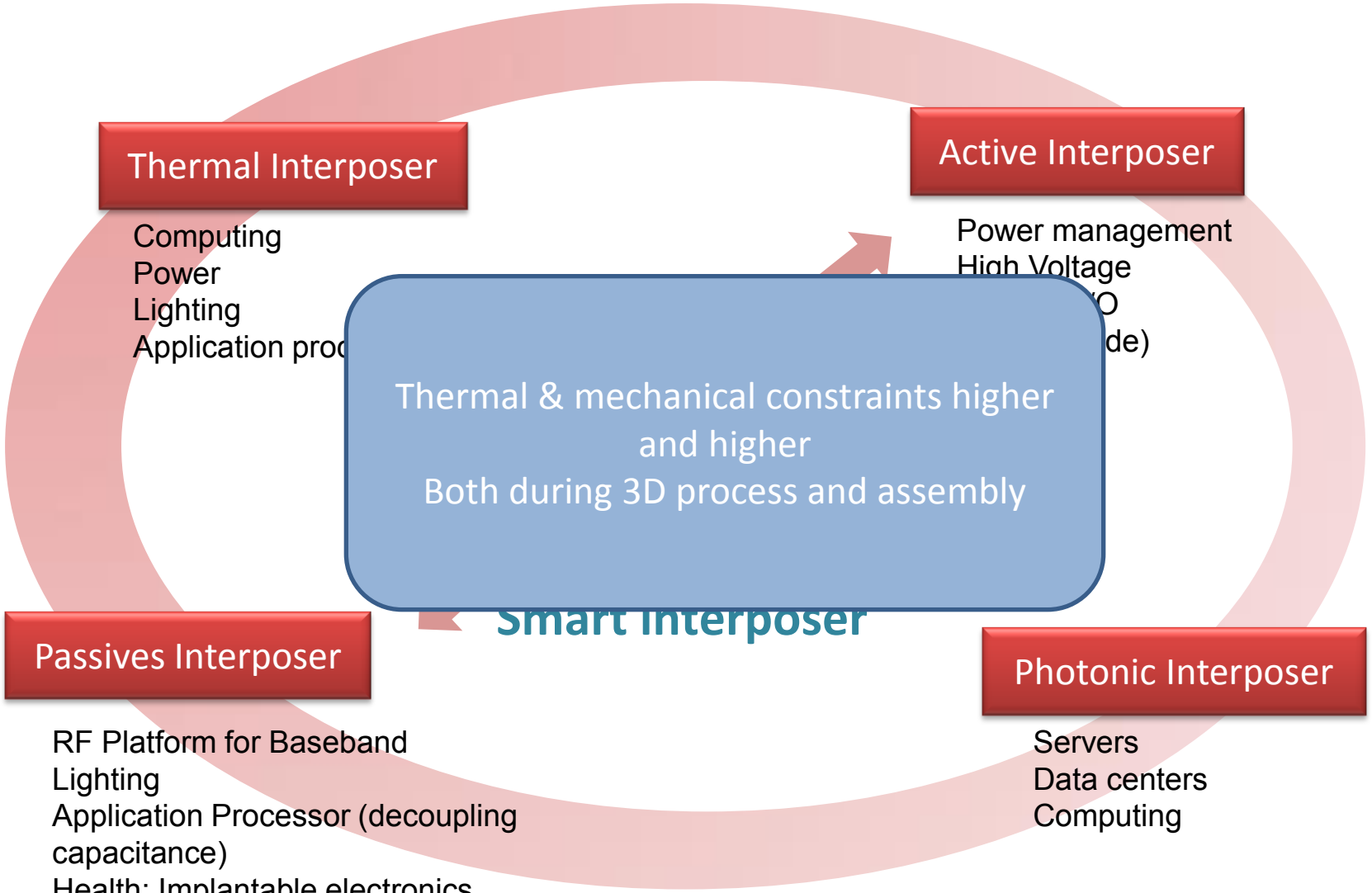
Large Cu Pillar



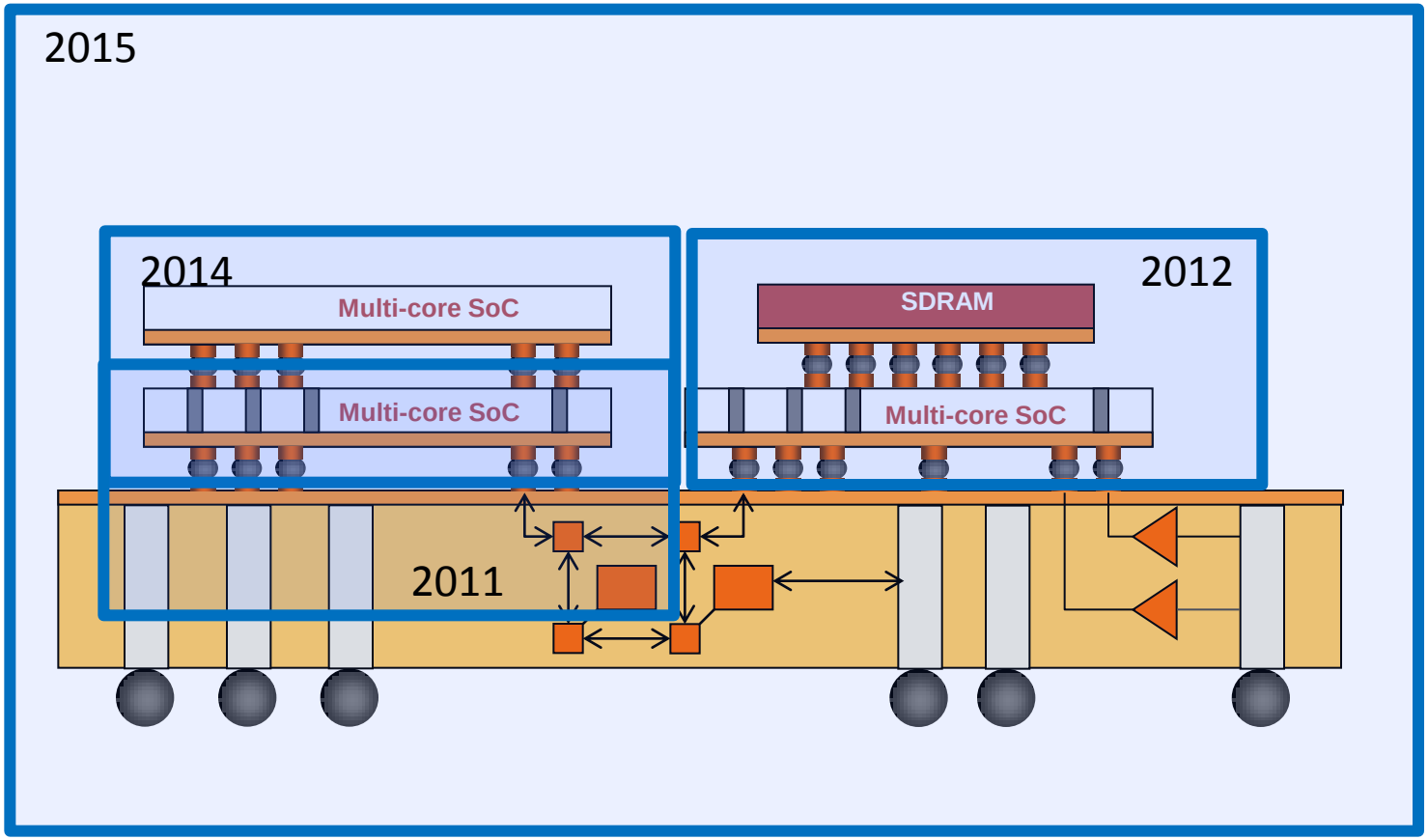
Leti SHINKO *Joined Lab*

J. Charbonnier et al., ESTC 2012

Smart and complex interposer



3D @ Léti, next steps: Partitioning for Flexibility

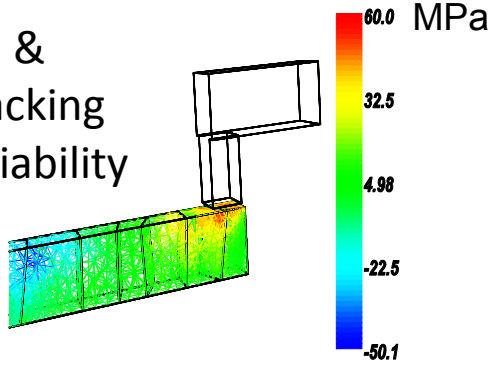


- ➔ More and more complex
- ➔ More and more thermal sensitive
- ➔ Larger and larger

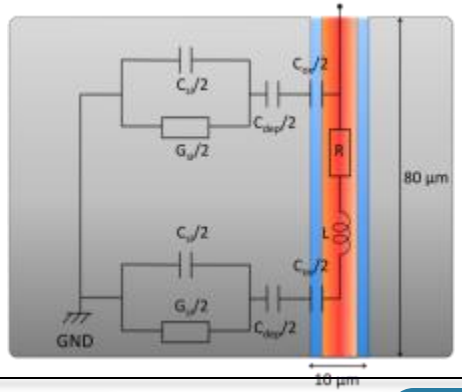
3D performances assessment

3D specific reliability

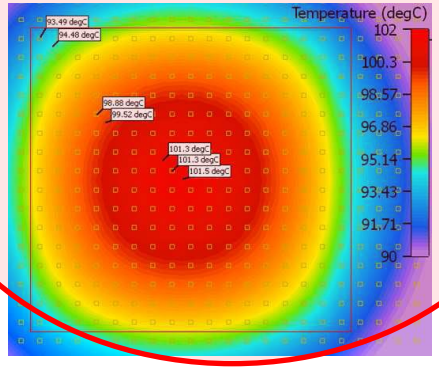
3D & stacking reliability



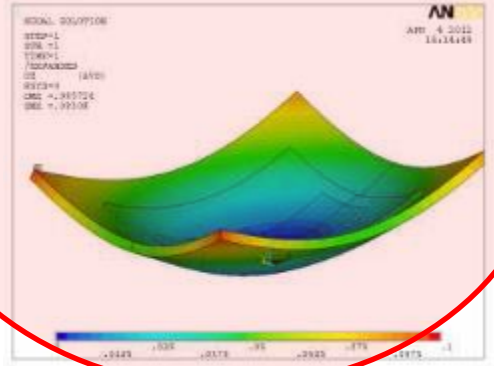
RF Model



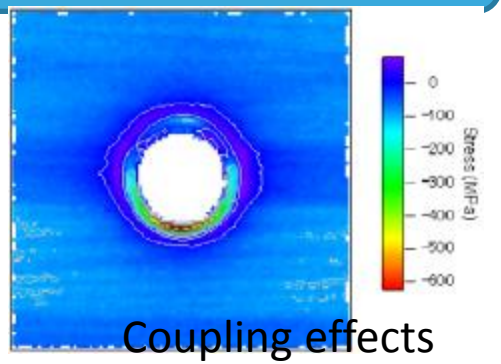
Thermal



Thermo-mechanical



TSV & substrate impact on MOS



Coupling effects

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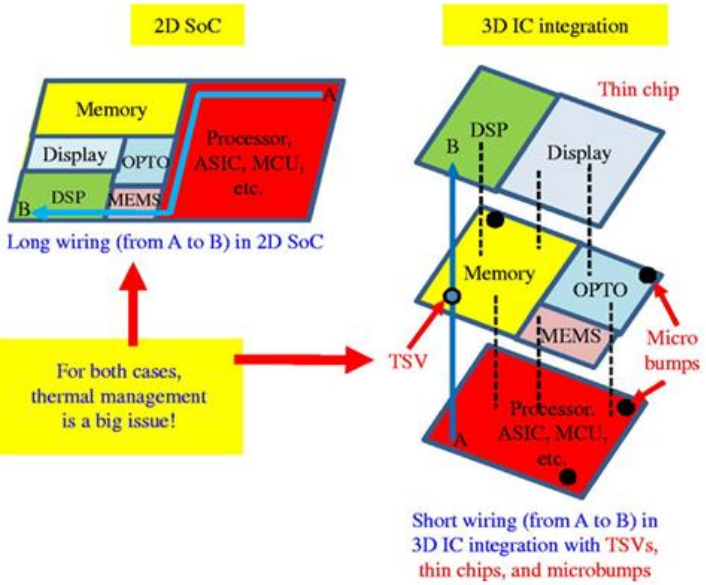
Thermal challenges

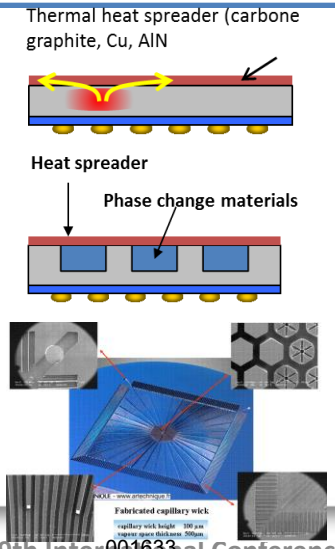
Thermal issues



- Increased **heat dissipation** per unit surface area
- Poor **thermal conductivity**
- Inter die **heating**
- **=> increase temperature max in the stack**

Model and design rules

- **Simulation**
- **Measurement based on a specific thermal stack**
- **Thermal characterization**

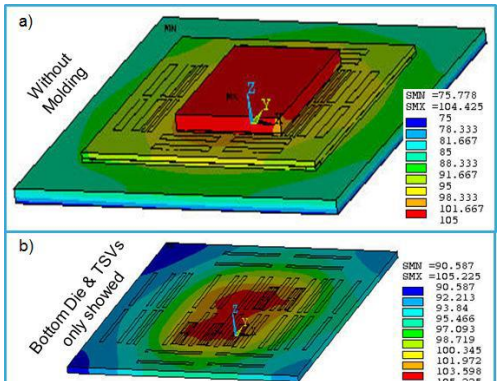


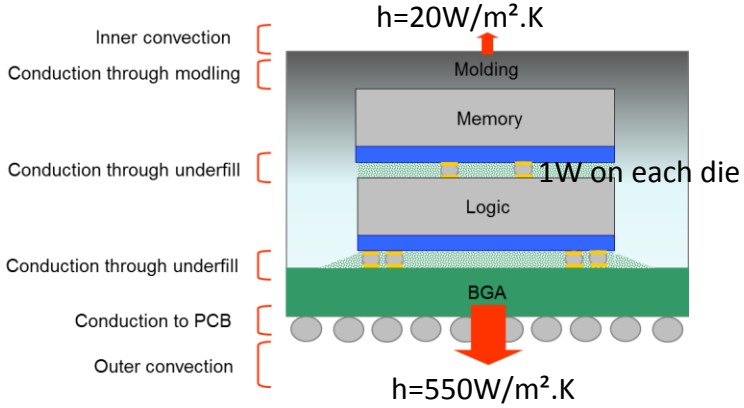
Thermal solutions

- **Lateral heat speader**
- **Dynamic smoothing**
- **Extraction**

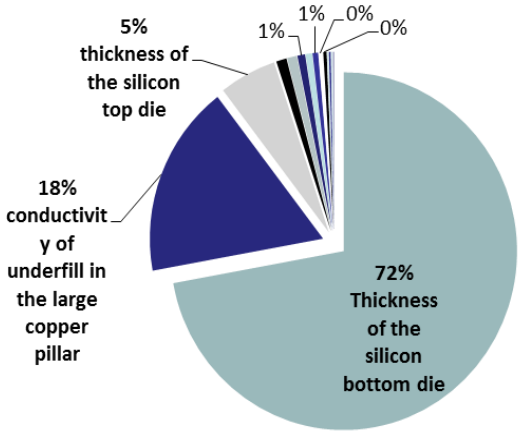
Thermal simulation of a 3D stack

Max temperature in bottom and top die is similar – spreading is different



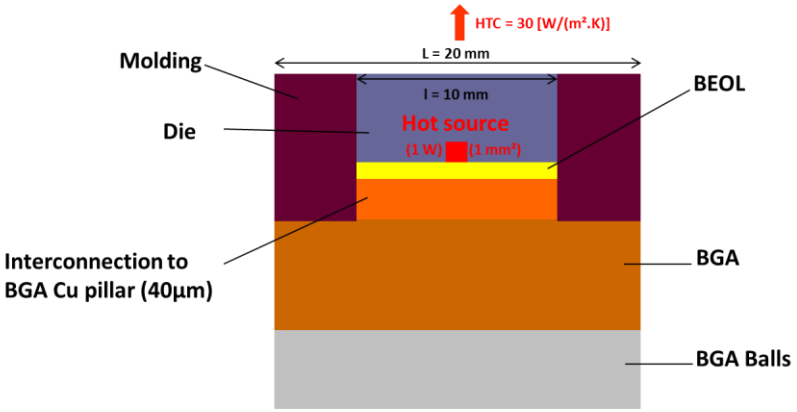


Thickness of the bottom die is the 1st influent factor

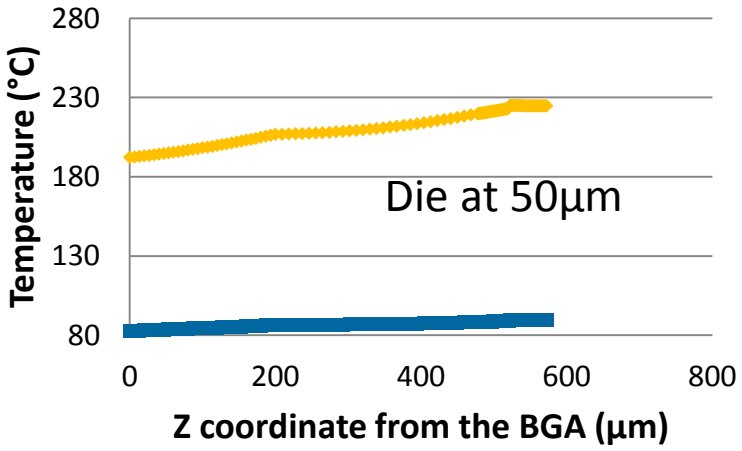


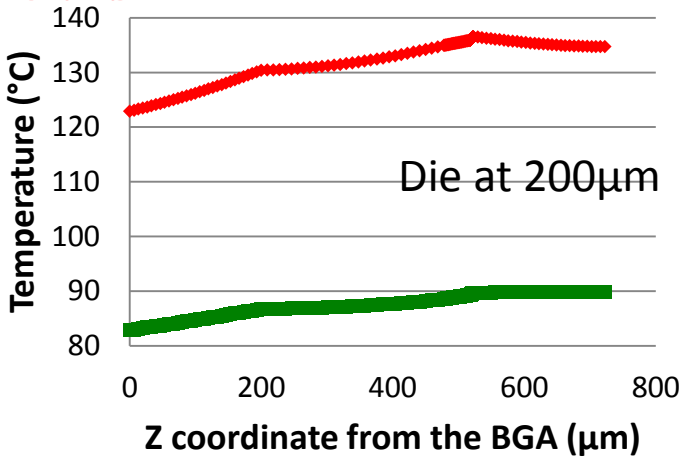
Thermal behavior in stack-based 3D Ics, *ESTC 2012*
P. Momar & Al

Bottom die thickness influence



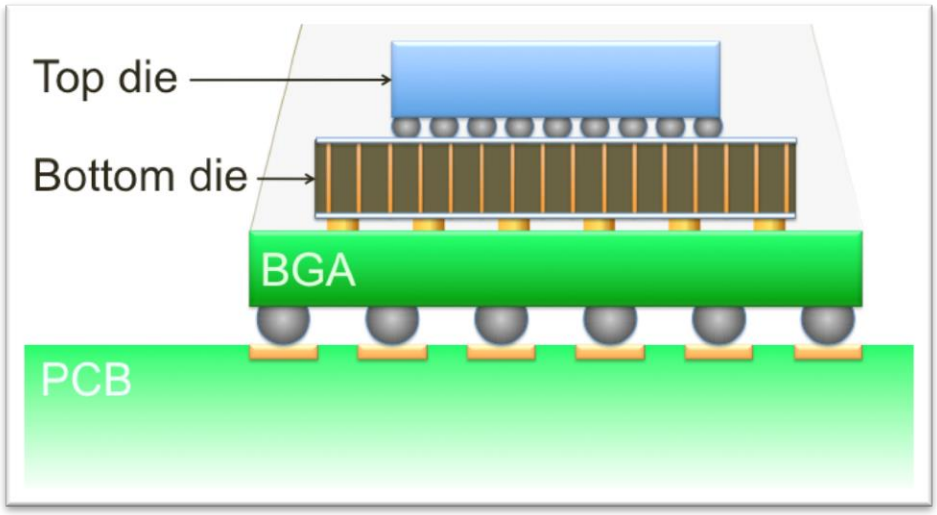
Boundaries conditions taken to allow comparative study



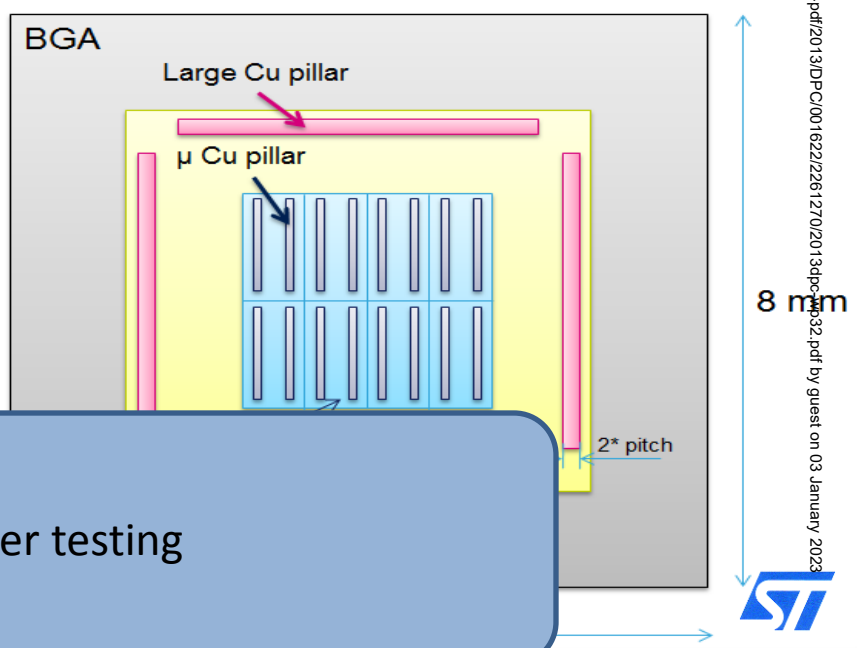


Increase the thickness from 50 to 200µm leads to a 30% temperature decrease

Thermal stack



- **Dies** are composed of **test circuits**
- **Heating element** (like transistor) and **temperature sensors** (like diodes or resistors)
- **4 heater** cores per **test circuits**

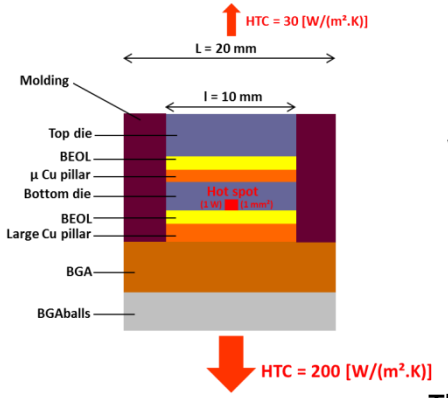


- **Comparison and fit with 3D stack simulation possible**
- **=> Drawing of simulation with alternative mat… interconnect di…**

Currently under testing

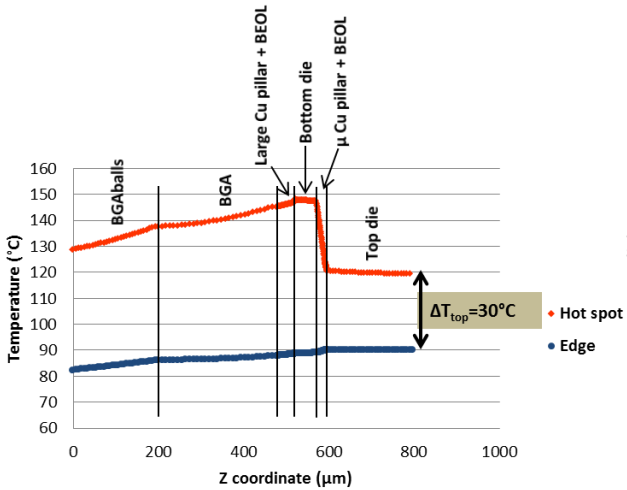
Heat spreader onto the 3D stack

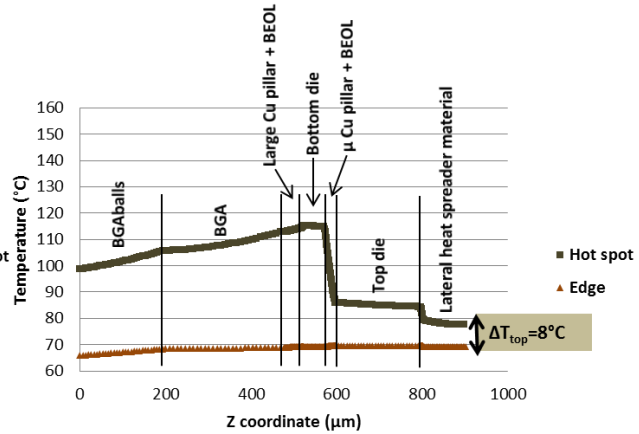
Possible heat spreader material : Cu (400W/(m.K))/ graphite sheet (from 1000 to 1600W/(mK) in x & y)



With or without heat spreader on top of the package

Theoretical study of the thermal impact of a passive heat spreading layer integrated in 3D mobile device, *S. Salman, JP. Colonna & Al, Imaps 2013*





Clear trend: a decrease of more than 30°C is measured both on top and bottom die

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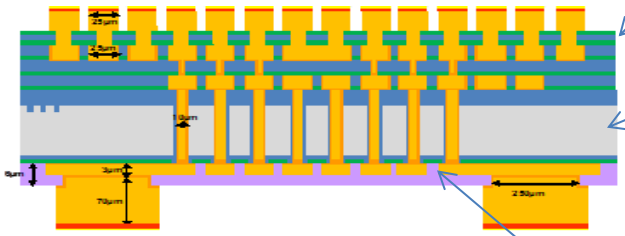
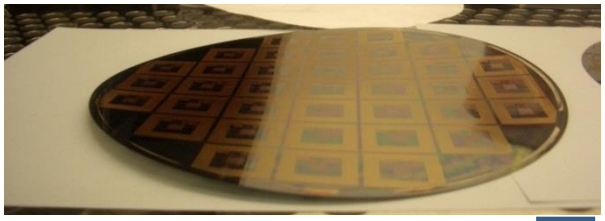
Bow management

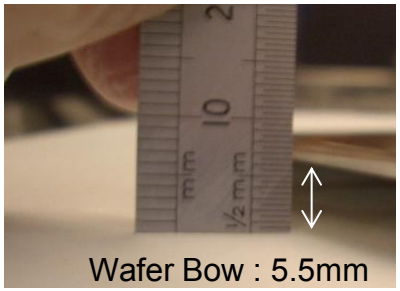


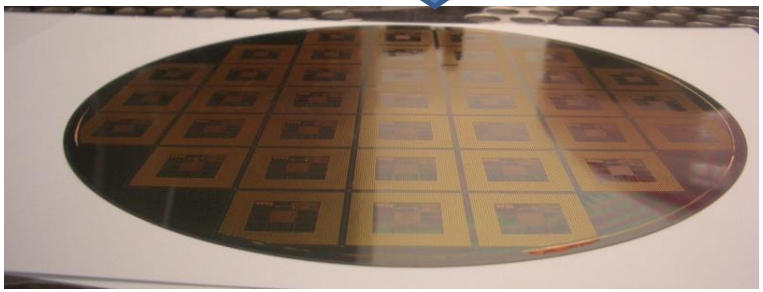
BEOL: Several microns of heterogeneous layers

<100µm Silicon and very large dies (> 25*25 mm)

Backside Process: also an heterogeneous stack…but not the same

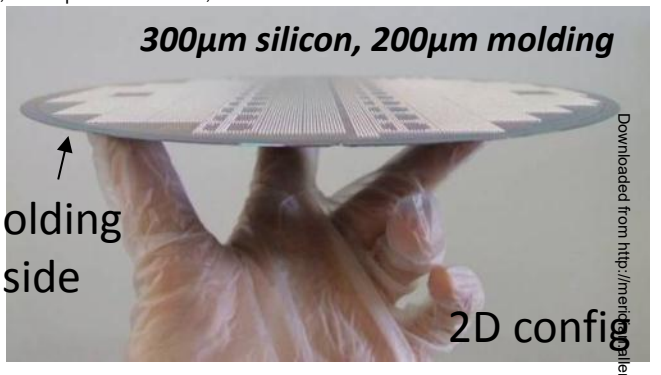


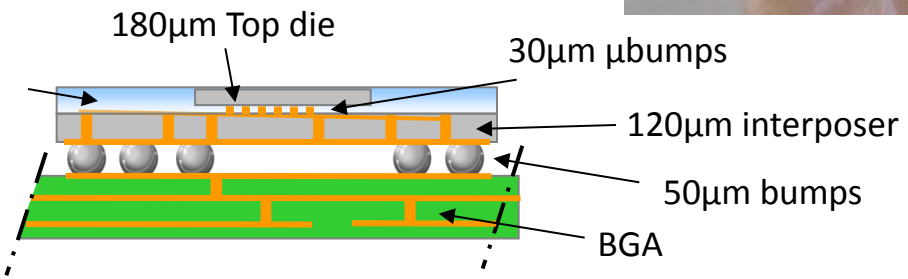




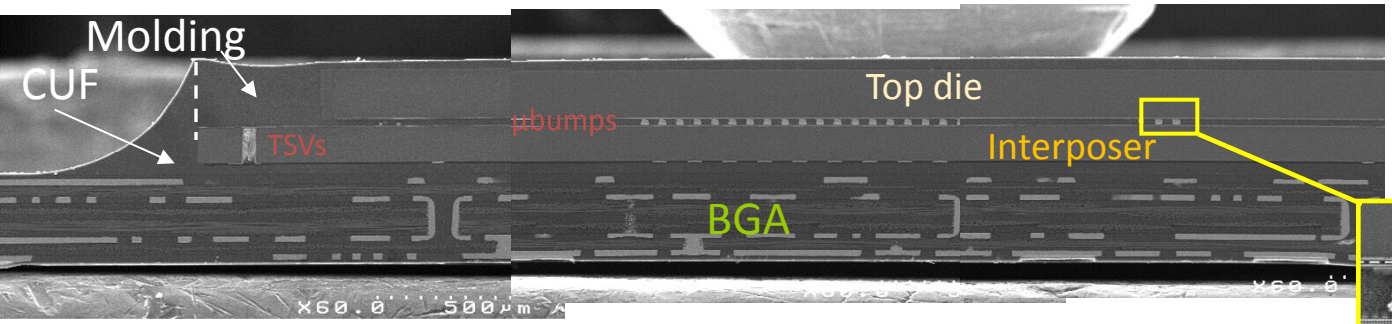
- Solutions:
  - Dev. of low stress material both sides - Insertion of polymer compensation layers
  - Add compliant interconnects
  - Increase interposer thickness
  - Polymer encapsulation
- A keypoint to go to very large interposer

Polymer encapsulation

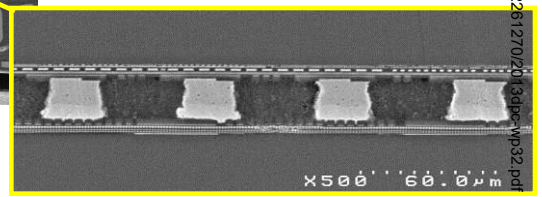




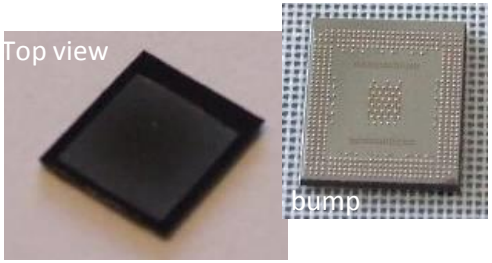
Innovative Wafer-Level Encapsulation & Underfill Material for Silicon Interposer Application, *ECTC 2013, C. Ferrandon & Al*



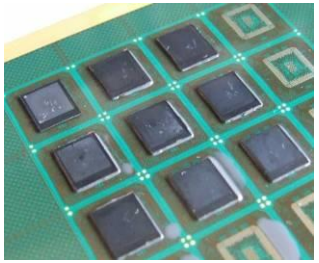
1st level
100% molding under-filling



Top die and interposer creation – die to wafer stacking at LETI

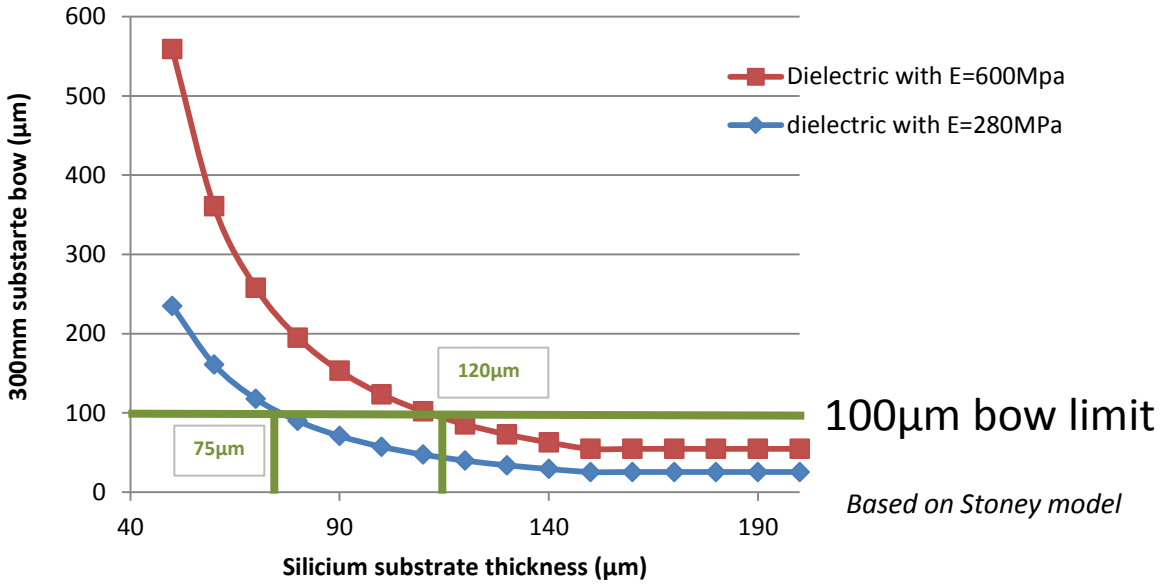


Molding/underfilling and dicing at LETI



Report on BGA/CUF at ST

Interposeur thickness



120µm to 150µm minimum thickness would be necessary to obtain raisonnable bow – Aspect ratio TSV from 15 to 20 necessary

Thickness from 100 to 150µm decreases the warp by a factor of 2!

Submitted at EMPC 2013, Grenoble France, J. Charbonnier

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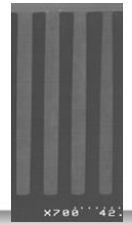
Conclusion & prospects

- 3DIC is the future of 2,5D but with some specific challenges to be addressed now
- …Among with thermal and mechanical challenges

- 2,5D already faces to mechanical challenges – will be even more critical on active silicon
- Thermal challenges must have dedicated solution Vs application

- Both challenges have a common solution : increase bottom die thickness

Work on high aspect ratio TSV is a must



AR15:1

Aknowledgments

- To Léti Cea team

- To our partners ST and Shinko

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Thanks for your attention