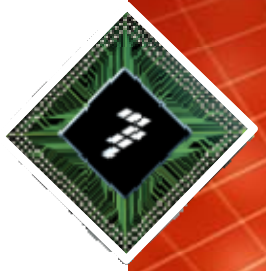
Reliability and Performance Improvement of 3D System-in-Packages in Fan-Out Wafer Level Packaging

Scott Hayes, Tony Gong, Doug Mitchell, Michael Vincent, Jason Wright, Yap Weng Foong
Freescale Inc.



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Outline

SiP/3D Packaging

- Motivation
- Current SiP approaches and 3D enablers

SiP in Fan-out Wafer Level Packaging

- The Redistributed Chip Package (RCP) Technology
- SiPs in RCP
- Critical RCP SiP Structures

The RCP Through Package Via (TPV)

- Process and Reliability
- Electrical Characteristics

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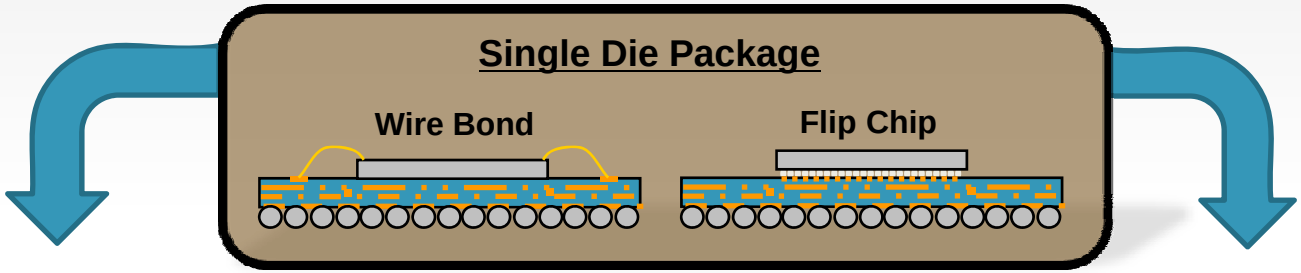
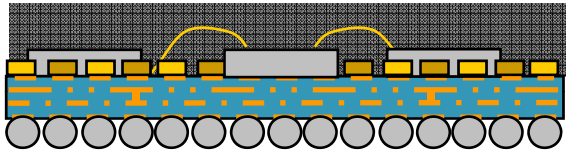
System in Package (SiP) Motivations

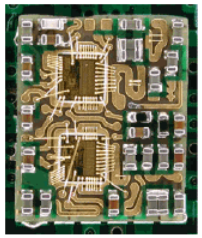
- Performance
  - Die/system performance improvements
- Size/Volumetric Efficiency
  - Smaller footprint, thinner packages
- Heterogenous Integration
  - Die of different nodes/thickness, SMT, discrete components, MEMS…
- Differentiating Solutions
  - SiPs increase opportunity/accessibility for unique systems

Standard Package and SiP Approaches



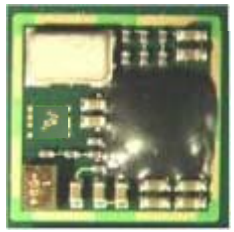
Multi-Chip Modules
(WB, FC, SMD)





-Agilent

-STATSChipPAC



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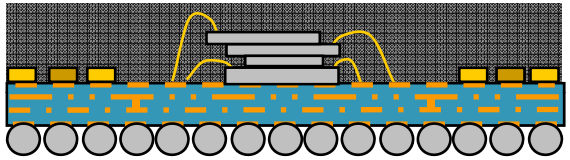
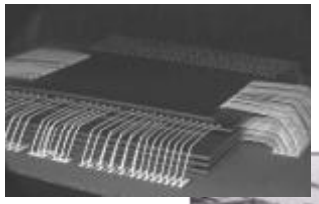
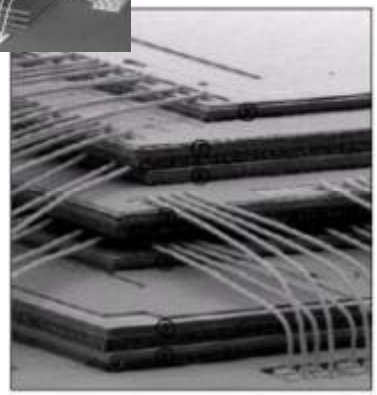
Stacked Die
(WB, FC, SMD)



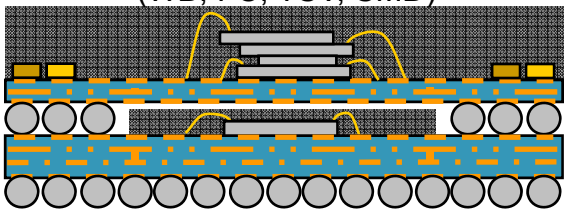


-Toshiba



-ECN

Package on Package
(WB, FC, TSV, SMD)



-Amkor

-STATSChipPAC

-ESCATEC

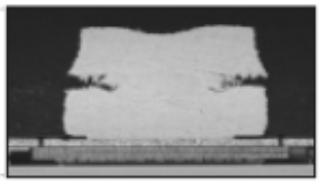
Some Additional SiP/3D Technologies

Double Sided Flex

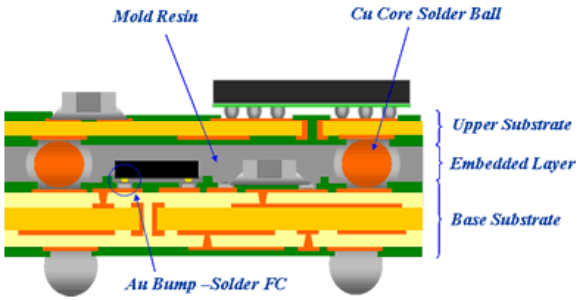
-Starkey

Embedded Substrates

-Imbera

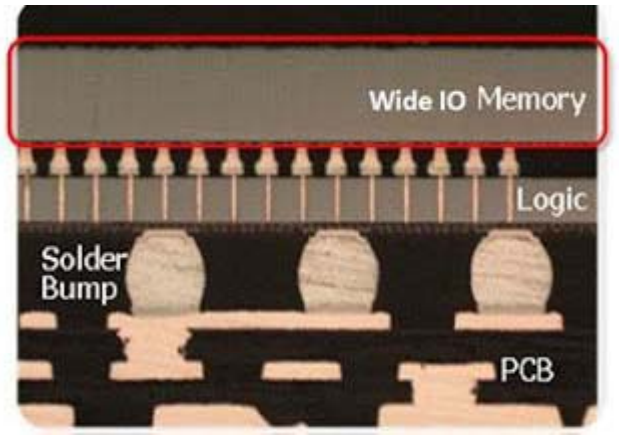


-AT&S



-Shinko

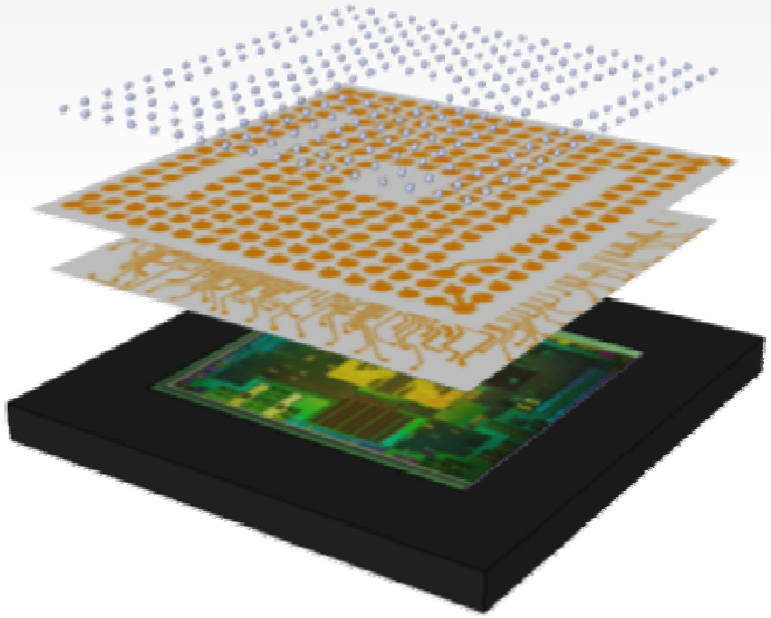
TSV/Si Interposer

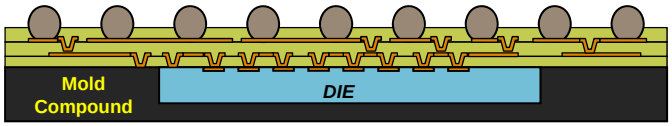


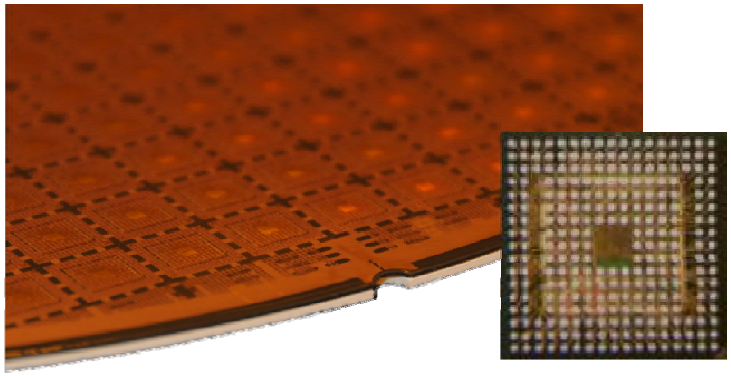
-Samsung

Freescale Redistributed Chip Packaging (RCP)

- Freescale proprietary technology.
- Scalable, fan-out chip scale package.
- A technology solution for:
  - Small form factor packages
  - High performance.
  - Multi-die, heterogeneous integration.
- 2D, 3D System in Package (SiP) solution.
- Key Applications
  - Medical
  - Defense
  - Migrate to Consumer, Industrial & Auto







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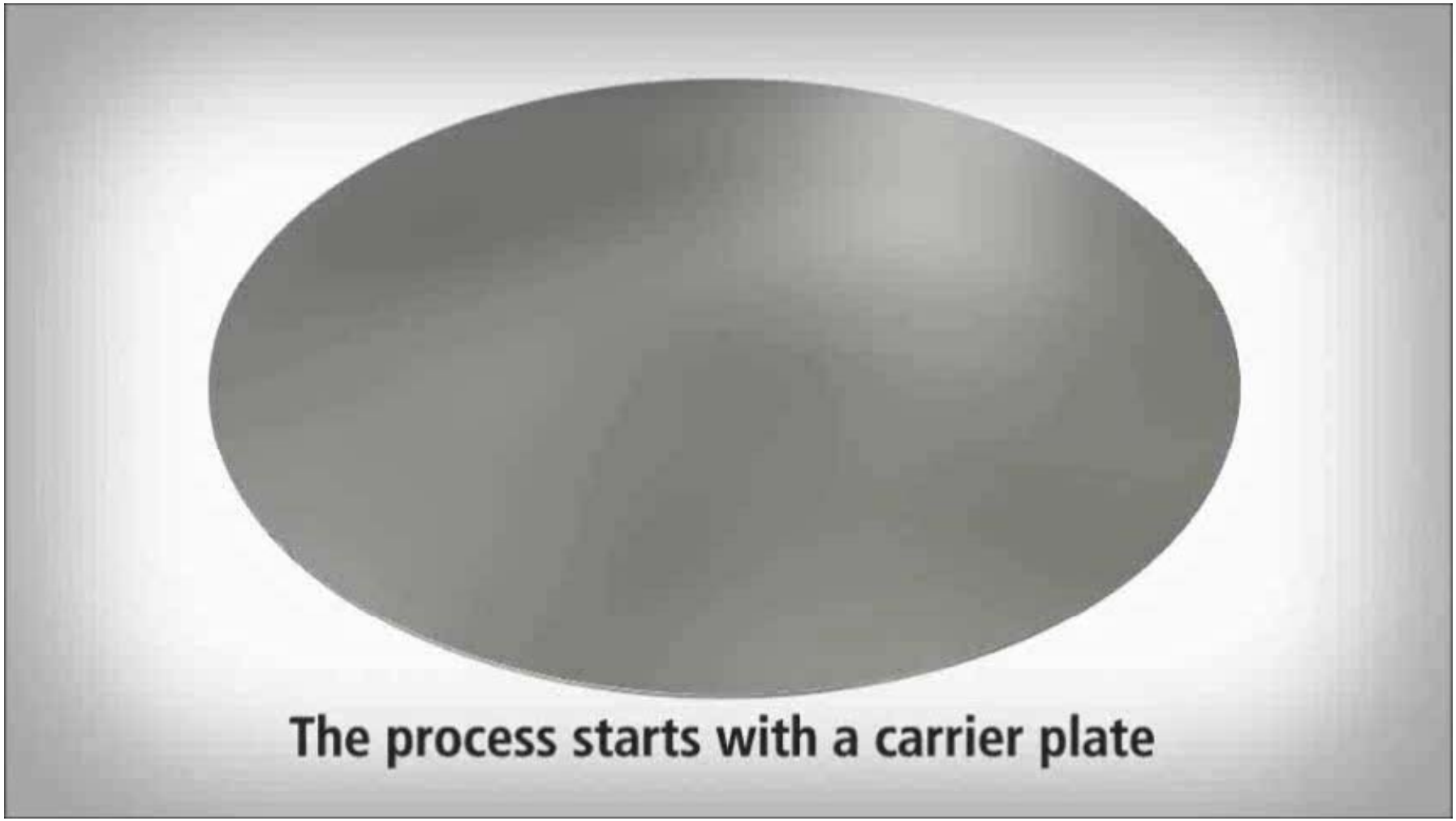
Freescale's Redistributed Chip Package (RCP)



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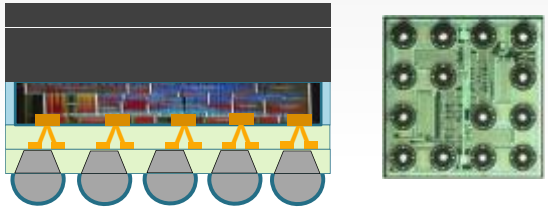
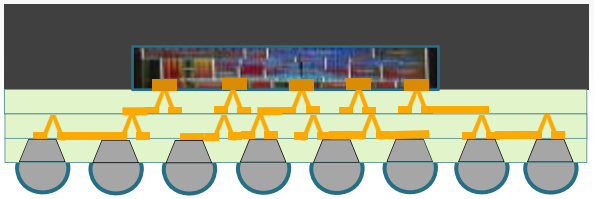
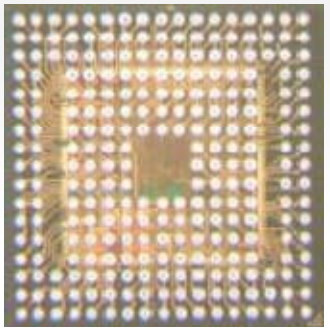
Fan in vs. RCP Fan out packaging

Fan-in Wafer level CSP

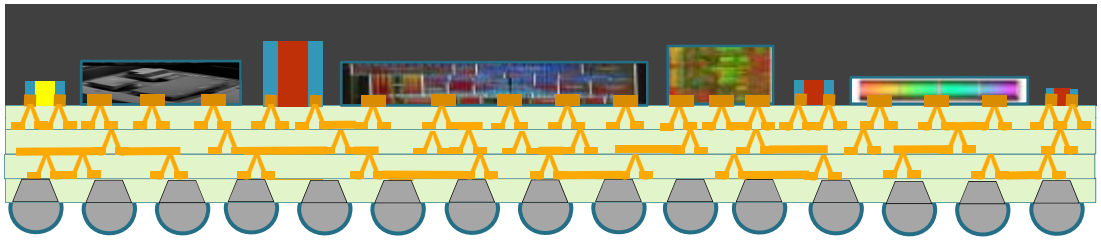


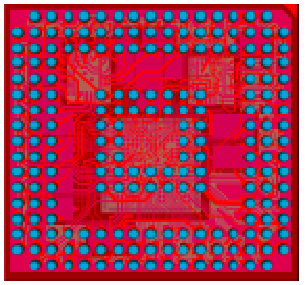
Fan-out single die RCP



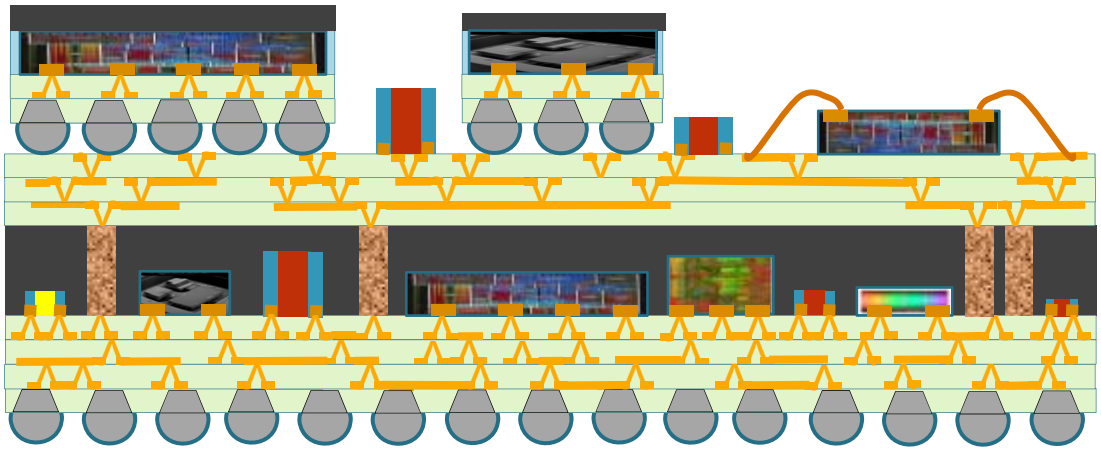


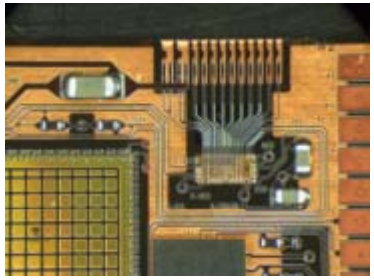
Fan-out multi die RCP (SiP)

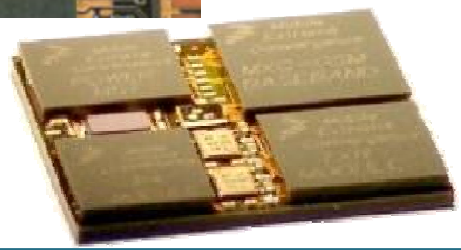




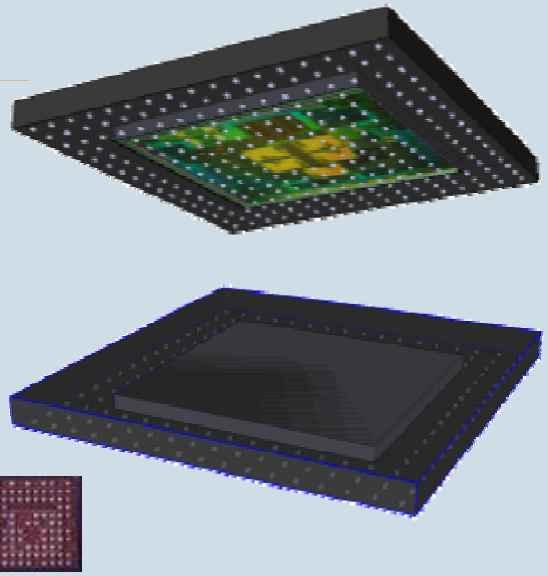
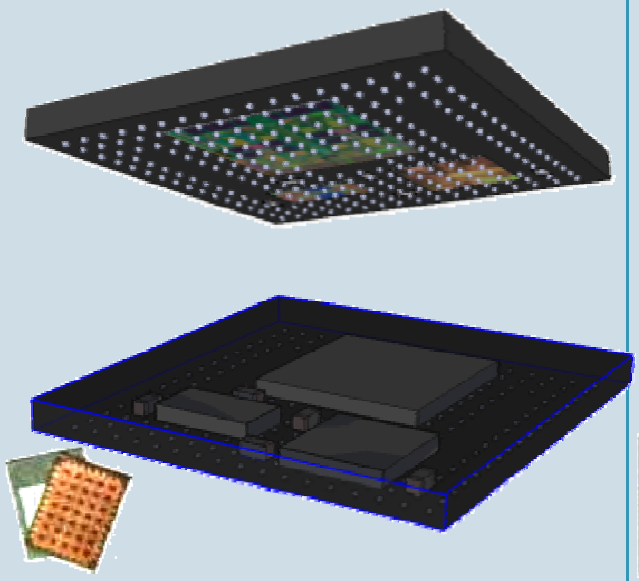
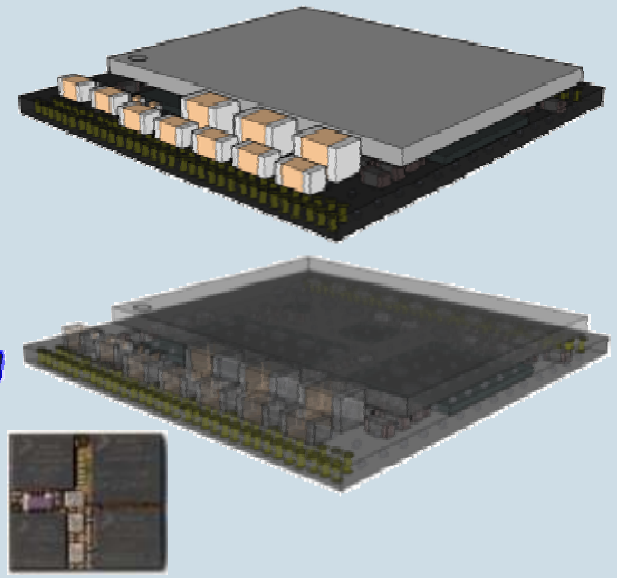
Fan-out 3D RCP (SiP)







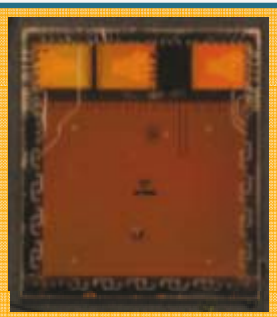
RCP and RCP SiP Manufacturing

Single Die Package	2D Multi-die Package	3D System-in-Package
XY: pkg. size: die size + 0.5mm + Z: Low profile ~ 125-760µm	XY: Fine die-die spacing rules Z: Low profile ~ 125-760µm Embedded components	XY: Fine die-die spacing rules Z : SMT dependent
		
• Prototypes: Now • Production: Now	• Prototypes: Now • Production: Q2'13	• Prototypes: Now • Production: Q4'13

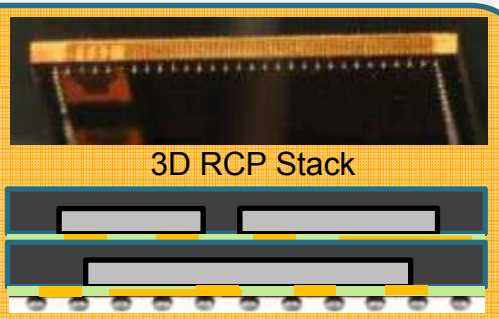
Methods of Achieving 3D in RCP

Stacking

- Edge connections
- Very thin
- Routing constraints



RCP-SiP Layer

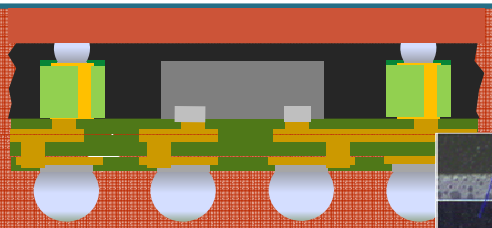


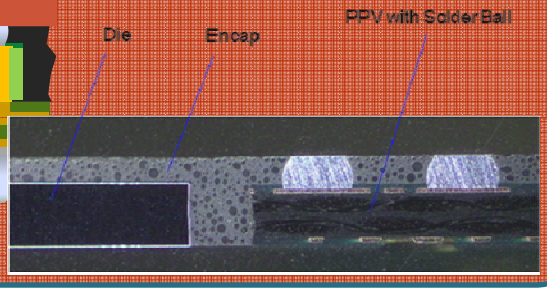
3D RCP Stack

Two laminated layers, BGA

Pre-placed vias

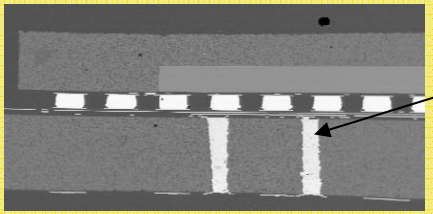
- Lower cost
- Good use as PoP solution
- Simplified process
- Limited double sided build up

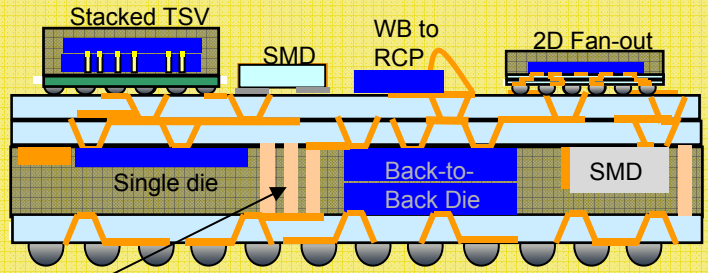


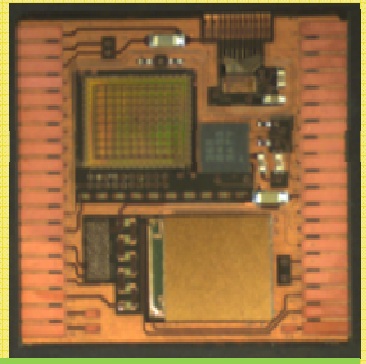


Through package vias

- Minimal routing constraints
- Double sided buildup
- Use of RCP as a 'PCB'
- Most flexible solution







Enables 3D SiP solutions for unique medical, defense and consumer applications

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RCP SiP/3D Integration

Integrated Elements
Processor, uController, PMIC, ASIC
RF (baseband, transceiver)
FET, IGBT, RGT, SCR
Film Battery
Memory (DDR, Flash, SDRAM)
MEMS (accelerometer)
IPD, SMD (R, L, C)
Oscillator
mmWave (Tx-PA, Rx, VCO)
Thin Film Resistors
Shielding, Thermal management

Demonstrated Applications/Constructions
Low Voltage applications
High Voltage applications (~1kV)
Single Die, 2D Multi-die, 3D SiP, Stacked SiP packages.
BGA, micro-BGA, Flex connectors, wirebond.
Ultra thin packages
High density packages (>100 units in BoM)
Contactless, remote functions

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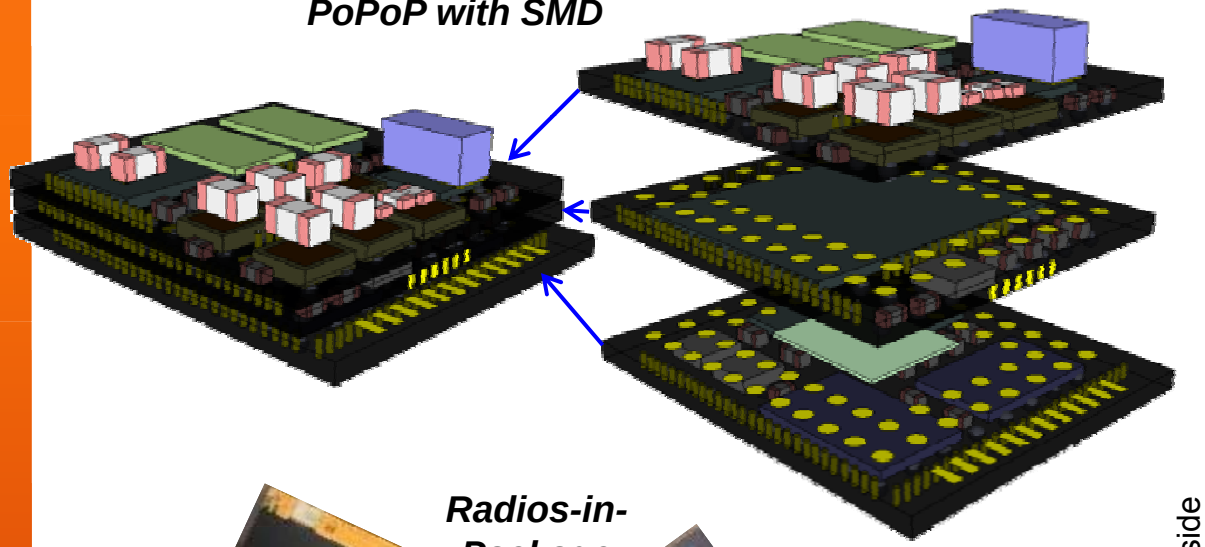
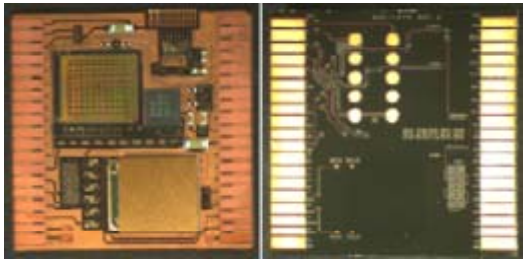
A Few Applications Enabled by RCP TPVs

- Applications include TPVs and double sided build up.
- SiP BoM counts range from 2 to >100.
- Common systems include processor, memory, ASIC, MEMS, discretes.

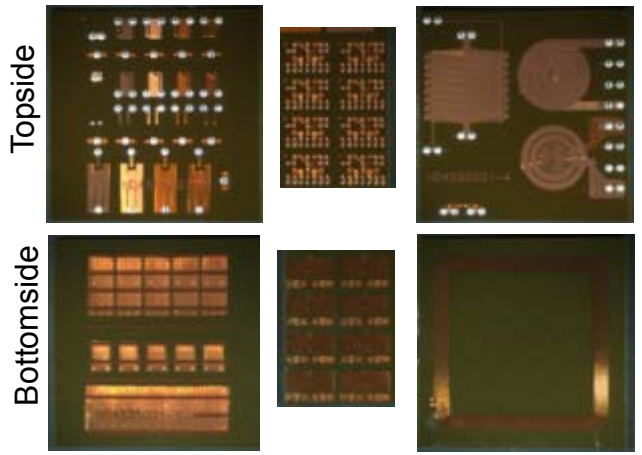
PoPoP with SMD



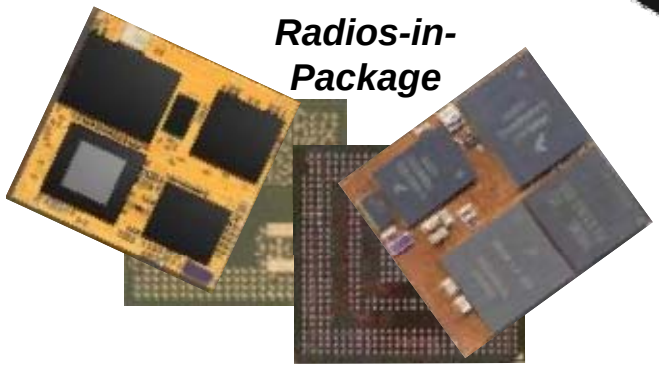
RCP-3D SiP with MEMS



High Voltage and Charging TVs



Radios-in-Package



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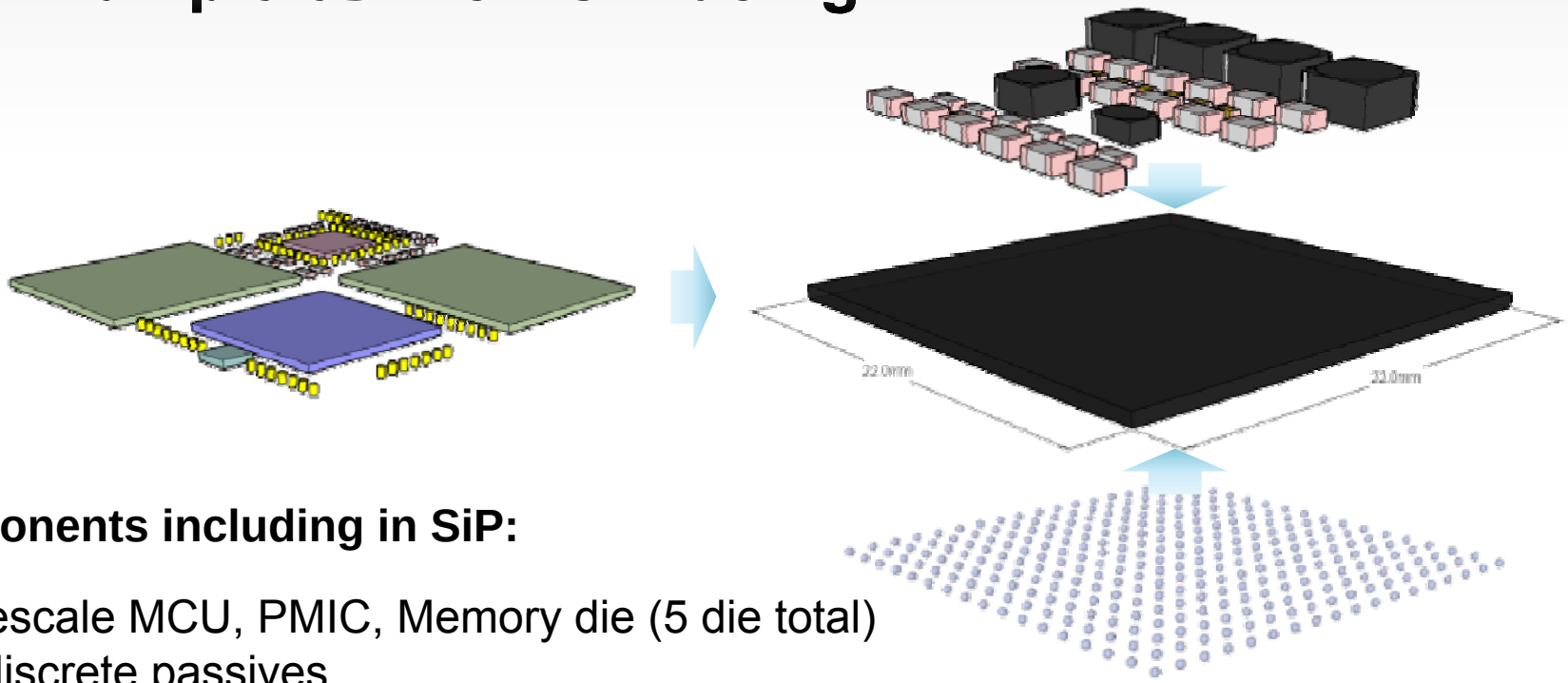
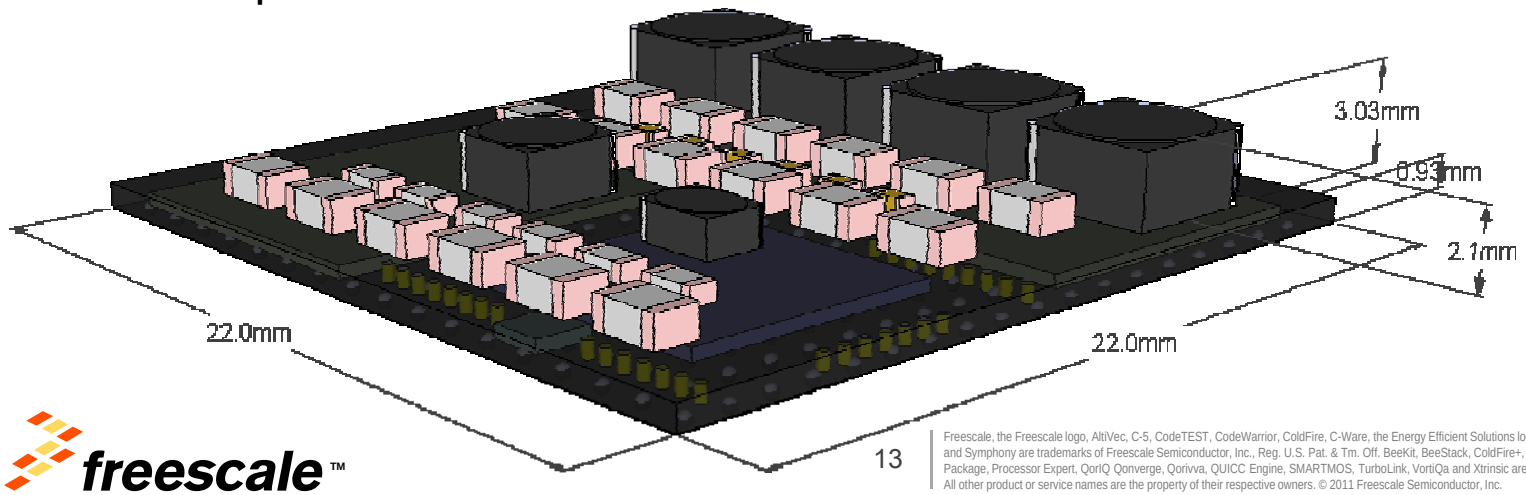
Example 3D RCP SiP using TPV



Components including in SiP:

- Freescale MCU, PMIC, Memory die (5 die total)
- 68 discrete passives



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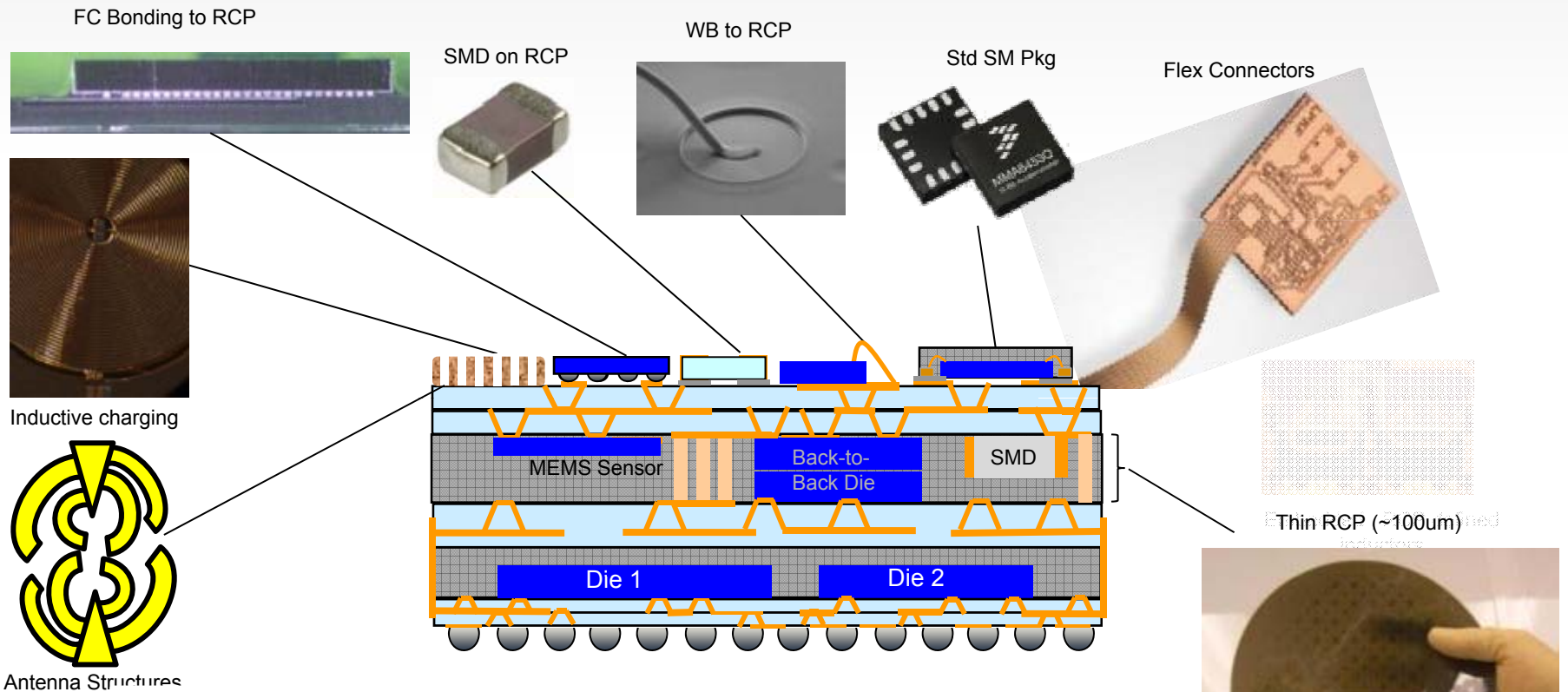
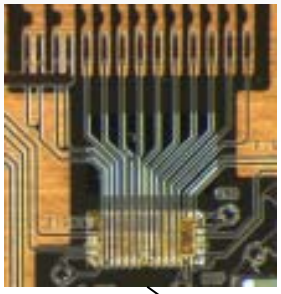
RCP SiP/3D 'Building Blocks'



RCP SiP/3D 'Building Blocks'

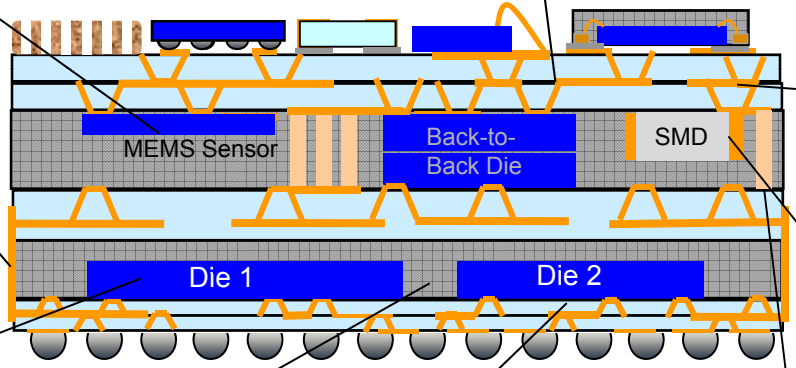
Embedded Sensors

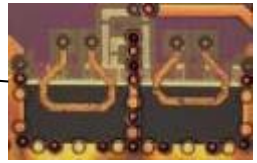


Multiple layers of signal routing including power, ground, and signal isolation

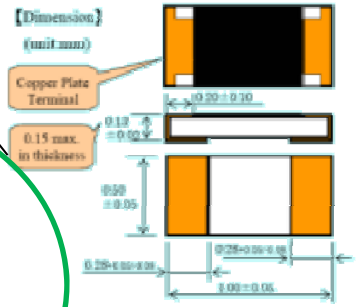
M1
M2
M3
M4

Ultra Thin Pkg Stacking with Side Connections

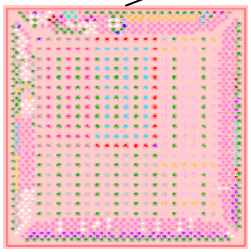




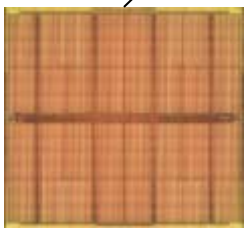
Embedded , RCP defined inductors



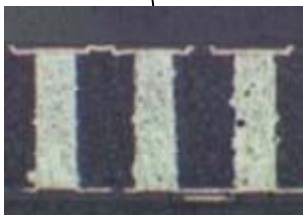
Embedded SMD



High Pin Count Embedded Die



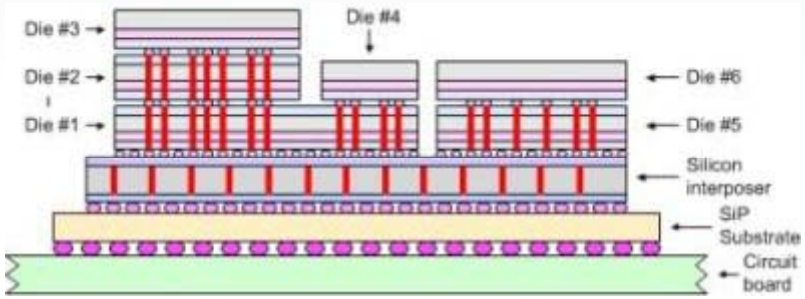
Memory



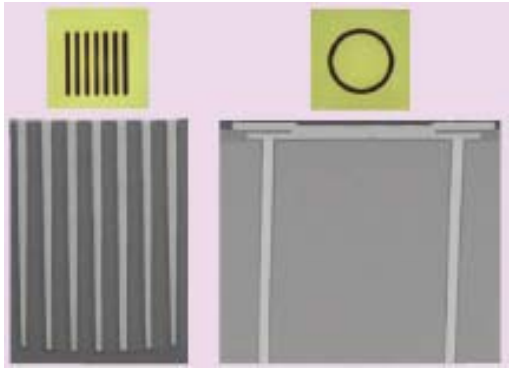
Through Package Vias

TSV and TPV: Complementary 3D Enablers

Through Silicon Via



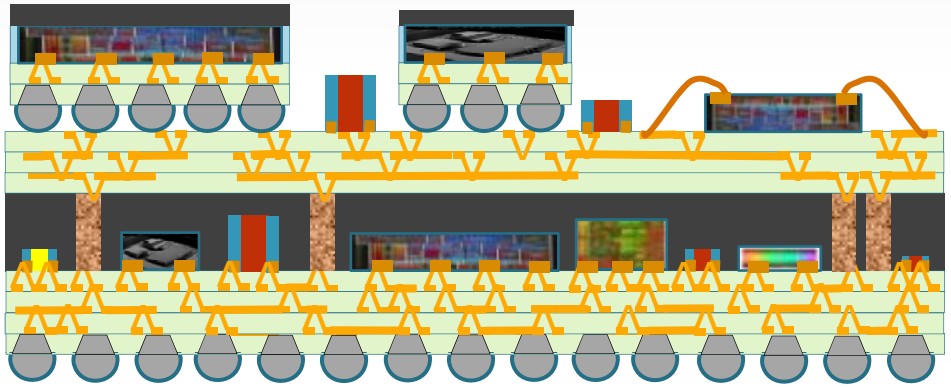
-EETimes

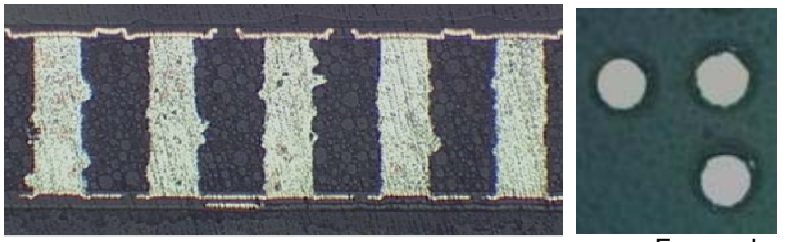


-P.S. Andry, et. al., IBM Journal of Research and Development

- Fine geometry possible (~10µm dia)
- High aspect ratio possible (>10:1)
- Low resistance possible (<50mΩ)
- Typical uses: 2.5D, 3D-die stacking, high I/O, high bandwidth

Through Package Via





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- Coarse geometry (~100-200µm dia)
- Lower aspect ratio (3:1 – 5:1)
- Low resistance typical (<50mΩ)
- Typical uses: 3D SiP, true heterogeneous integration

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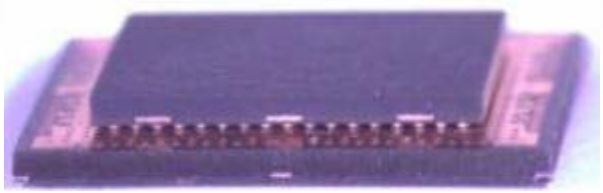
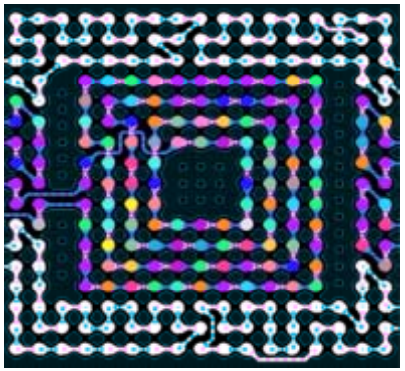
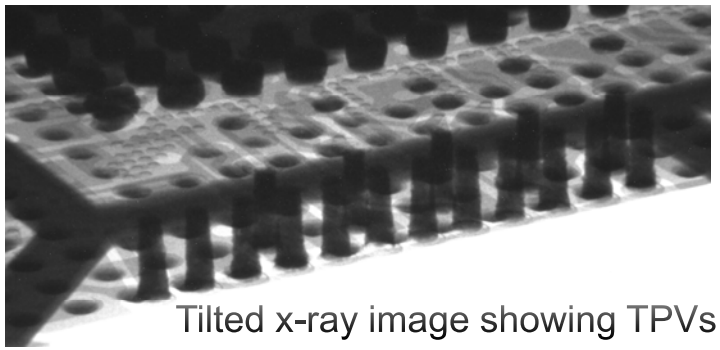
RCP TPV – Reliability Vehicle



3D RCP PoP TV



Test Loops on
3D RCP PoP TV



Tilted x-ray image showing TPVs

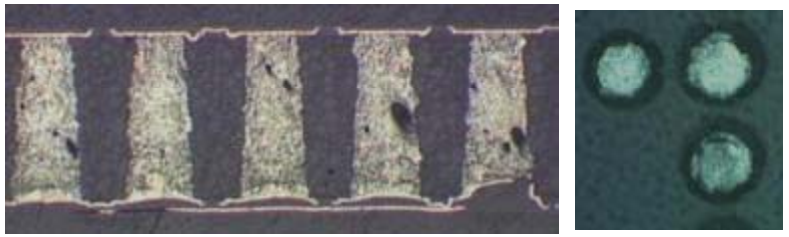
3D RCP PoP Test Vehicle

- Base Pkg: 12x12mm, P0.4mm, 2ML/1ML Double Sided RCP, TPV
- Top Pkg: 9x9mm, P0.5 mm, 2ML RCP

Reliability Plan

- Pre-con (MSL3/260C)
- AATC (-40 to 125C)
- uHAST

JEDEC: JESD22-A104
JEDEC: JESD22-A118



TPVs before optimization

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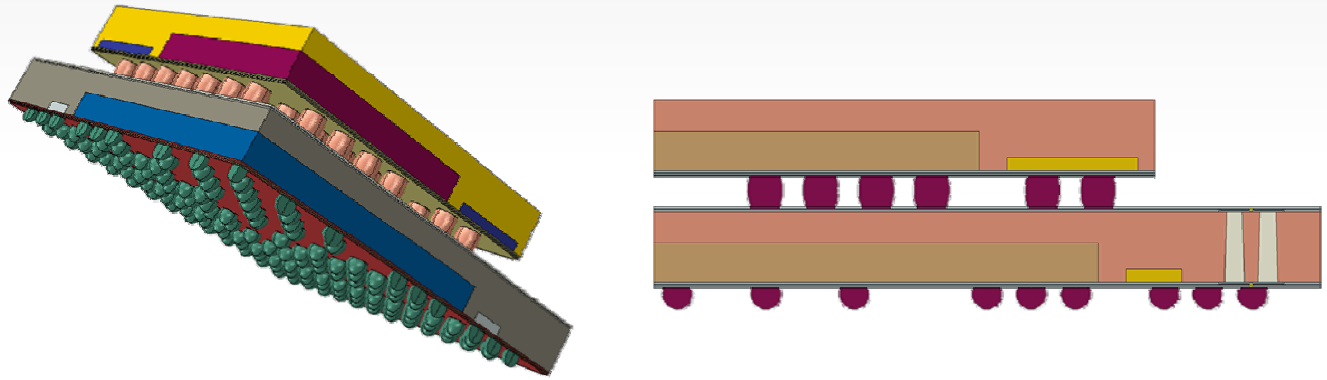
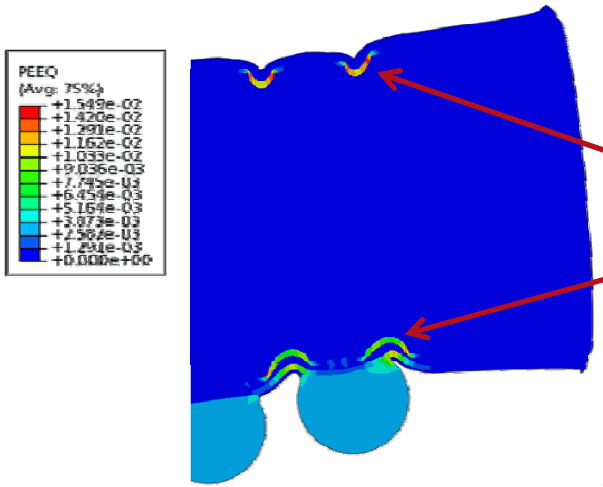
RCP TPV – Predictive Modeling



Quarter and cross sectional models used for simulation of thermomechanical behavior of through package via structures

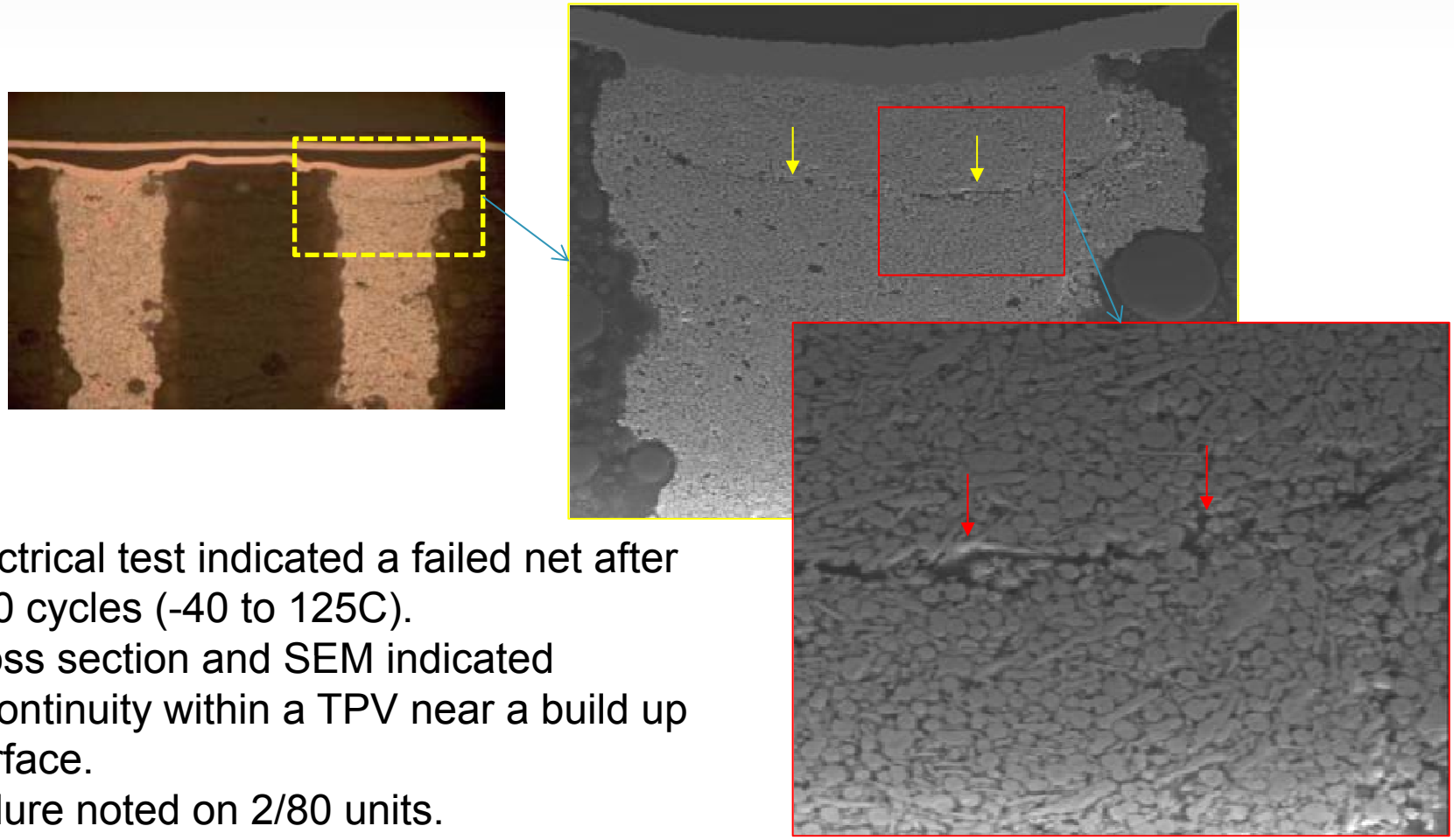


Simulated Effective Plastic Strain in RCP TPV resulting from AATC

Regions of elevated stress/strain resulting from simulated AATC.

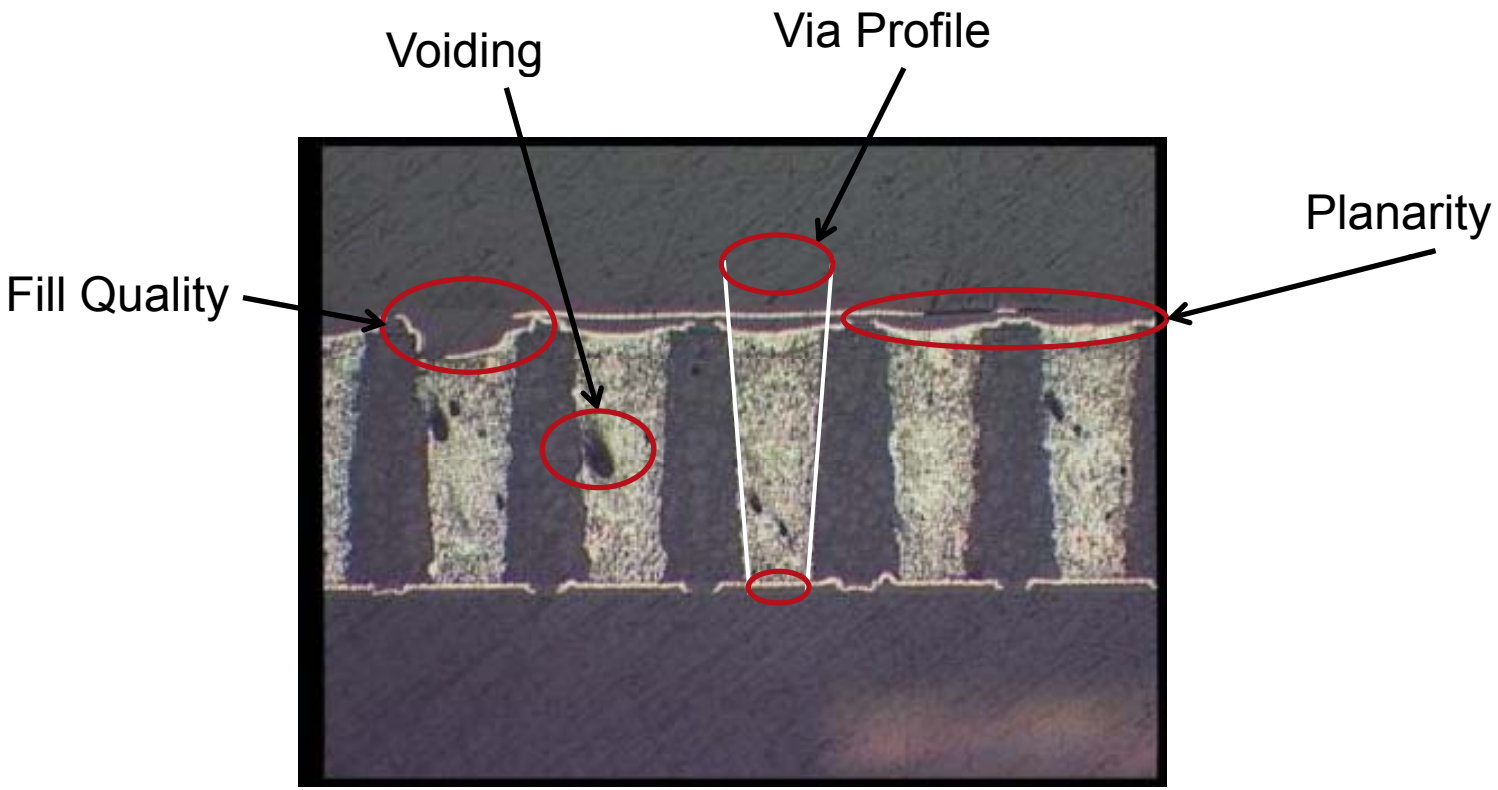
Potential areas of concern through temperature cycling.

RCP TPV – Reliability Findings



- Electrical test indicated a failed net after 1000 cycles (-40 to 125C).
- Cross section and SEM indicated discontinuity within a TPV near a build up interface.
- Failure noted on 2/80 units.
- Structural optimization continued.

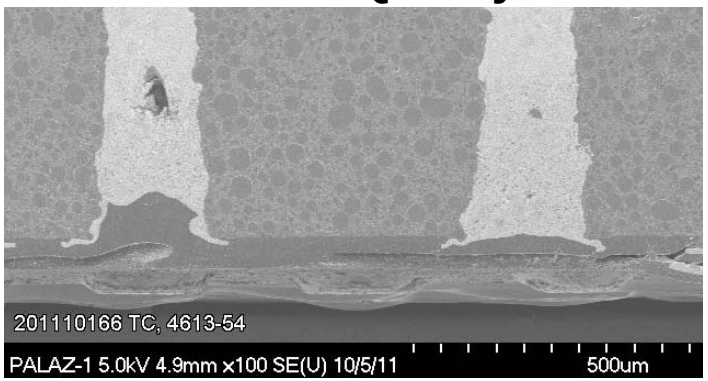
Through Package Via - Challenges



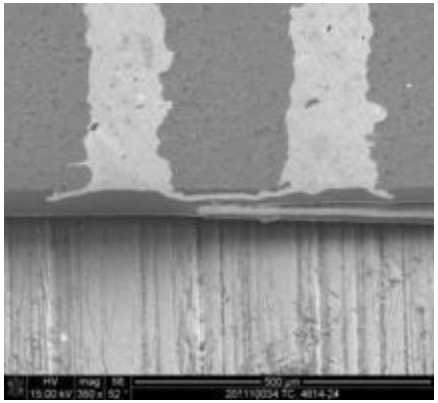
Pre-Optimization TPV

Through Package Via – Structure Optimization

Via Fill Quality

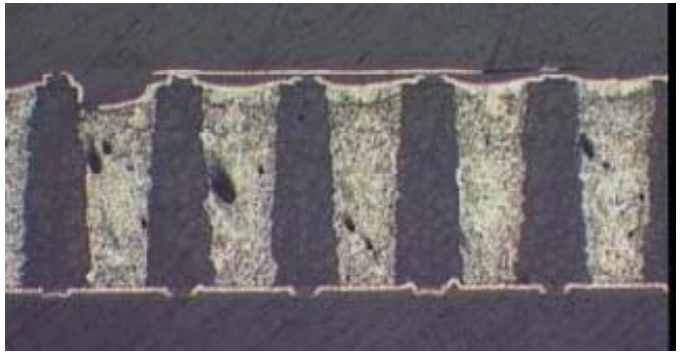


- Voiding
- Incomplete fill

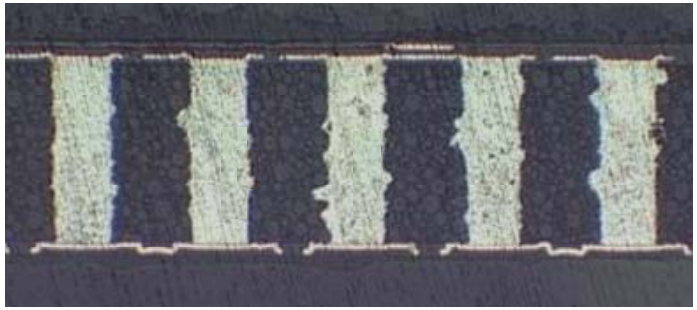


- Improved yields
- More reliable interface

Via Profile



- >50um difference via top to bottom
- Process implications, variance.

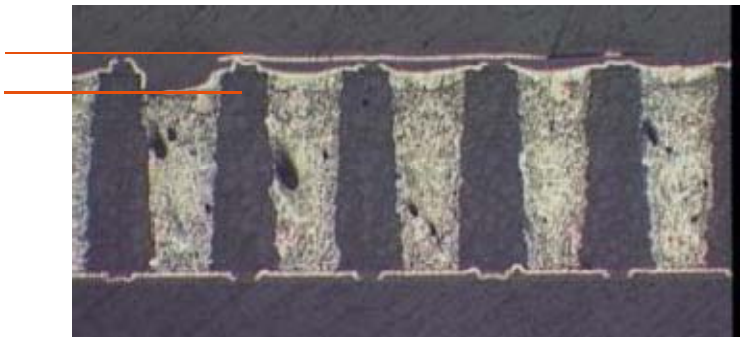


- <25um difference via top to bottom
- Improved yields, deviation.

RCP TPV – Structure Optimization

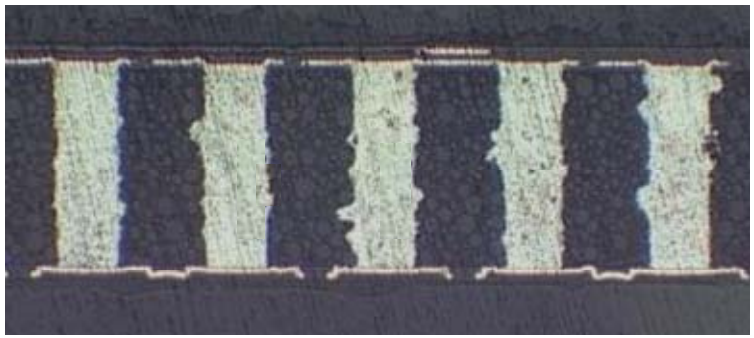
Via Planarity

Pre-Optimization



- >25um planarity typical, significant variance
- Yield, process, reliability

Post-Optimization



- ~4um planarity

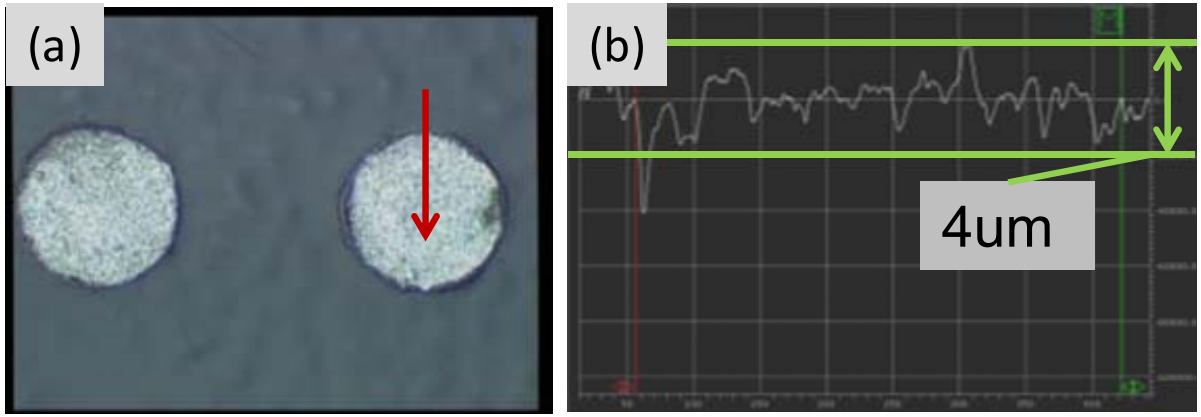
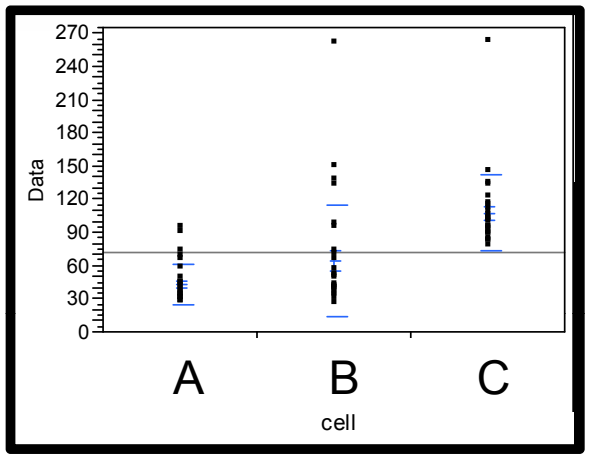


Figure. a) Top view of post-process TPV with direction of planarity measurement and (b) topography profile.

RCP TPV – Electrical Characterization

Time Zero

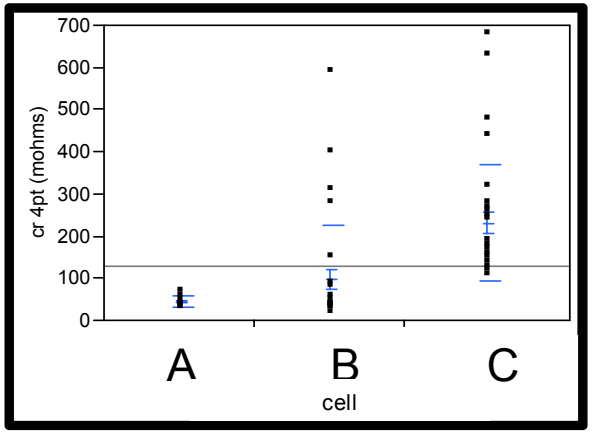


- R_m cell A (PoR) 42.8mΩ.
- N=30
- STD~18.1mΩ.

- No significant increase in TPV resistance.
- Each net contains 2 vias
- Typical TPV resistance <25mΩ.

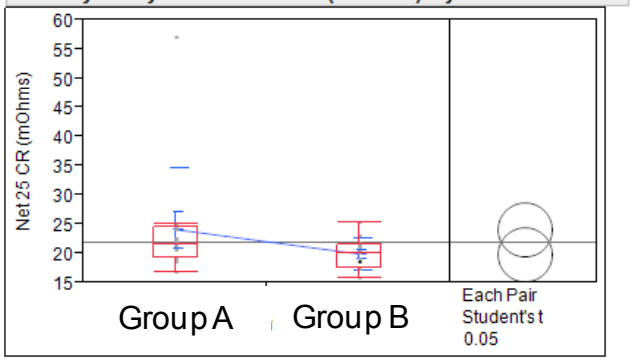
Post 2000 Cycles

(AATC -40 to 125C)



- R_m cell A (PoR) 44.3mΩ.
- N=30
- STD~12.8mΩ.

T0 R_m – Additional Optimization



Means and Std Deviations

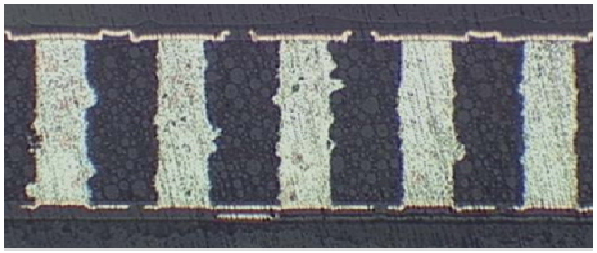
Level	Number	Mean	Std Dev	Std Err Mean	Lower 95%	Upper 95%
Center	12	24.1750	10.6467	3.0734	17.410	30.940
Edge	12	20.0083	2.7054	0.7810	18.289	21.727

- Further optimization of TPV structure shows average net resistances <25mΩ.

*Four point probe structure used for measurement

RCP TPV – Reliability Results Post-Optimization

- Optimized process yields 99.4%
- Optimized structure surviving AEC Grade 0 (2000AATC, -50°C to 150°C)



RCP 3D PoP – Reliability Results

AATC

Cell A (-40/125)	MSL3/260	250 cycles	500 cycles	1000 cycles	2000 cycles
Lots 6160, 6164, 6166	0/40	0/40	0/40	0/40	0/40

AATC

Cell B (-50/150)	MSL3/260	250 cycles	500 cycles	1000 cycles	2000 cycles
Lots 6160, 6164, 6166	0/40	0/40	0/40	0/40	0/40

uHAST

Cell C (uHAST,130C/85RH)	MSL3/260	96hrs	144hrs
Lots 6160, 6164, 6166	0/40	0/40	0/40

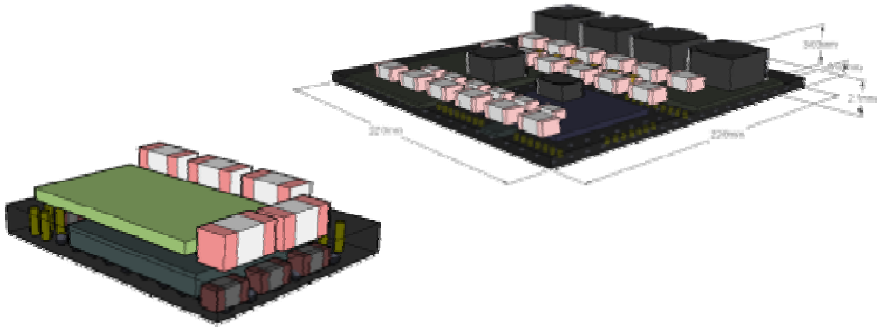
JEDEC: JESD22-A104
JEDEC: JESD22-A118

Summary

- 3D RCP with TPV structure demonstrated reliable passing:
  - MSL3 (260°C)
  - 144 hours uHAST (130°C, 85%R.H.)
  - 2000 cycles AATC (-40°C to 125°C)
  - 2000 cycles AATC (-50°C to 150°C) - AEC Grade 0

- Average measured TPV net resistance <25mΩ.

- RCP with TPVs enables SiP & 3D packaging solutions for:
  - ✓ Heterogeneous integration
  - ✓ System miniaturization
  - ✓ Enhanced system performance



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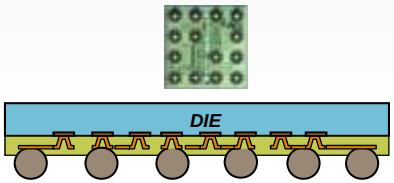
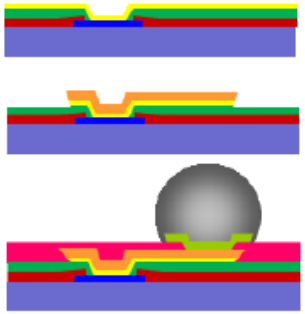
WLCSP vs. RCP

WLCSP

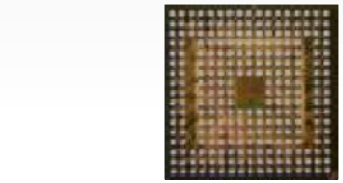


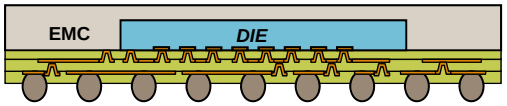
- Blind assembly directly on a wafer
- Pkg size = die size

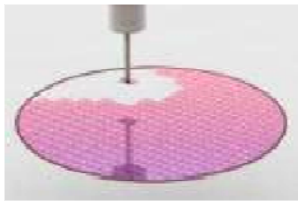


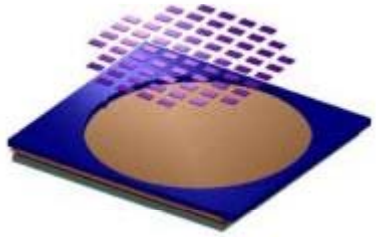
- Build up process based on bumping technology
- Single RDL (Redistribution Layer)
- Exposed back side and edge of die

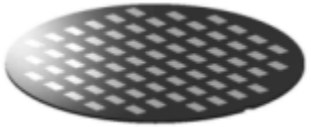
RCP











- Wafer reconstitution with KGD
- Space creation to accommodate more IOs and sophisticate routing

- Build up process with “Fan-out” routing
- Multiple RDLs (Redistribution Layer)
- Physical protection for die

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