CORNING

Glass Carrier Wafers for The Si Thinning Process for Stack IC Applications

Aric Shorey, Ph.D.
Sr. Technical Manager, Semiconductor Glass Wafers
Corning Specialty Materials

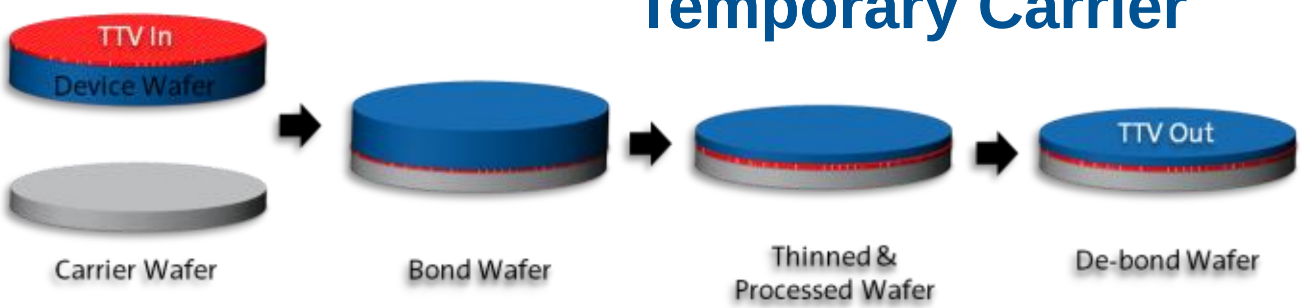
March 13, 2013

Agenda

- Why Glass?
- Glass Carrier Total Thickness Variation (TTV) and Warp
- Wafer Metrology
- Stack TTV
- Conclusion

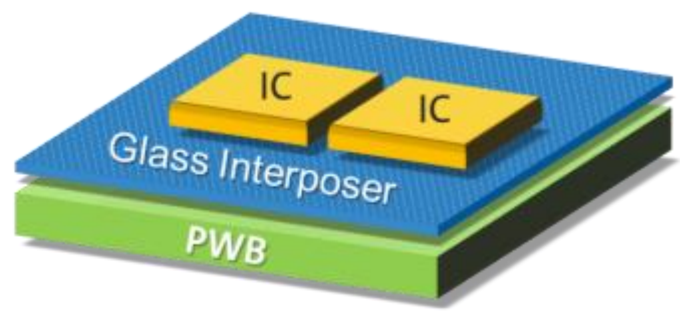
Roles Of Glass In Advanced Semiconductor Packaging

Temporary Carrier



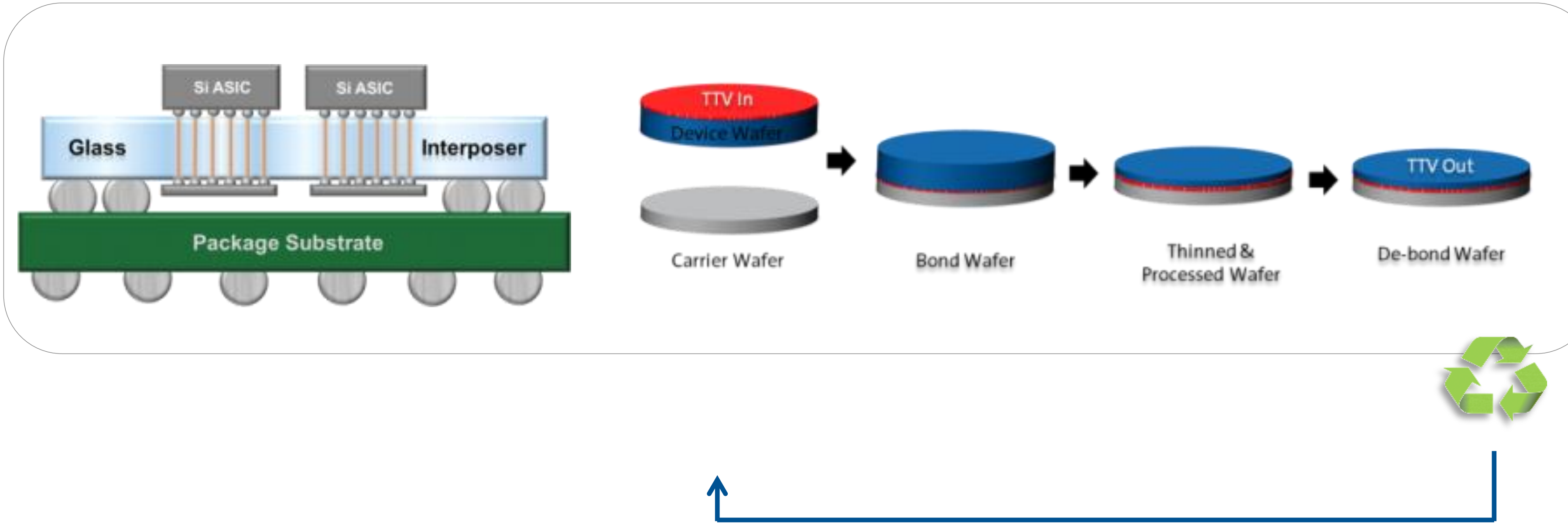
Integrated Carrier

Interposer



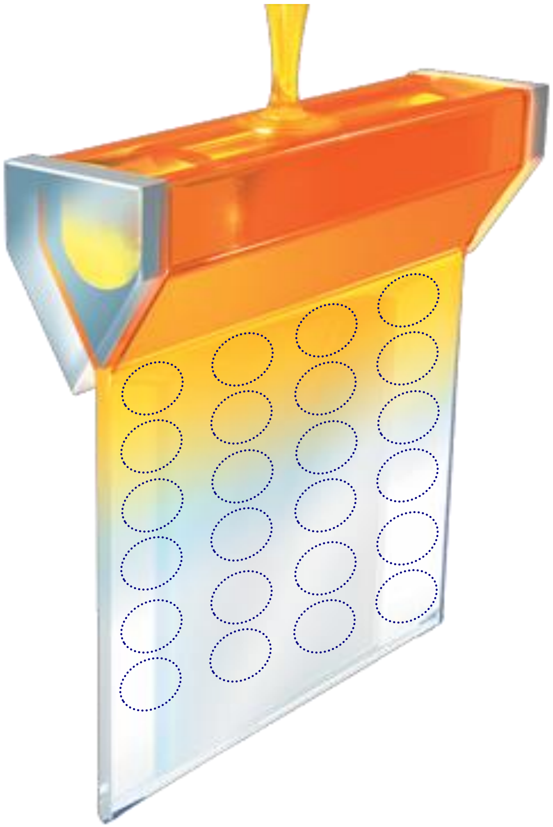
2.5D and 3D Integrated Packaging

Glass Carrier Wafers

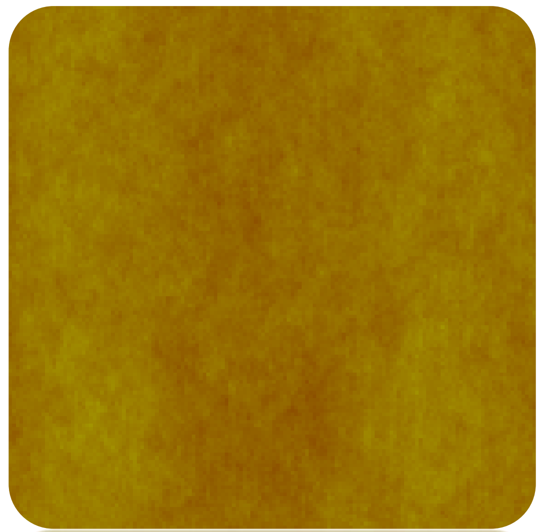


- Thinner, more functional and mobile devices require reduced chip thickness arranged in 2.5D (today) or 3D (tomorrow) arrays
- Carrier wafers required during thinning
- Corning fusion process provides ideal platform for manufacture of carrier wafers

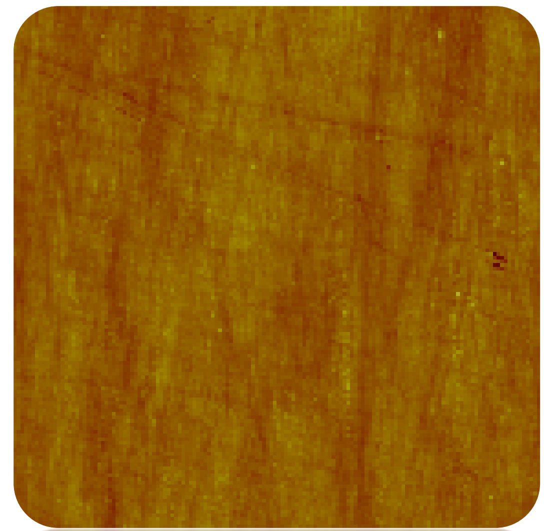
Corning's Fusion Platform Delivers A Pristine Surface With No Polishing Required



Corning fusion glass surface



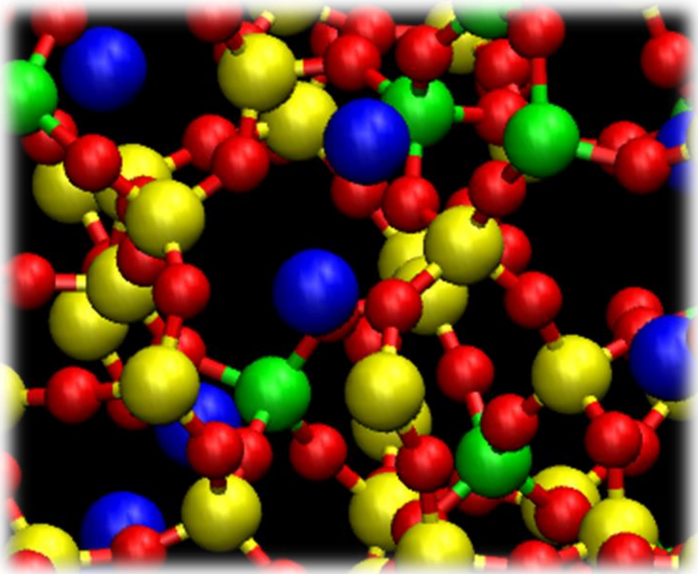
Polished glass surface



Roughness Measurement Results (AFM)

	Fusion	Lap & polished
RMS	0.3 nm	1.5 nm
Ra	0.2 nm	1.1 nm
Z-Range	4.2 nm	33.7 nm

The Aluminosilicate Glass System Affords Substantial Opportunity For Optimization Of Properties



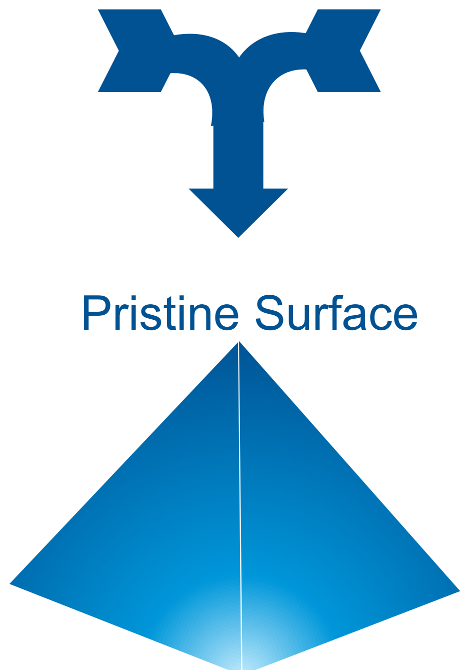
*Computer molecular model of an **aluminosilicate** glass*

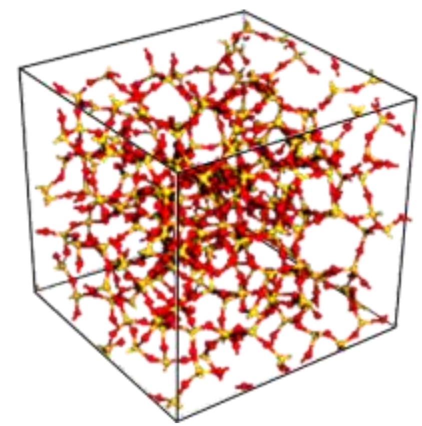
Properties Under Control By Glass Chemistry

- **Thermal Properties (Expansion)**
- Chemical Durability
- Mechanical Strength
- Surface Hardness
- Elastic Properties
- Optical Properties
- Electrical Properties

Corning's Strategic Intent in Semiconductor Glass

Advanced Optical Melting Fusion Sheet Forming Process **+** Innovative Aluminosilicate Glass Compositions





Pristine Surface

Optimized Expansion

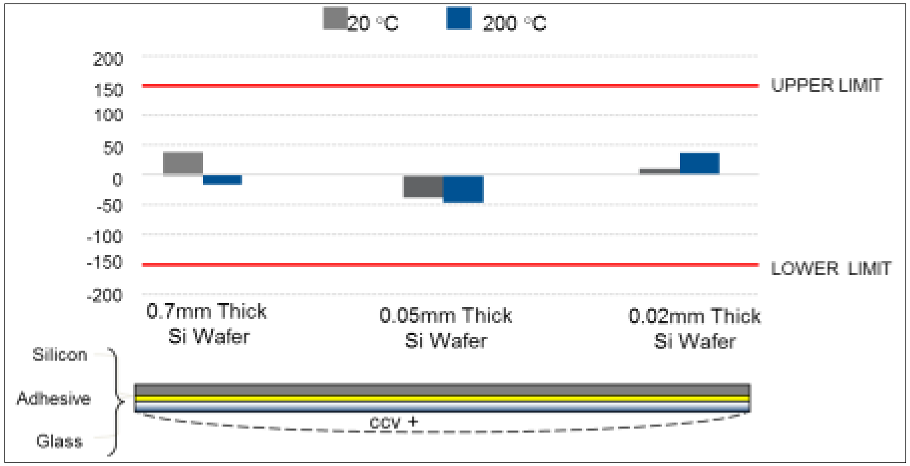
Profoundly Flat

Thin & Strong

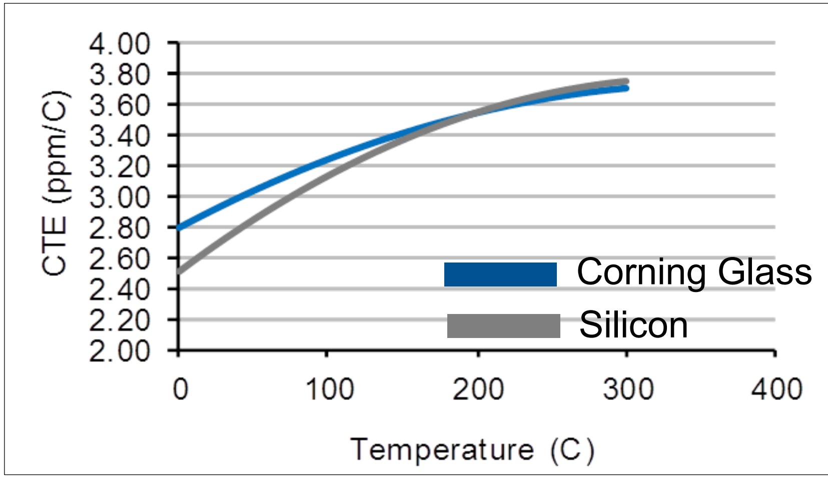
Wafer Bow During Thermal Process Is A Function Of Relative CTE Of Glass, Si And Adhesive

Coefficient Thermal Expansion (CTE) matched to silicon

Wafer Stack Bow vs. Si Thickness & Temperature



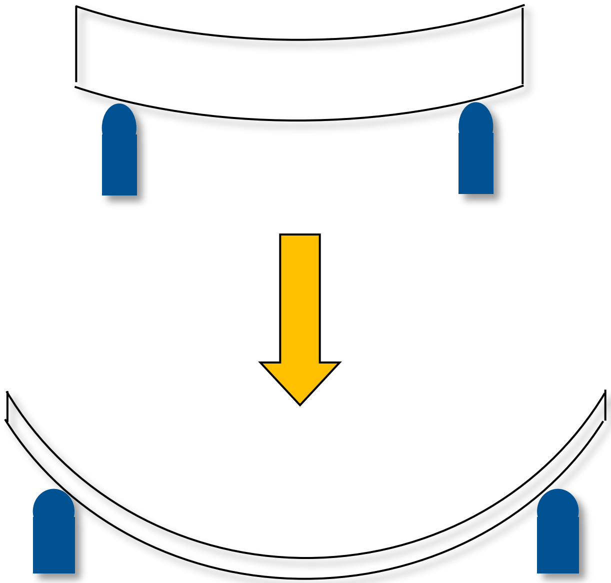
Instantaneous CTE vs. Temperature



- A target maximum BOW of 150µm during processing is achievable due to good expansion matching between the glass (SGW3) carrier and Silicon wafer
- For many next generation I/C designs, wafer thinning leads to an **increase** in total stack-up CTE, requiring a higher CTE carrier to match. (Corning SGW4, SGW8)

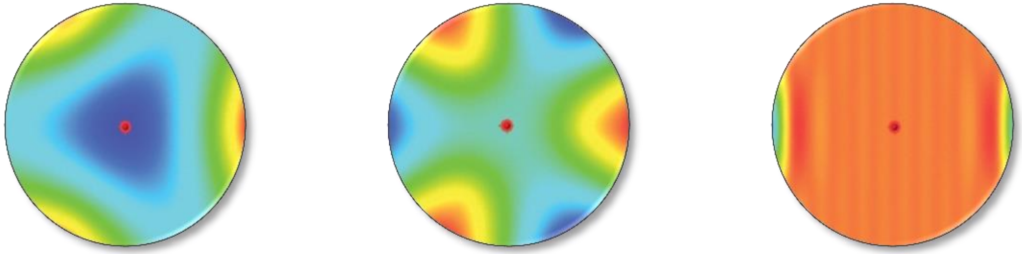
Motivation: Historical silicon methods do not easily transfer to large, thin wafers

- Metrology strategies have evolved from methods used to characterize smaller, lower aspect ratio geometries
- Large, thin wafers have inherently low stiffness, leading to large deflections
- Conventionally, three point mounts have been used to measure flatness/warp of wafer along with the gravity compensation
  - Calibration techniques
  - Multiple measurements (Side A/B)
- Large amounts of deflection from the mount makes compensation more challenging
- Corning's Flatmaster® MSP 300 provides new methods to overcome the shortfalls of traditional methods



Carrier Wafer Characterization: Deflection (um) from FEA

Deflection due to gravity *(prior to compensation)*

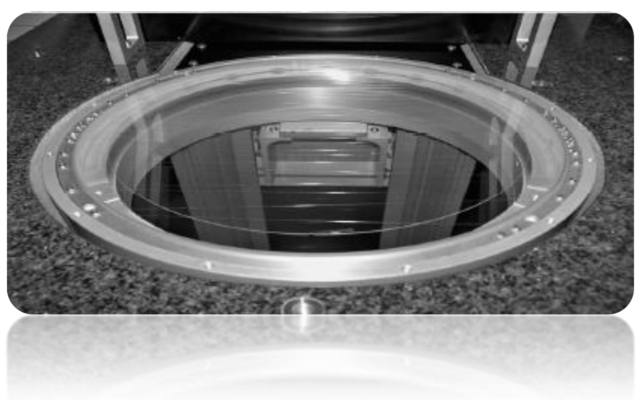


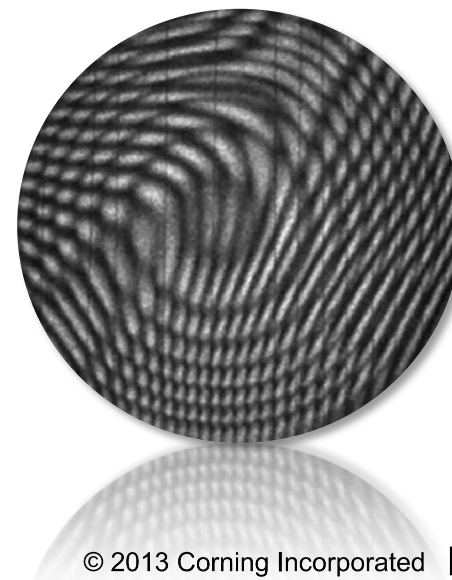
Material (thickness)	3-Pt. perimeter (0.7 mm)	3-Pt. 0.7 radius (0.7 mm)	Wire Support (0.7 mm)
Si	217	61	0.6
SGW3	422	121	0.6

- Techniques that use calculation/calibration to remove gravity effects assume many consistencies which may affect data (material, thickness etc.)
- Wire support minimizes gravity effects, which eliminates this complication

How Precision Glass Carriers Are Measured MATTERS

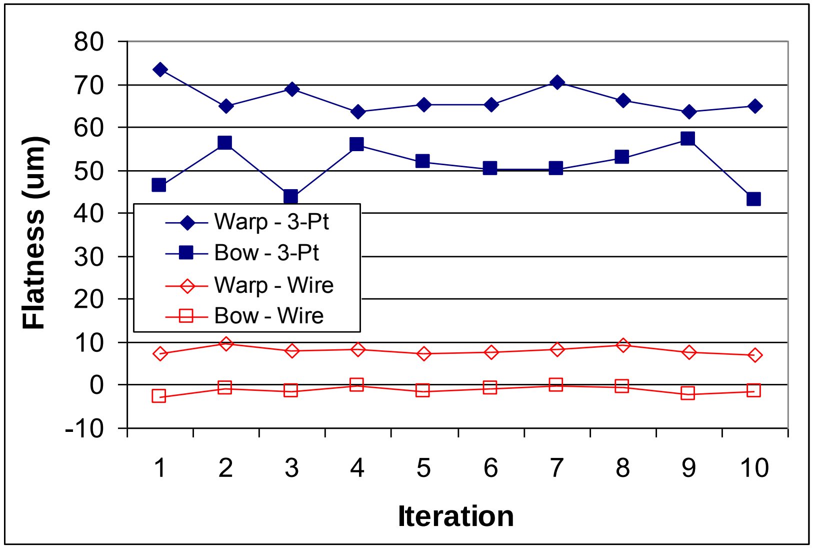
- Frequency stepping interferometer avoids limitations of standard phase measuring interferometers or point-by-point scan based techniques
- Simultaneously measure flatness, TTV and absolute thickness (<1minute/wafer)
- Full aperture interferometric approach gives sub-millimeter lateral resolution (~3,000,000 data points /300 mm wafer!)
  - Z-Resolution of 10 nm (0.40 µinch)

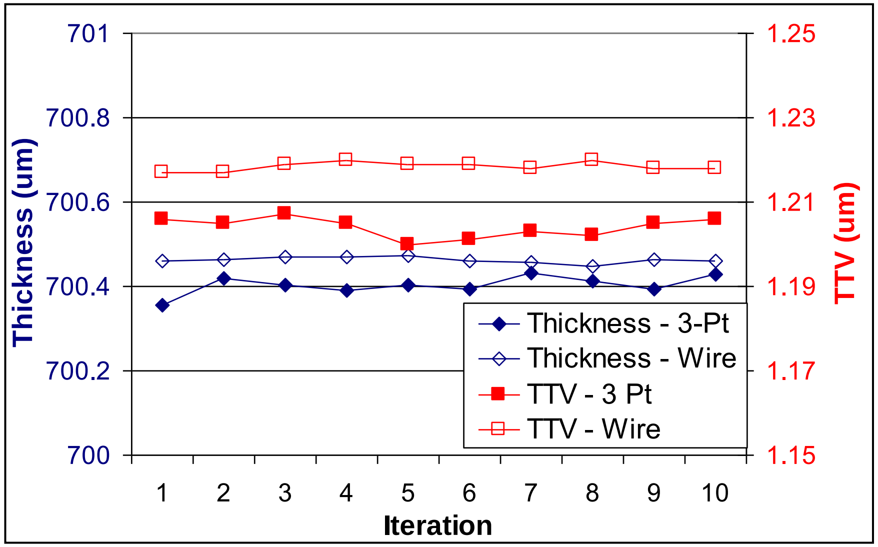




Consistency Of 3-Point & Wire Support

Evaluate Repeatability From Mount Techniques On MSP





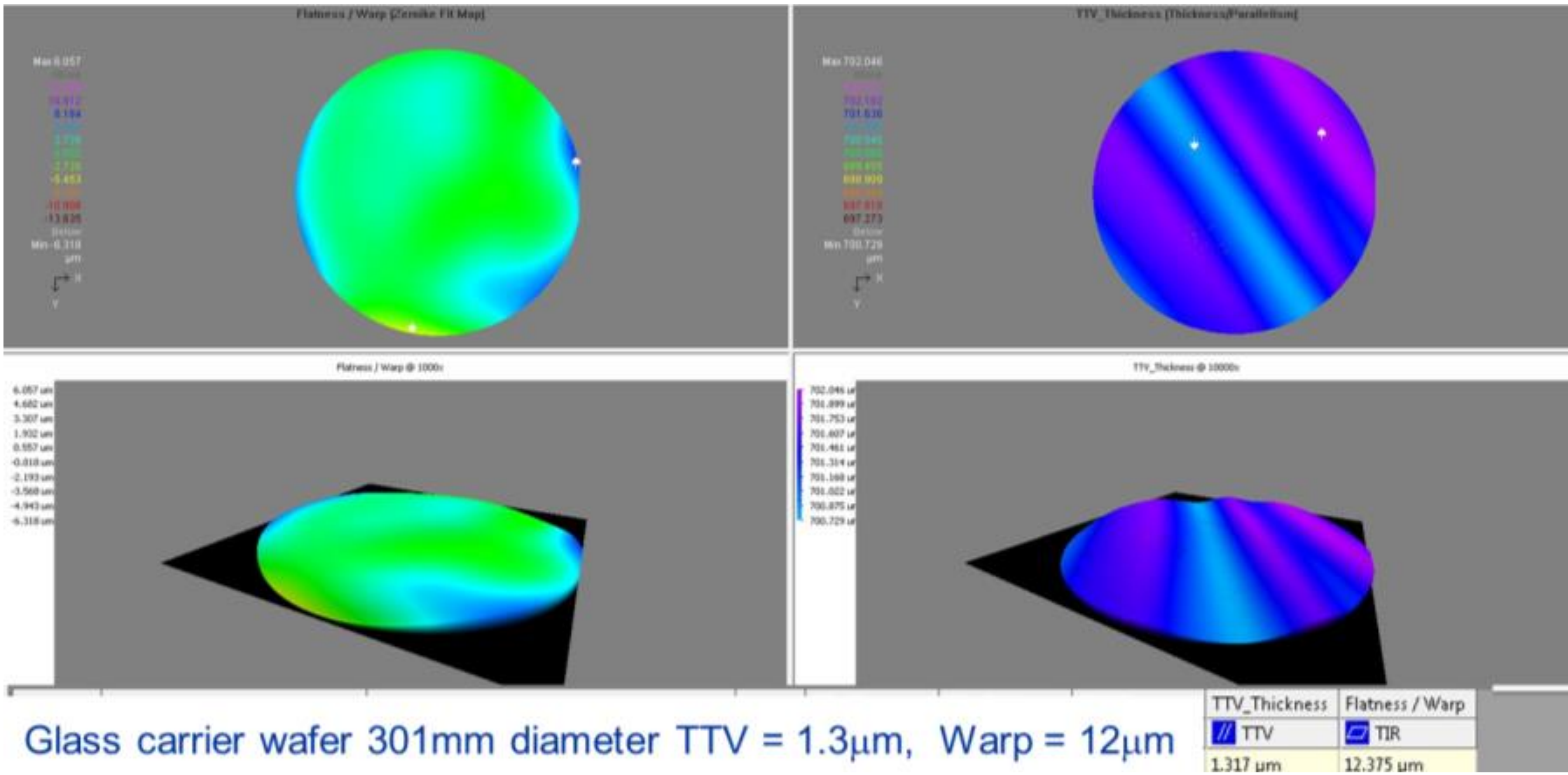
200 mm diameter glass wafers

- Measure same part 10x with 2 mount techniques (3-point at 0.7R, wire support)
- 3-point support creates larger warp and standard deviations compared to the wire support
  - 10 μm variation with 3-point for the same part
  - Compensations strategies do not account for this error
- Wire support method gives thickness repeatability better than 0.03 μm & TTV repeatability < 0.003 μm.

TTV and Warp Attributes
With NO POLISHING - Champion Grade (< 2.0µm TTV)

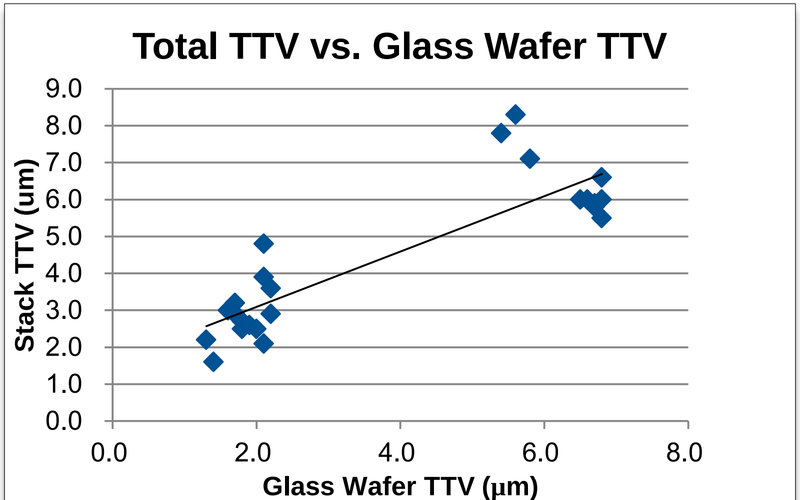
Lot results – 50 wafers
Avg TTV = 1.4 µm, Std deviation = 0.2 µm
Avg Warp = 17 µm, Std deviation = 5 µm

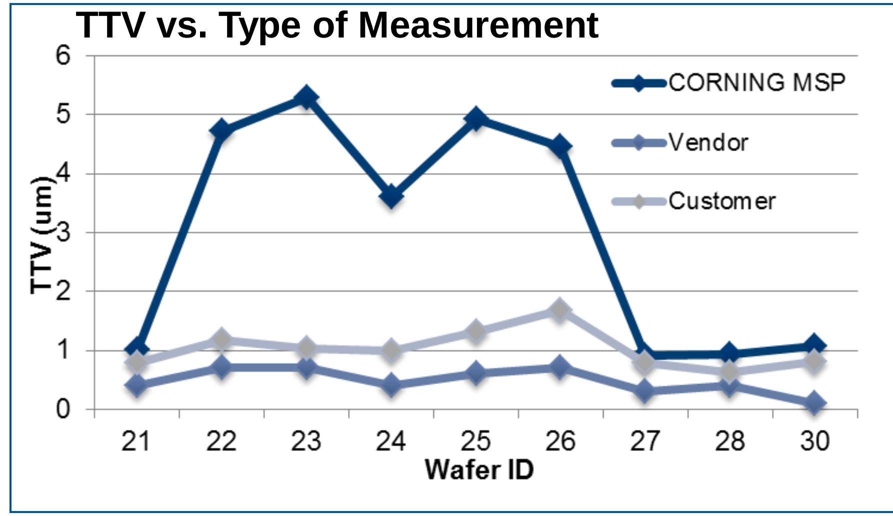
Measured on Flatmaster® MSP-300



Glass TTV and Wafer Stack TTV

Data taken using 3M WSS process

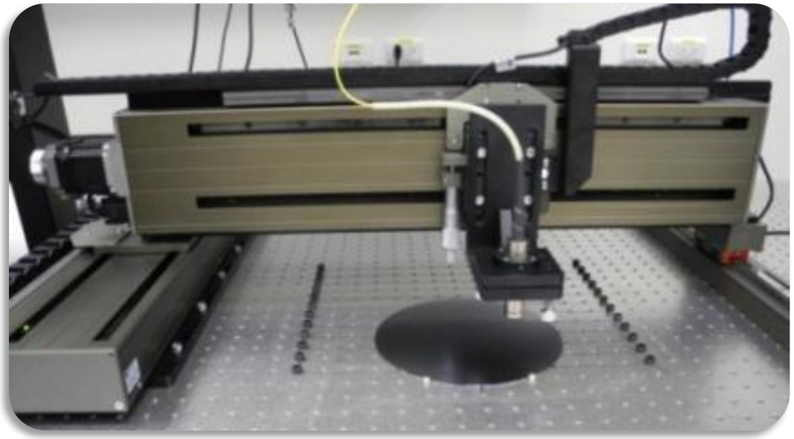




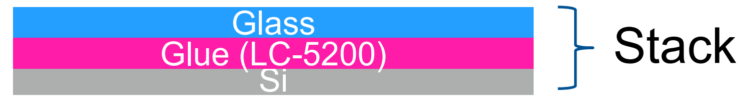
- Corning wafers (SGW3) of specified TTV (“low” and “high”) used with 3M WSS to study effect of wafer TTV on bonded stack TTV
  - Data is highly correlated (i.e. low glass TTV gives low wafer stack TTV)

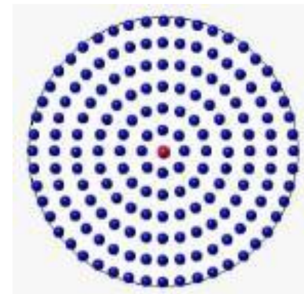
- Glass wafers from another established wafer supplier reporting TTV < 1 µm as based on only 5 measurements/wafer
  - Actual thickness variation as measured by MSP, was much greater than 1 µm, which can clearly impact bonded stack TTV

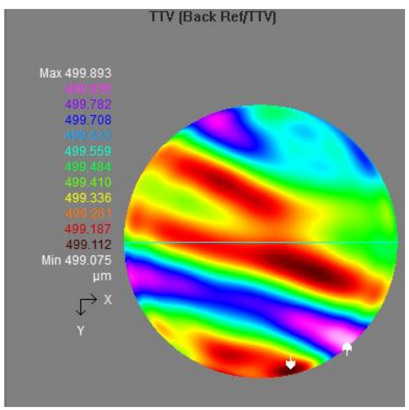
TTV characterization of each layer of a bonded stack



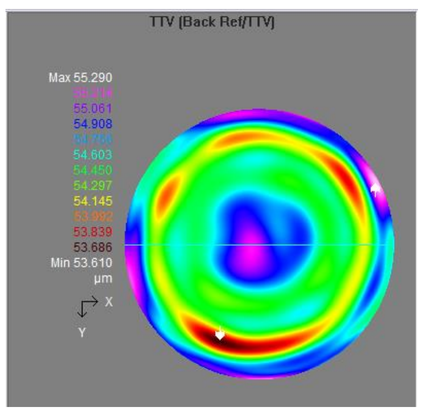
LCI scanning system developed in Corning Advanced Technology Center (CATC)



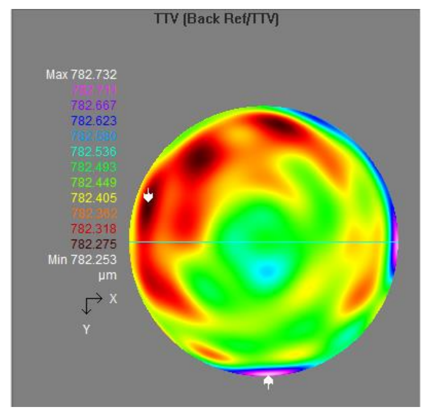




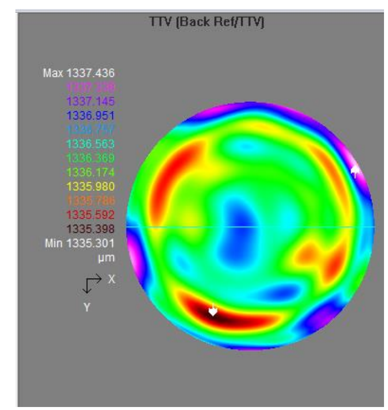
Glass



Adhesive



Silicon

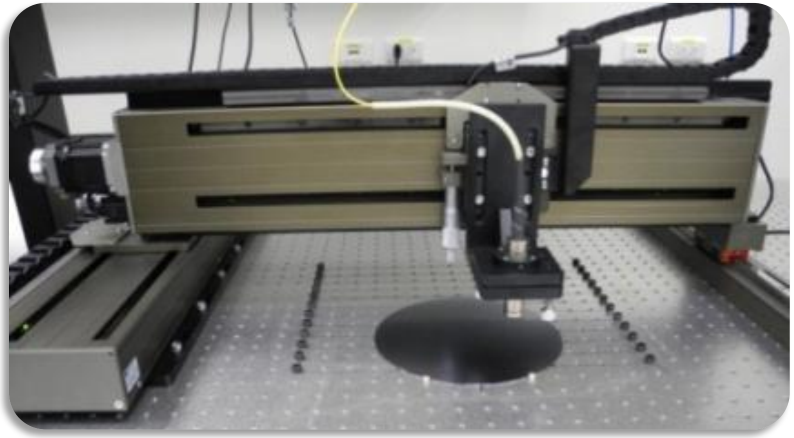


Stack

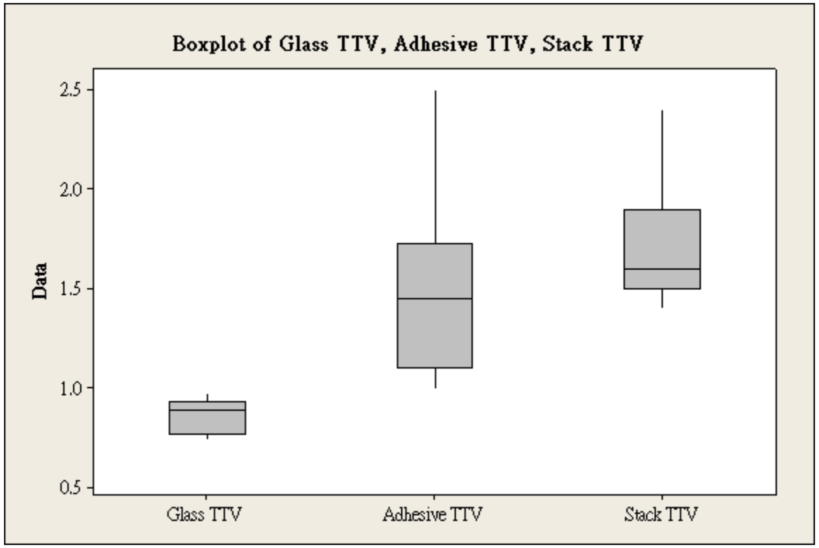
TTV Map Analysis

- Work with 3M WSS to demonstrate low stack TTV given by low carrier TTV
- TTV of all glass samples tightly distributed at < 1um TTV
- Stack TTV between 1.5 and 2 um demonstrated repeatability
- Stack TTV appears primarily driven by adhesive TTV

- Work continues in this area to understand how to best minimize Stack TTV

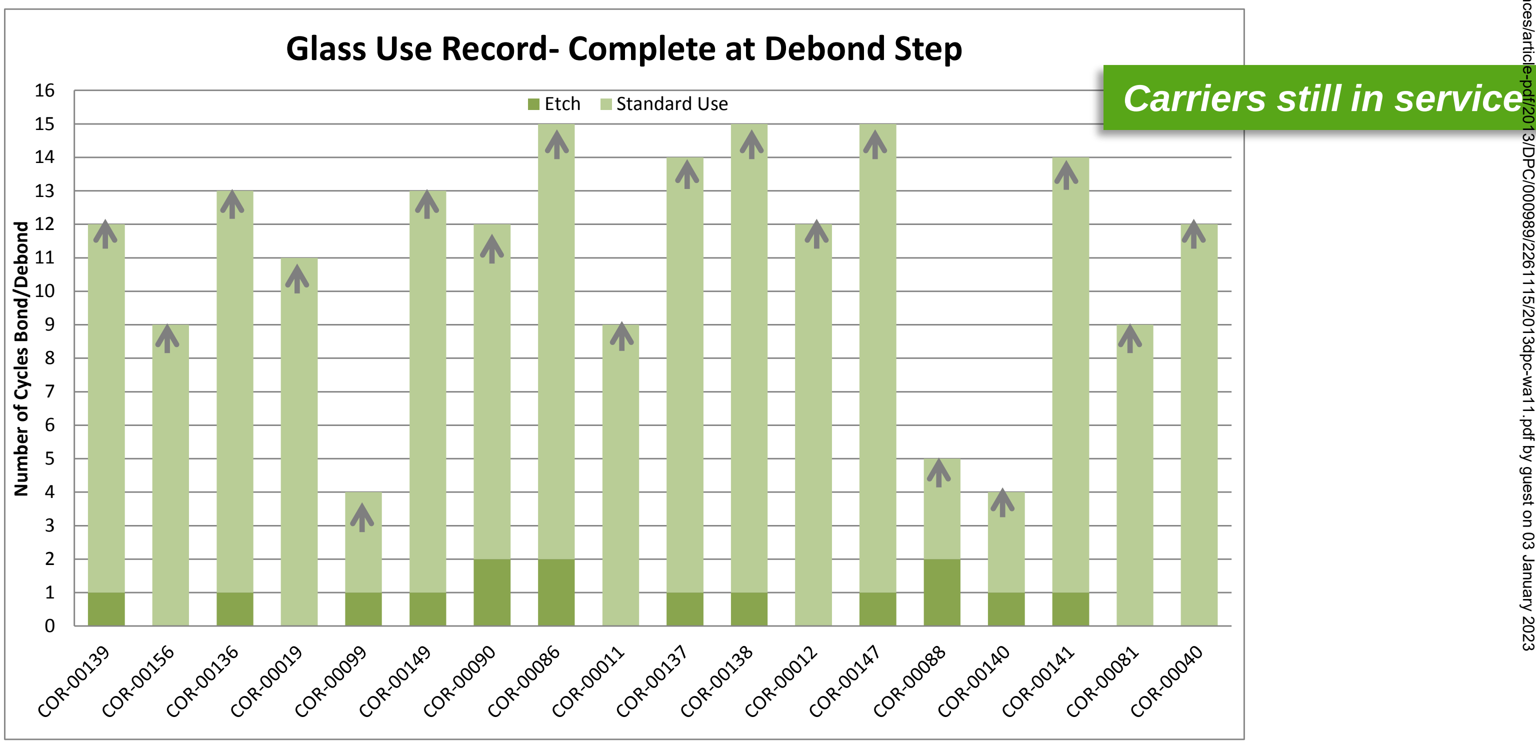


LCI scanning system developed in Corning Advanced Technology Center (CATC)



Corning Carrier Glass Recycling

- Corning has provided thousands of glass wafers of varying CTE related compositions to the industry featuring the same bond/debond process
- The primary factor controlling the number of carrier recycles is the cleaning process used to remove FAB specific contaminants (metals, oxides, particles, stains)
  - Must maintain carrier critical attributes (TTV, warp, durability)



Summary

- Glass is a versatile and robust material that with attributes well-suited for carrier applications
- Corning's capabilities in flat glass in aluminosilicate family and the fusion process in particular provide excellent foundation for the development of glass carriers
  - Low Total Thickness Variation, low warp/bow - < 1 um TTV demonstrated without polishing
  - There is opportunity to adjust glass composition to tailor properties/attributes such as CTE
  - Good mechanical strength, chemical durability
  - Scalability and adjustability of wafer diameter, process scalable for HVM
  - Transparency (inspection of bond layer, bond/de-bond processes)
  - Ability to Recycle
- Metrology is important: How the wafer is characterized (mount strategy, number of data points) is important to predict functional performance
- Ability to leverage attributes of fusion glass for high quality, low TTV glass carrier wafers to produce low TTV bonded stacks has been demonstrated.

Thank You!

CORNING