From WLCSP to smart interposers

Yann Lamy, program manager at CEA LETI

Yann.lamy@cea.fr

O. El Bouayadi, C. Ferrandon, L. Dussopt, C. Dehos, A. Siligaris, P. Vincent, A. Jouve

CEA, LETI, Campus MINATEC, 17 rue des Martyrs, 38054 Grenoble Cedex 9, France

S. Joblot, STMicroelectronics, 850 rue Jean Monnet, 38926 Crolles Cedex, France

T. Lacrevaz, C. Bermond, B. Fléchet, IMEP-LAHC, UMR CNRS 5130, Université de Savoie, 73376 Le Bourget-le-Lac Cedex, France

About CEA-LETI

MINATEC®

At the heart of Minatec campus, dedicated to Micro and Nanotechnology

- 1500 people working on Silicon technology with industrial partners
- ~ 80 people working on 3D IC and 3D Packaging
- Full 200mm & 300mm 3D capabilities

Outline

- Introduction: from WLCSP to smart interposers
- Mmw interposer description and characterization
- Conclusions and perspectives

Today electronic devices challenges

Data servers

High performance computing

Dense integration

Power reduction

Wireless

Low power

Low cost

Mobile & smart devices

…translating in new technology requests

Data servers

High bandwidth

Good yield

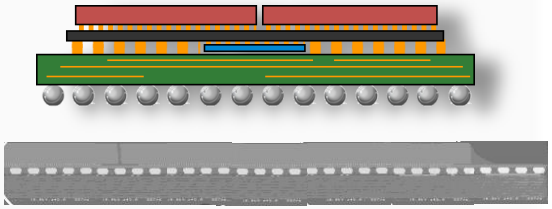
Thermal management

Low loss RF RDL & interco

Low cost process

More wires…

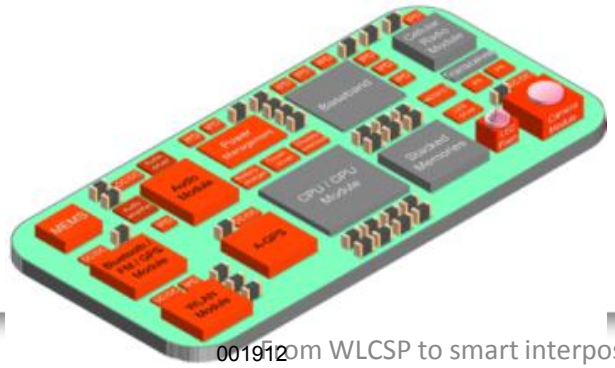
Multichip Interposer



Increase interconnect density

More than wires…

Mobile & smart devices

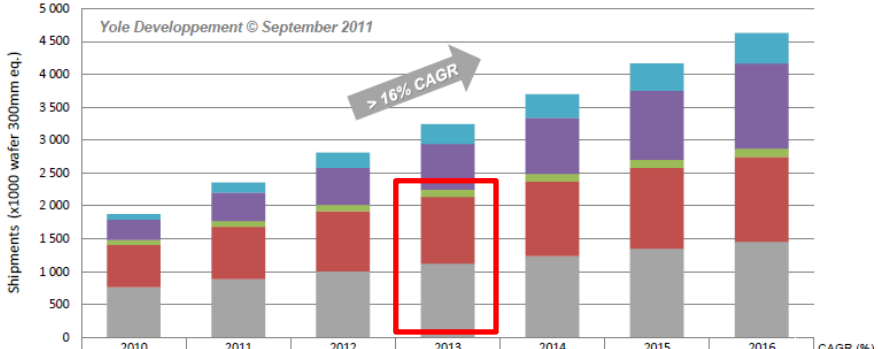


More functionalities directly reported on board

A steady increasing demand in WLCSP

WLCSP wafer forecast

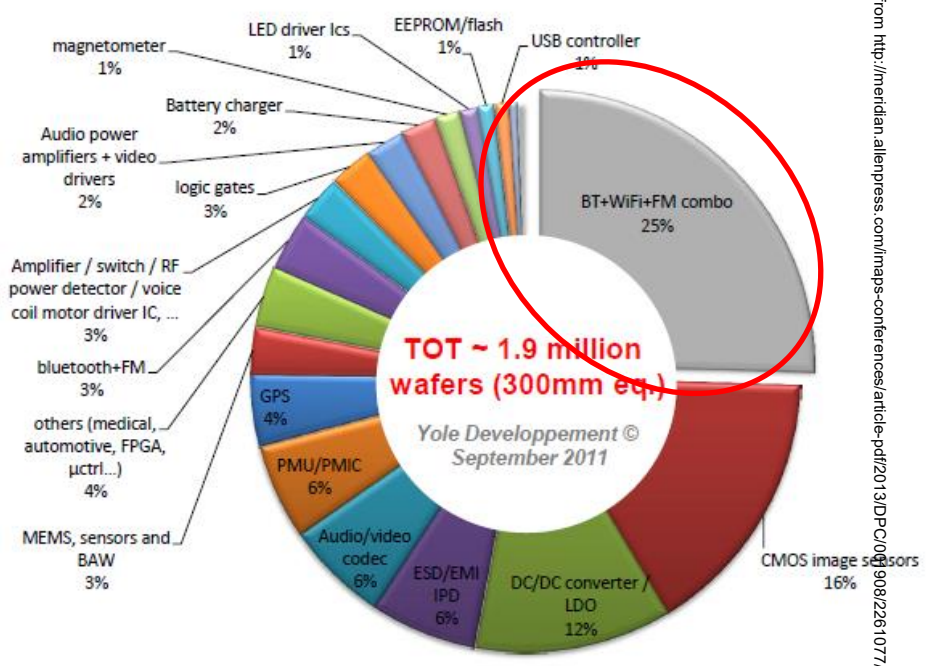
by device categories (12'' eq wspy x1000)



	2010	2011	2012	2013	2014	2015	2016	CAGR (%)
MEMS and sensors	82	152	232	303	359	417	464	33.5
CMOS image sensors	310	431	564	694	854	1 050	1 292	26.8
Misc. Logic and memory	72	86	96	106	115	123	130	10.2
Wireless Connectivity	644	798	913	1 018	1 136	1 223	1 287	12.2
Analog and Mixed Signal	765	887	1 007	1 122	1 236	1 353	1 457	11.3
total	1,874	2,354	2,812	3,243	3,700	4,168	4,630	16.2

2010 WLCSP produced wafers by device type

(x 1000 wafers 12'' eq.)



Courtesy of Yole

- Wafer Level Chip Scale Packaging (WLCSP) is following a tremendous increase
- Driven by RF (25%) and CMOS image sensors (16%) devices
- Clear trend of devices « combo » packaging

From WLCSP to smart interposer

TODAY

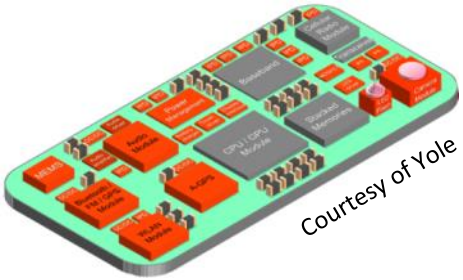
WLSCP

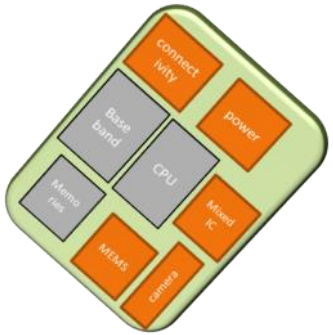
- Cost (reducing BOM)
- Size reduction
- Performances

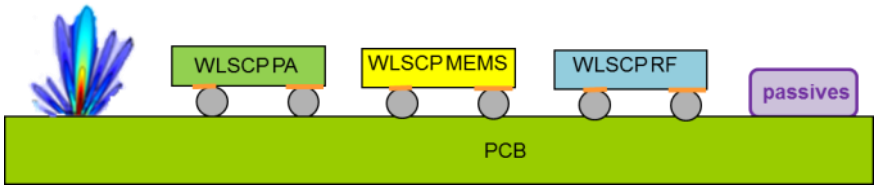
Silicon package

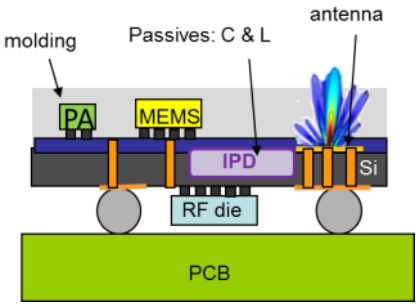
modules in SiP + IPDs
No extra BGA

Many individual components & passives









Why Si interposer for RF applications ?

- Miniaturization (high density)
- Antenna integration
- Improved signal integrity (shorter distances)
- High passives performances integration
- Increase reliability
- Possible baseband integration

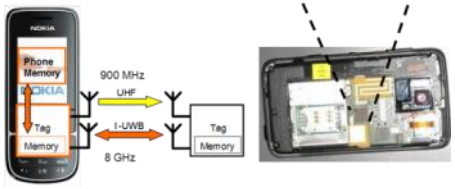
2,4 GHz

Wifi, 3G, LTE, PA size reduction

Courtesy of IPDIA

8-10 GHz

UWB



60 GHz

WiHD, WiGiG 1-7 Gbps

Smart interposer: the high data rate wireless case

- *Non licenced band exploitation* [57-66 GHz]

→ Available bandwidth: **9 GHz** (against 83,5 MHz at 2,4GHz)
→ Data rate : until **7 Gb/s** (standard WiGig)
→ 60 GHz → λ/2 = 2,5mm → antenna integration

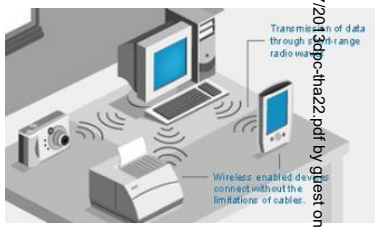
© WiGig Alliance, 2010

- Consumers applications → final cost limitation

→ CMOS technology for transceiver
→ Low cost and miniaturized silicon wafer level packaging

- Integration / Miniaturization

→ Heterogeneous integration functions: RF, MEMS, logic,…
→ Modules vertical stacking integration: 3D in high resistivity silicon



mmW interposer concept & challenges

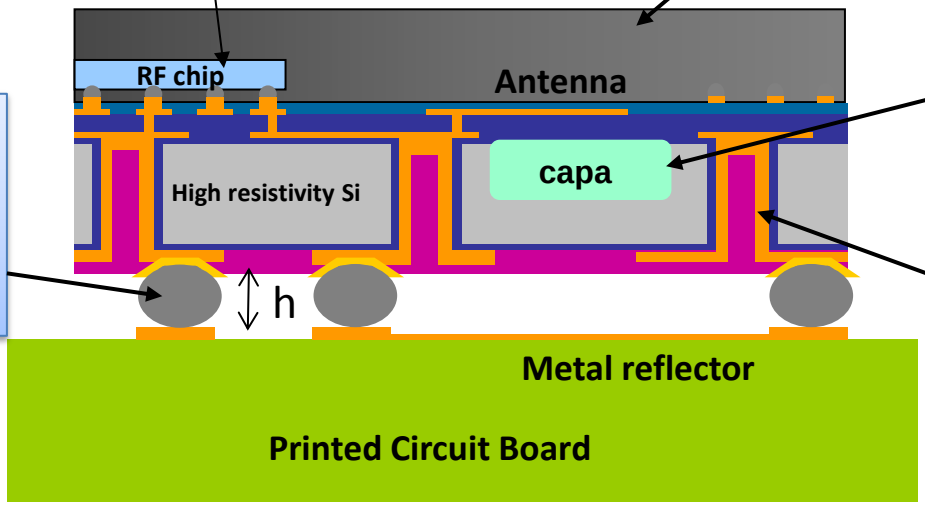
Heterogenous dies sourcing and I/Os

Wafer level passivation / biocompatibility

Compliant and reliable fine pitch 2nd level interconnect and stand off

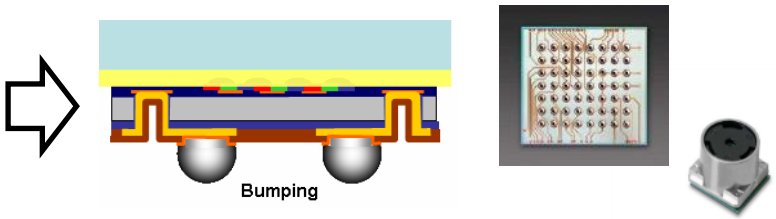
Integrated passives

Low cost TSV



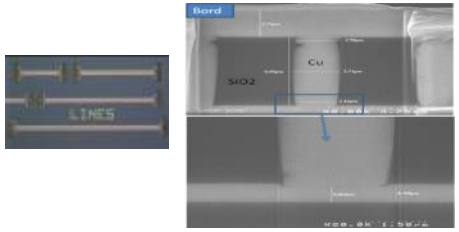
Re-use of TSV from image sensors

…and low cost

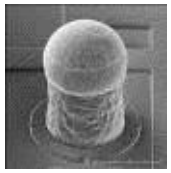


mmW interposer interconnection modules

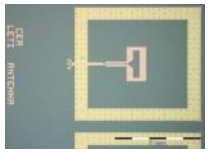
2 low loss routing level



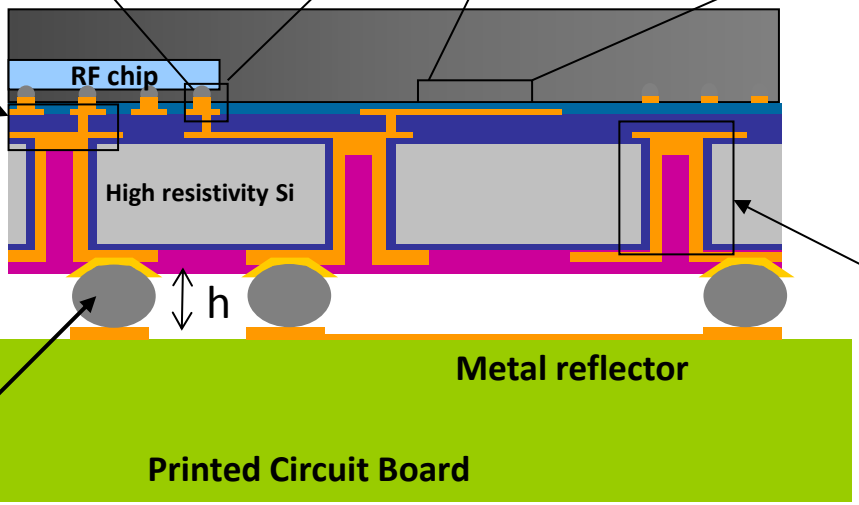
CPW and µstrip



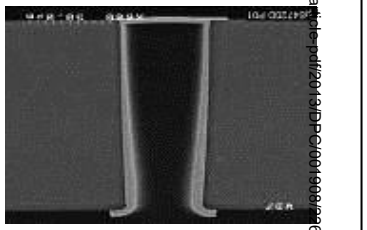
Cu pillars + RF die flip-chip



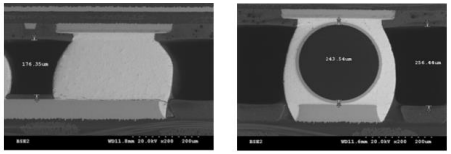
60 GHz integrated antenna



Through-Silicon-vis vertical connections (TSV)



Reliable blling to PCB



- All individual modules mature and ready
- Next step: integration in a functional mmW demonstrator

Outline

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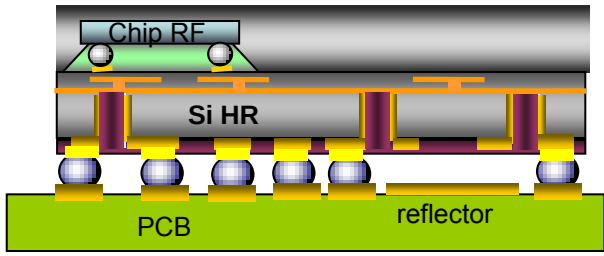
- Mmw interposer description and characterization
- Conclusions and perspectives

mmW interposer layout

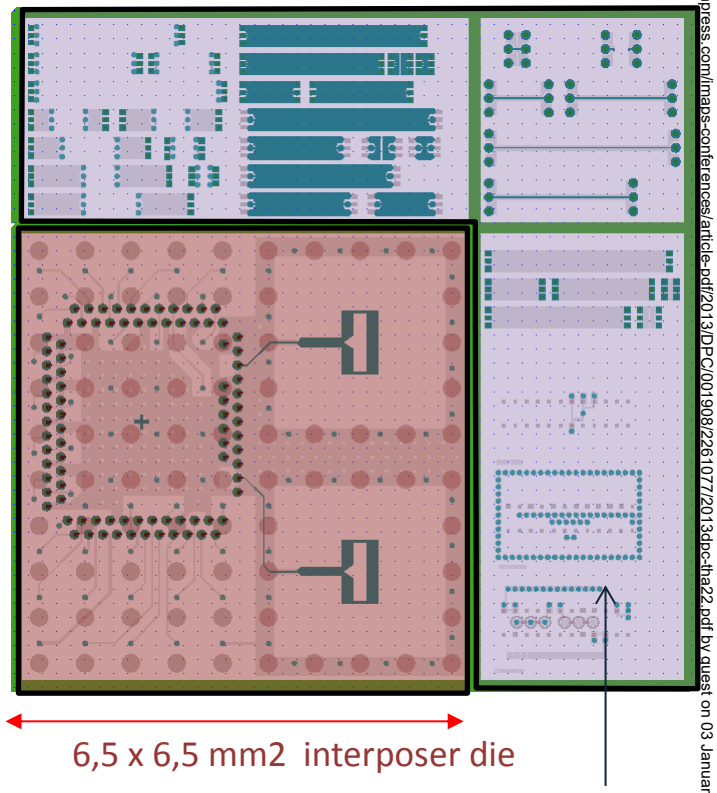
60GHz Si interposer demonstrator description



- High resistivity silicon wafers> 1kOhms.cm
- LETI MEMS 200mm line
- CMOS 65nm transceiver die
- One functional interposer die:
  - 2 x 60GHz antenna (Rx and Tx)
  - 81 I/Os (46 effective), 650µm pitch
  - TSV antenna shileding Faraday cage
  - line/space front side: 9µm / 9µm

  ➔ **Ultra compact design: 6.5 x 6.5 mm2**

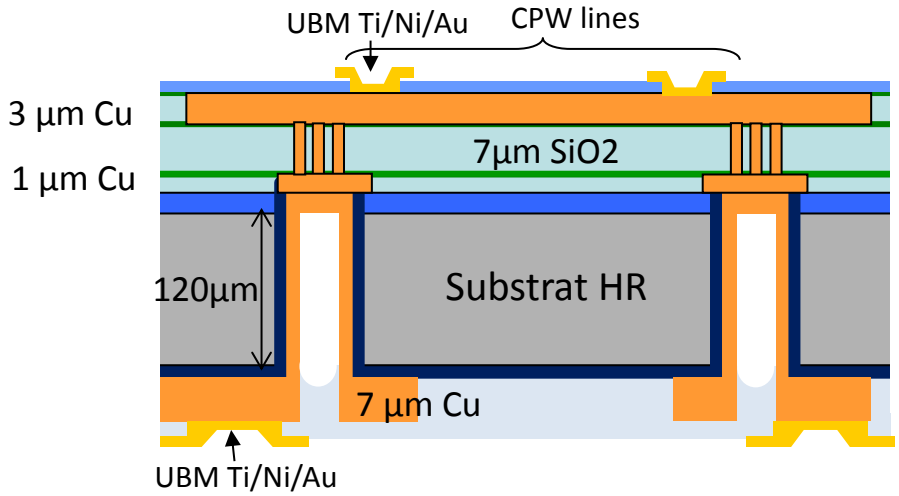
- Several DC and RF tests structures
  - Process qualification
  - Material electrical characterization(ε_{eff}, tan δ)
    - ❑ Silicon substrate
    - ❑ Passivation layer



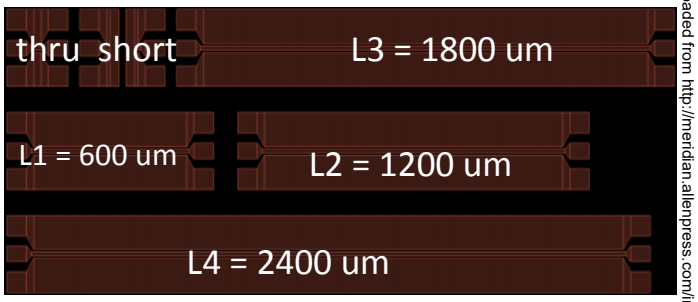
mmW interposer technology

Technological description

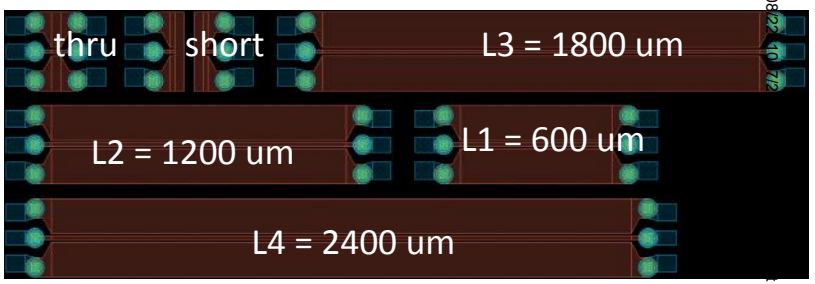
- Three level of metalization: M0, M1 et M2
  - Level interoconnections by TSv and micro vias
- Specific double thick Cu Damascene RDL designed for 60GHz
- Partial TSV filling
- Passivation and UBM metallization on both sides



Front side CPW 50Ω



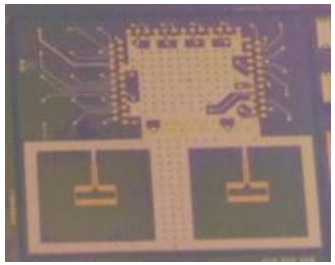
Same front side CPW 50Ω with TSV access from backside



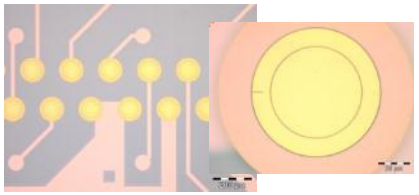
Interposer process flow

1. BEOL 2 levels + antenna

Full interposer die view

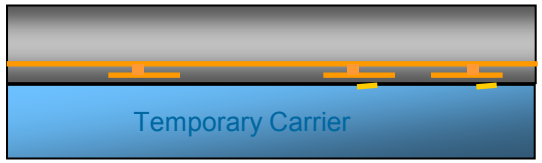


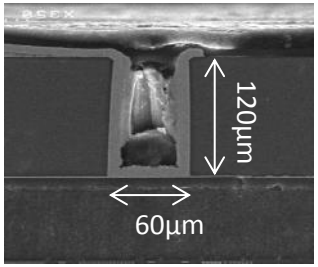
Folded dipole antenna



Frontside Cu RDL and TiNiAu UBM

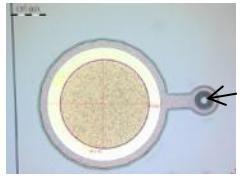
2. Temporary bonding and thinning to 120µm





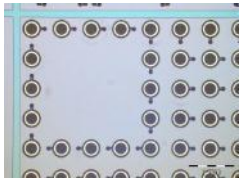
3. TSV AR=2 processing + RDL 5µm

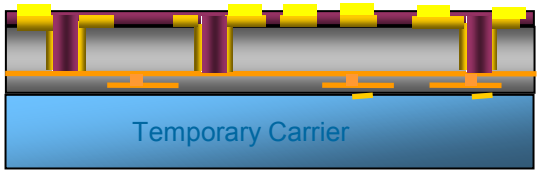
Backside TiNiAu UBM

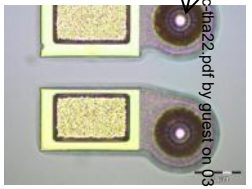


TSV

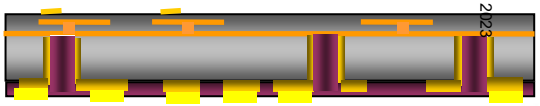
4. TSV + polymer passivation + UBM



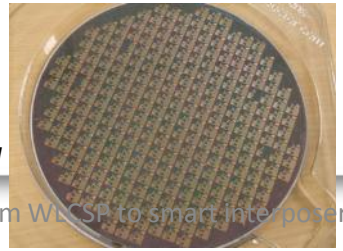




5. Temporary carrier debonding

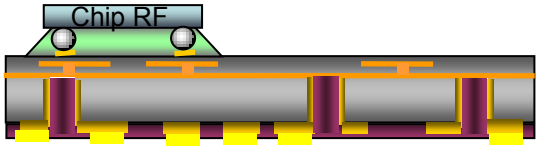


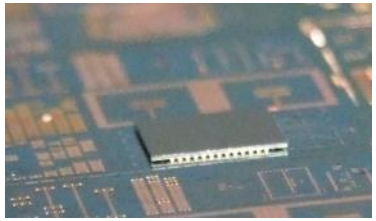
Final debonded 200mm wafer



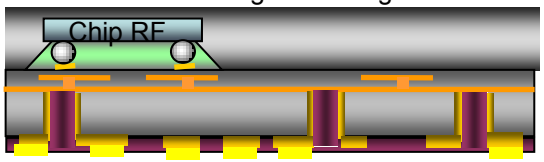
Interposer assembly

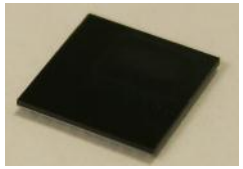
6. RF die flip-chip





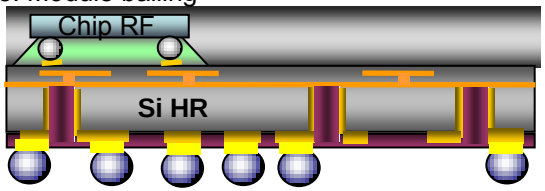
7. wafer-level molding and dicing

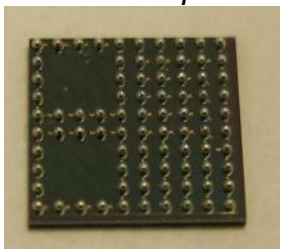


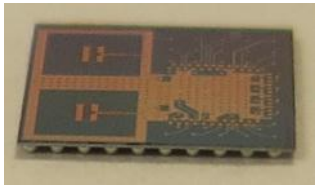


Molded interposer with balling

8. Module balling



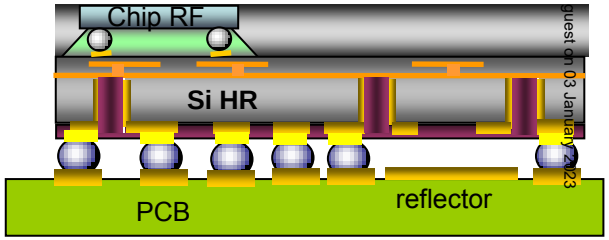




Interposer with balling w/o molding

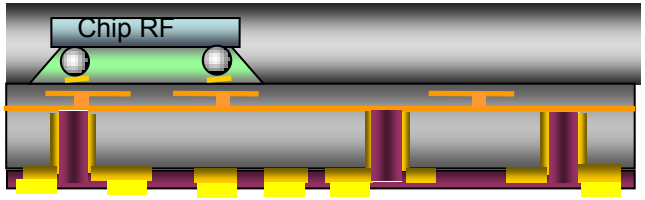
Note: Wafer-Level balling also possible (demonstrated on VT)

9. Assembly on PCB board – ***ON GOING***



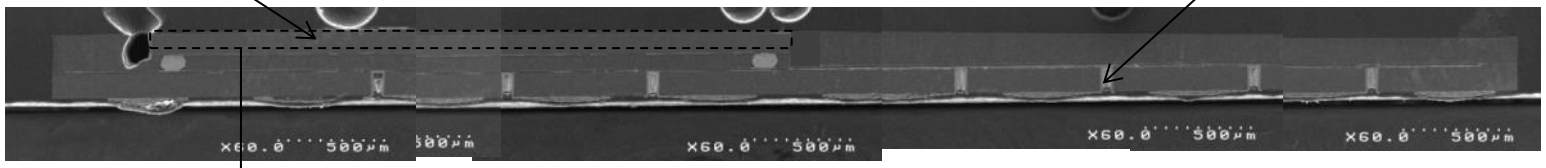
Interposer wafer level molding

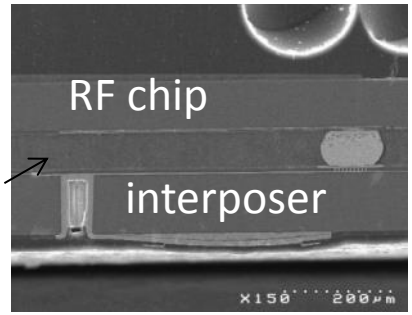
7. wafer-level molding and dicing



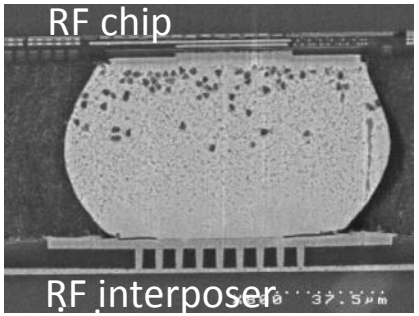
120µm thin CMOS transceiver die

TSV





Underfilled molding



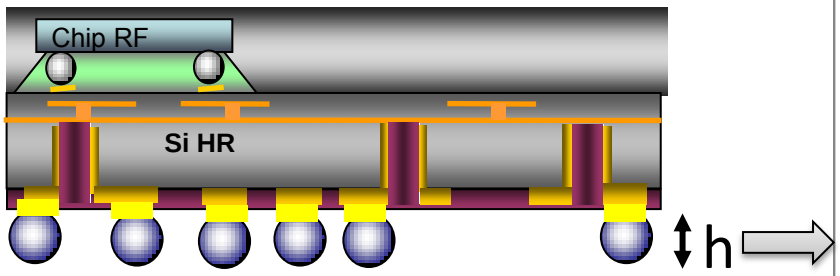
RF chip ball connection

50µm

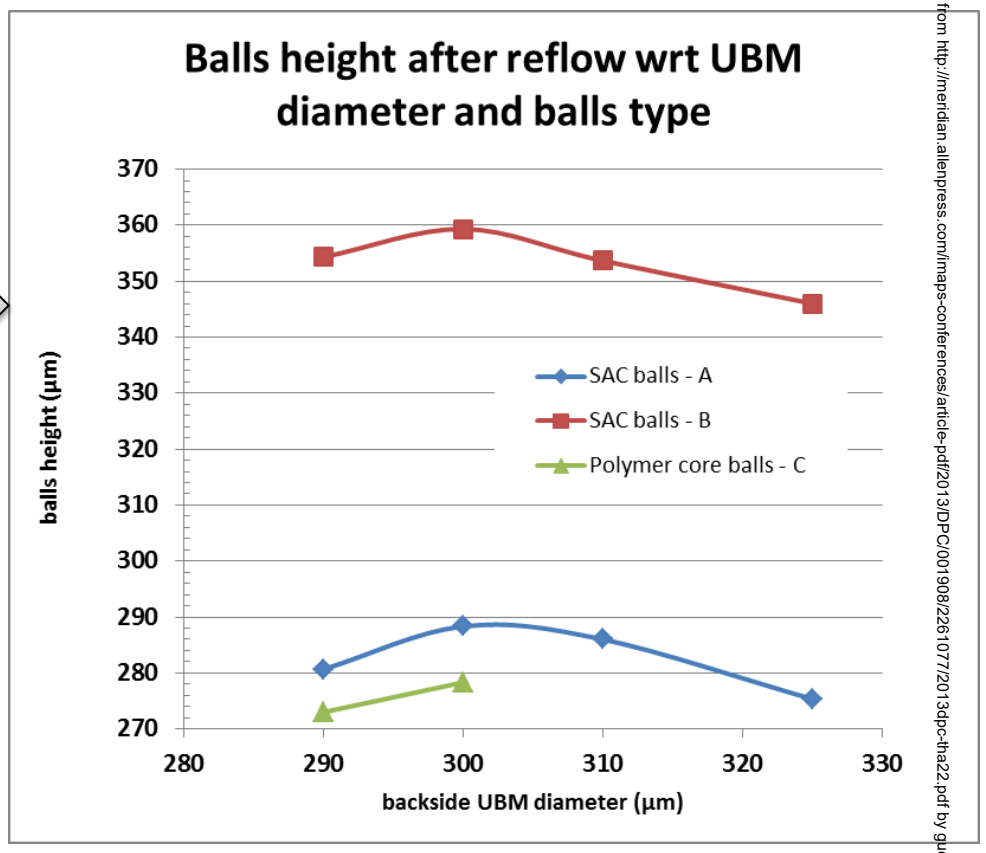
➔ Laminated molding acts as an underfill
➔ Reduction of pacakaging costs

Interposer assembly: balling and stand-off

8. Module balling

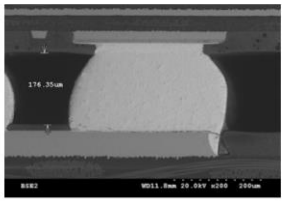


Final stand-off target : 270µm

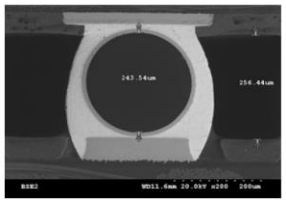


Balls height configurations investigations:

- 2 SnAgCu (SAC) with different diameters
- 1 polymer core ball
- 4 UBM different sizes



SAC ball

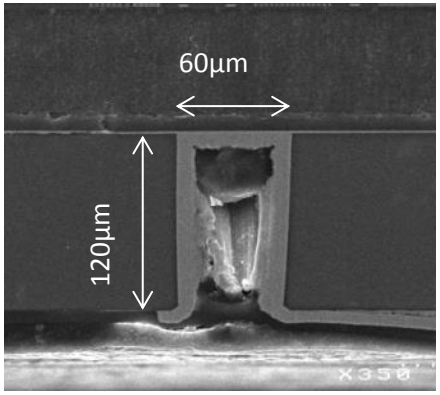


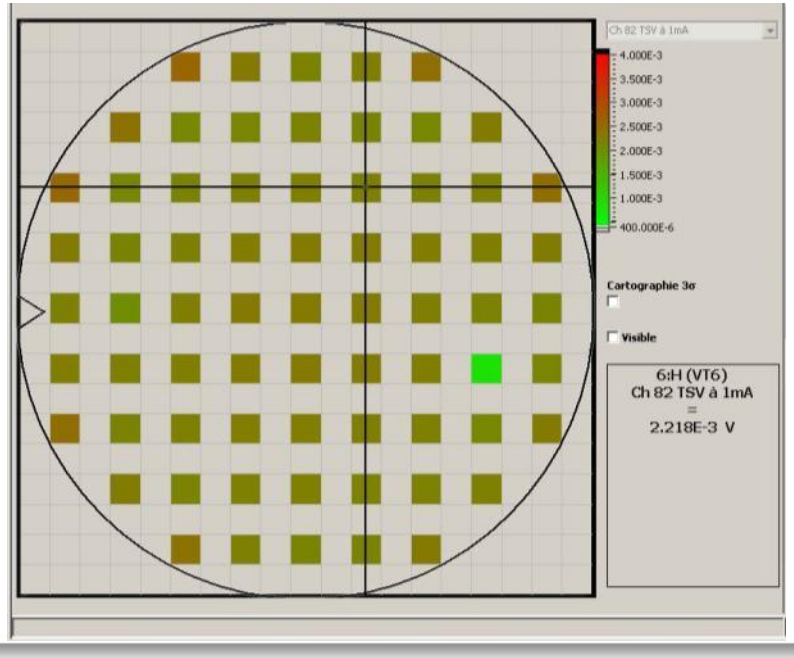
Polymer core ball

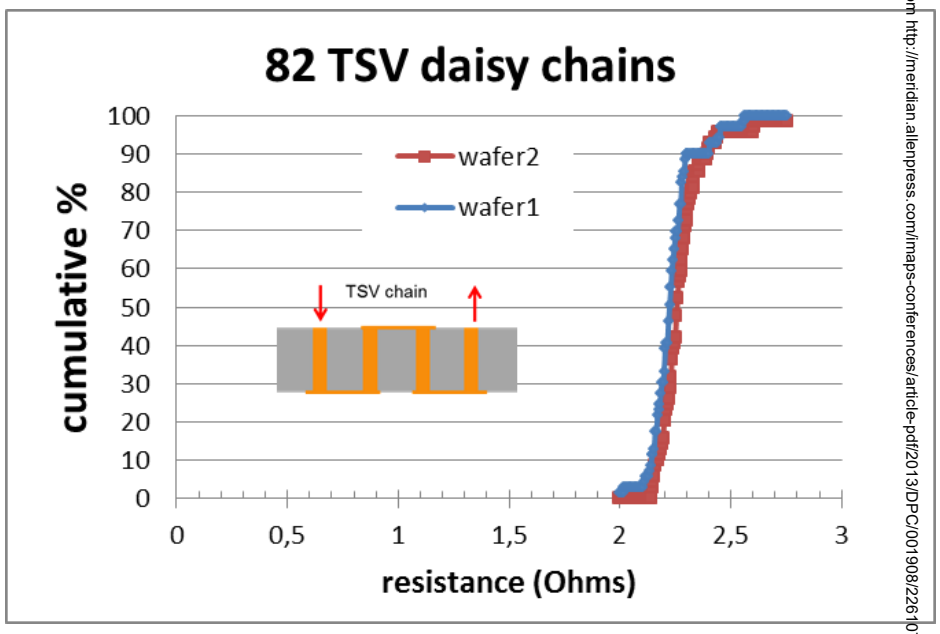
➔ Optimization possible with design
➔ Similar results than SoA WLSCP
➔ Thermal cycling and drop tests on-going

TSV DC characterization

DC measurement of a 82 TSV daisy chains







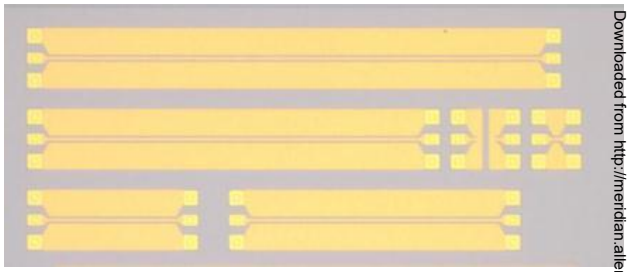
10 wafers
99% yield on TSV,
R_{TSV} ~ 15 mΩ per TSV

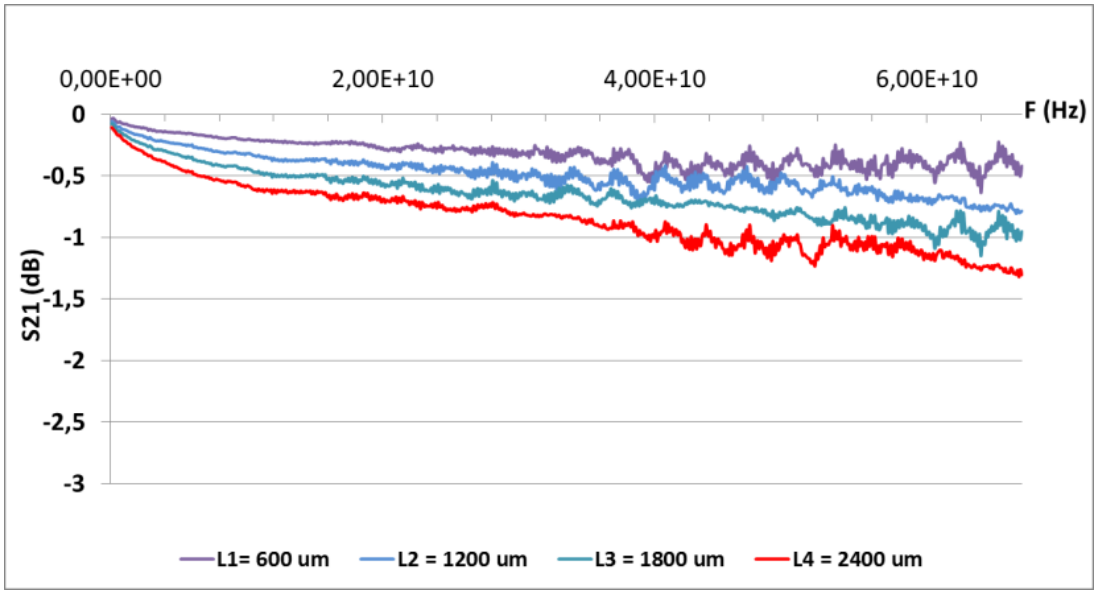
➔**Mature technology**

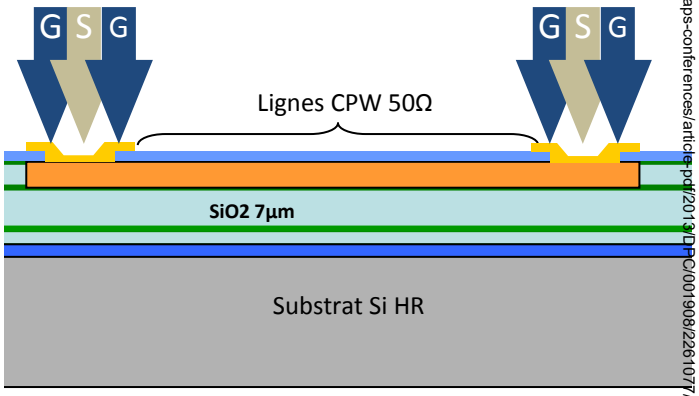
RF frontside characterization

Front side transmission line measurements

- Line length evaluation
  - Front side measurements up to 67 GHz
  - Design for 50 Ohm matching

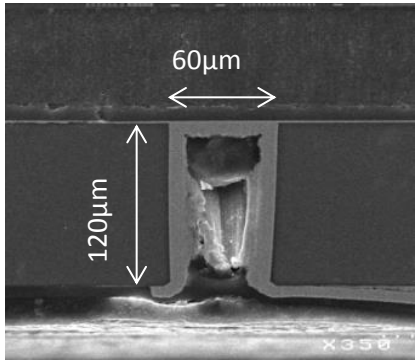


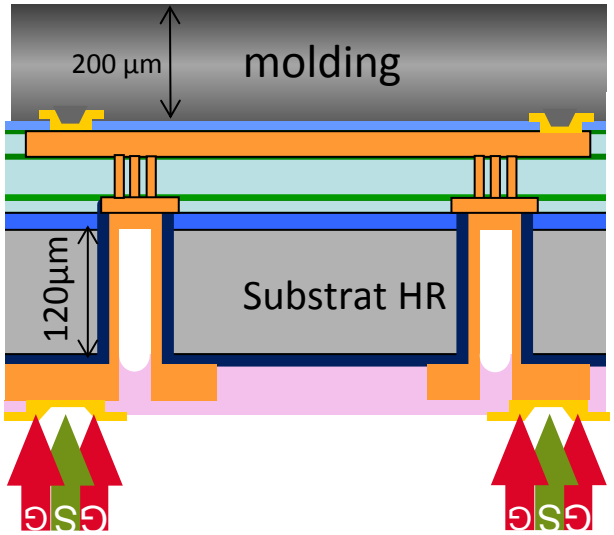




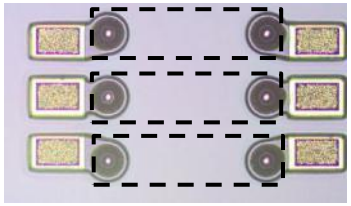
- 4 different lengths: 600, 1200, 1800 and 2400µm
- Attenuation loss <0.5 dB/mm thanks to 7µm IMD oxide
- S11 < -20dB up to 60GHz ➔ **good impedance adaptation**

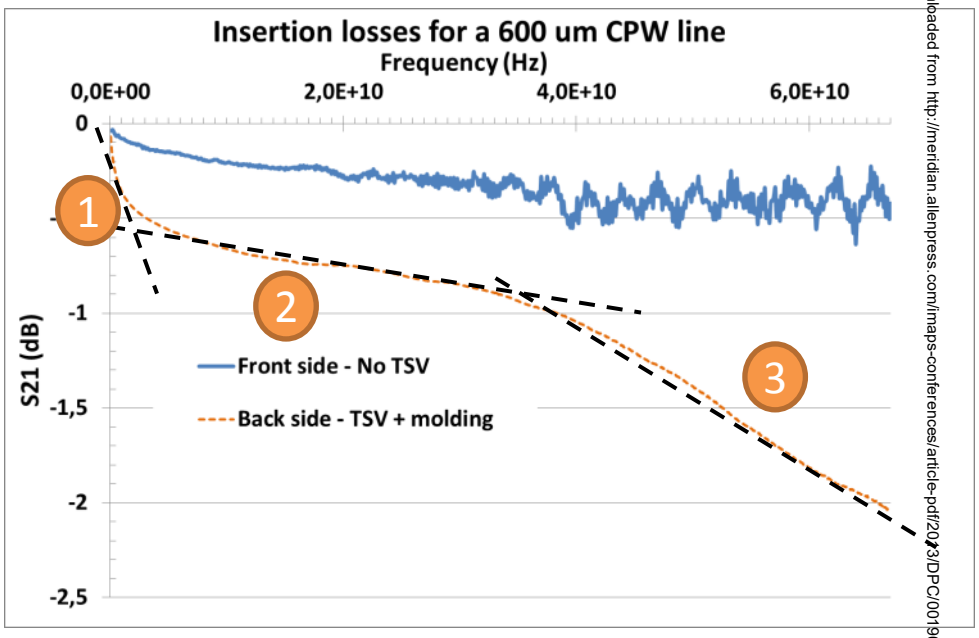
TSV RF characterization (1/2)





Backside measurments





3 typical regions:

1: Capacitive region: TSV capa driven ~ 1pF

➔ Increase the passivation thickness

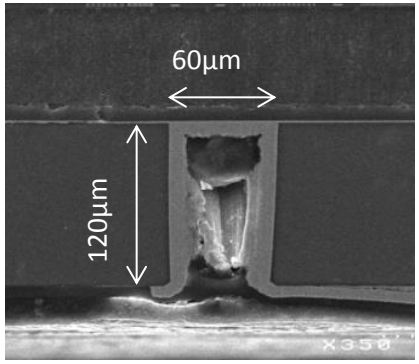
2: Si substrate : resistive region, impact of lossy Si

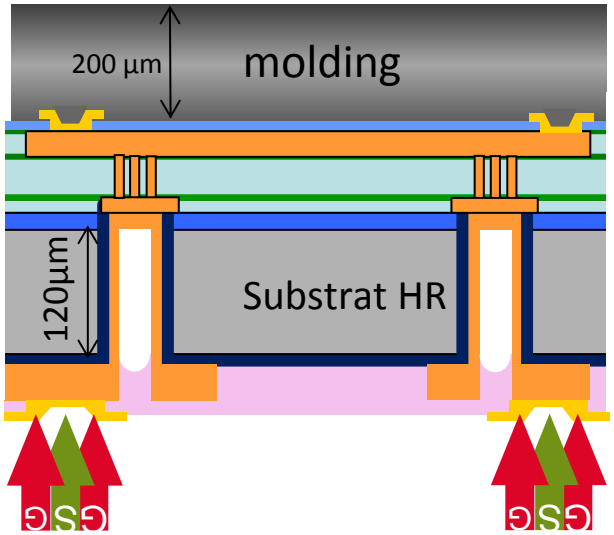
➔ increase Si resistivity

3: Inductive driven behavior

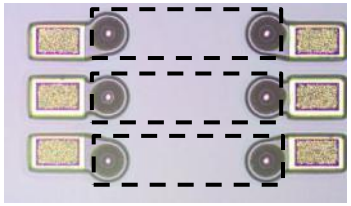
➔ Reduce the pitch of TSV

TSV RF characterization (2/2)

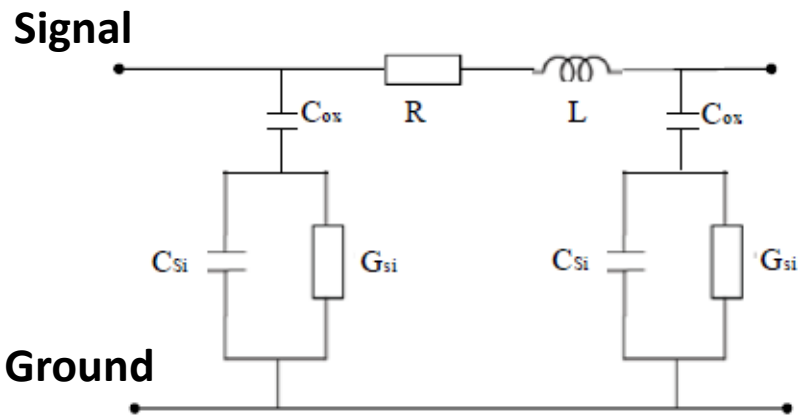




Backside measurments



TSV last π-model



At low frequency (<1 GHz): theoretical data confirmed by measurements:

- R ~ 15mOhms
- L = 38,3 pH
- Cox = 1237 fF
- Csi = 30,3 fF

At higher frequencies:

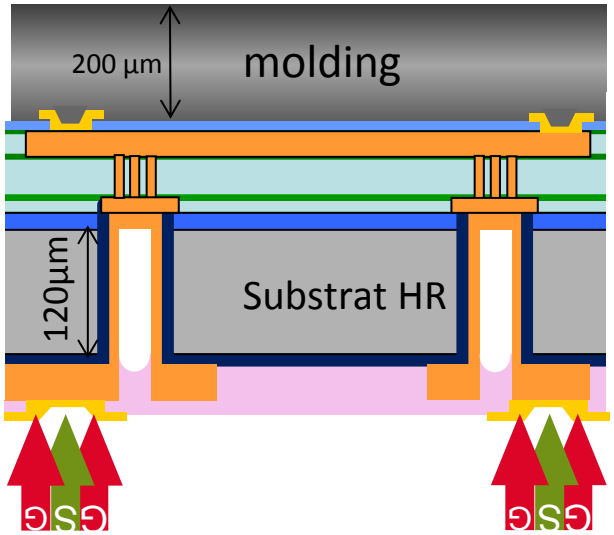
Insertion loss @ 60GHz: ~0.5 dB/TSV

➔ communication to PCB Ok for < 1GHz

➔ Acceptable loss at 60GHz, room for improvements

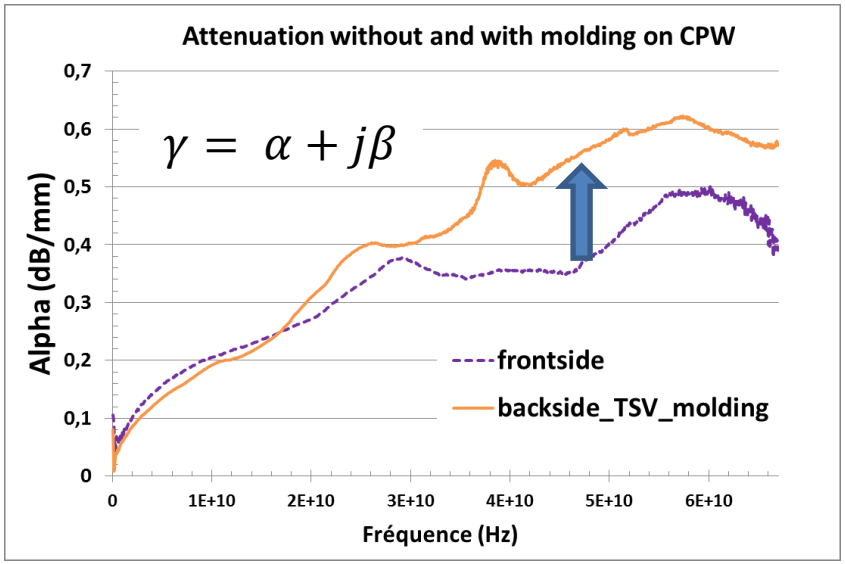
Molding RF characterization

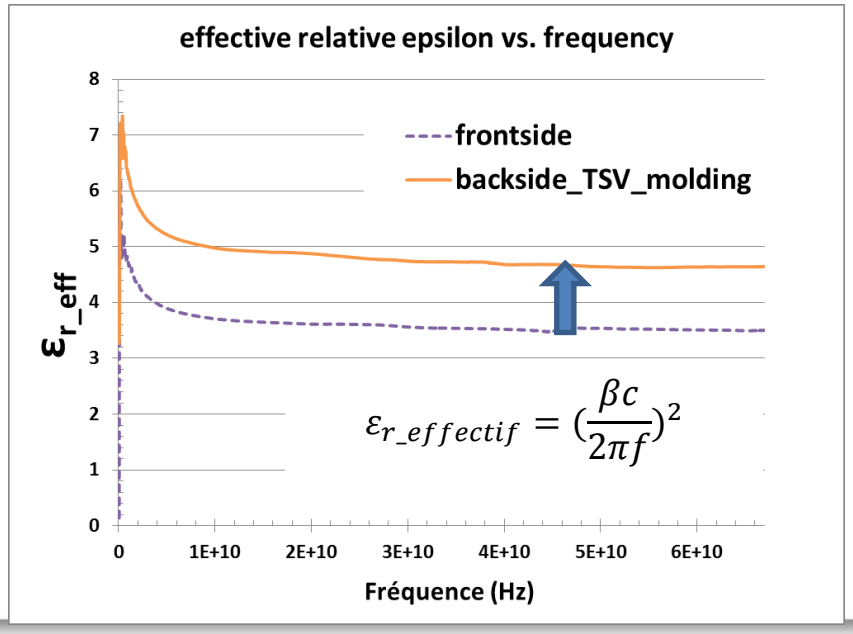
Laminated wafer level molding on 120µm thin Silicon wafer: No stress induced



Measurement of 2 lines l1 and l2:

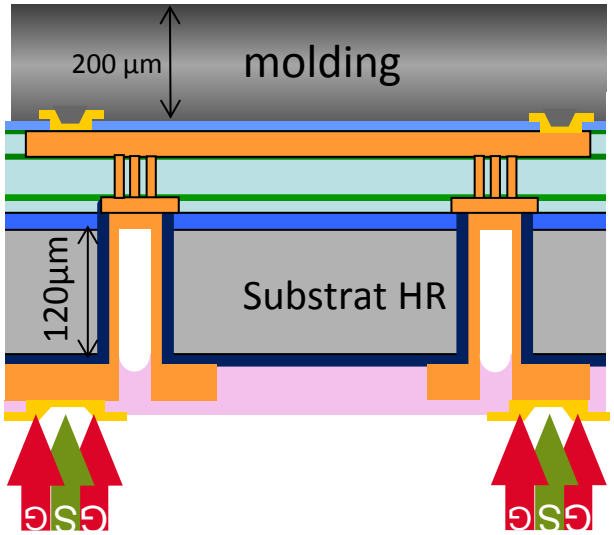
$$\gamma = \frac{arcosh\left(\frac{trace(T_2 * T_1^{-1})}{2}\right)}{l_2 - l_1}$$



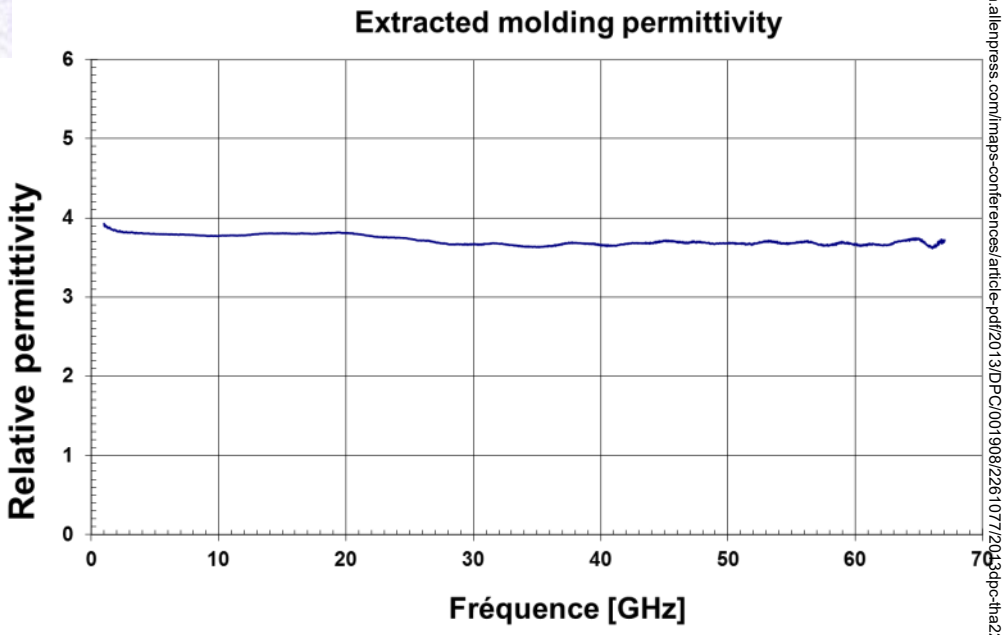


Molding RF characterization

Laminated wafer level molding on 120µm thin Silicon wafer: No stress induced



Differential method permittivity extraction:
Without molding - With molding datas



- ➔ Consistent with high content of SiO2 fillers
- ➔ Tangent delta loss at 60 GHz < 0,01
- ➔ Low stress WL molding suitable for 60GHz appl.

Outline

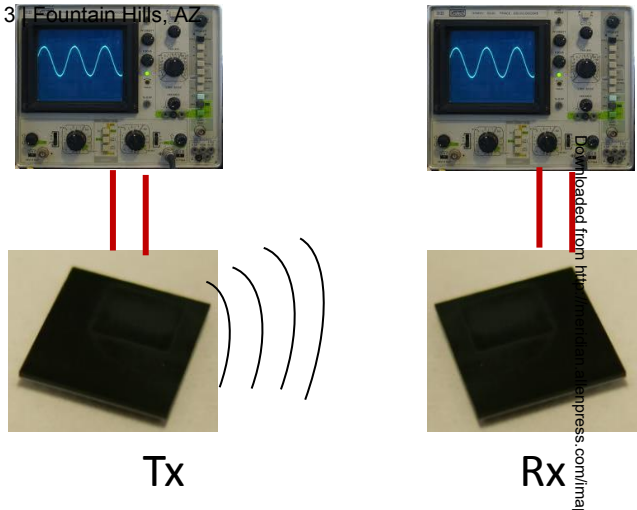
- Introduction: from WLCSP to smart interposers
- Mmw interposer description and characterization
- Conclusions and perspectives

Conclusions on mmW interposer

- Technological modules validated
  - Promising wafer level laminated molding
    - No stress observed
    - Laminated on 120µm thin wafer
    - Underfilling
  - Mature and low loss TSV-last technology
  - Adaptative balling wafer-level balling
- First promising mmW results
  - Attenuation loss compatible with applications
  - Very limited impact of the WL molding

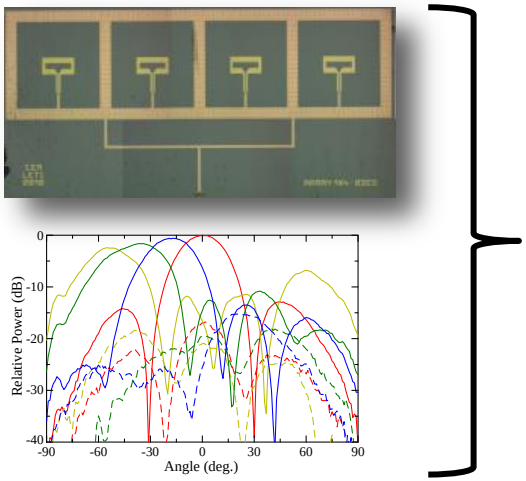
mmW demonstrator perspectives

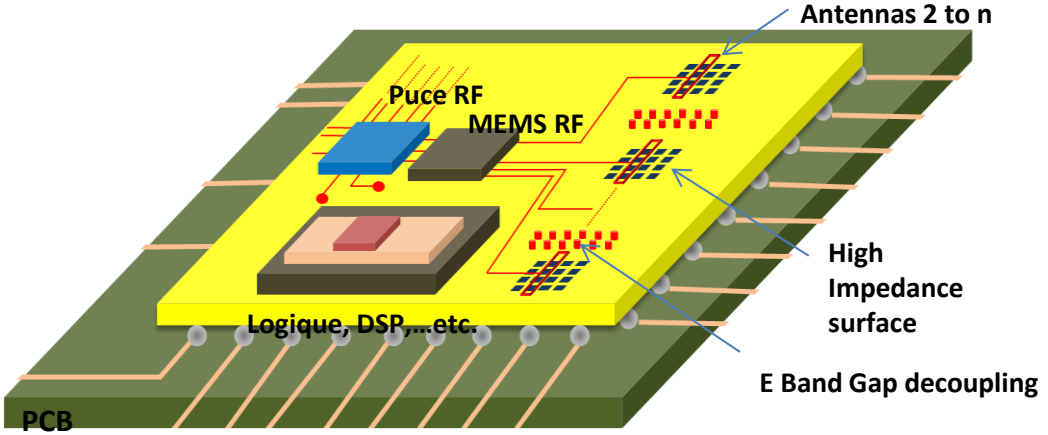
- Characterize the antenna with reflector on PCB
- Realize data transmission between 2 modules
- Validate the Board Level Reliability (TC and DT)



Medium term:

- Implement the technology for multi antenna
  - Shield the antenna from each other
  - Beamforming by individually controlled phase signals
- Implement phase-shifter in the interposer platform





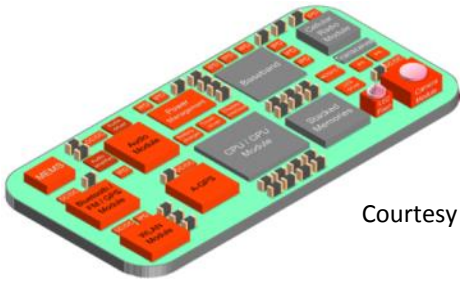
Dussopt, Lamy et al. IMS 2012

From WLCSP to smart interposer: perspectives

WLSCP

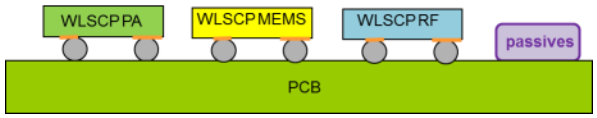
- Cost (reducing BOM)
- Size
- Performances

Many individual components



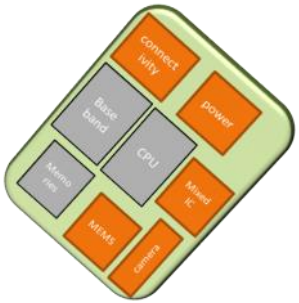
Courtesy of Yole

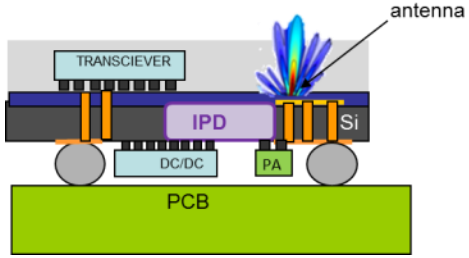
TODAY



Silicon package

modules in SiP + IPDs

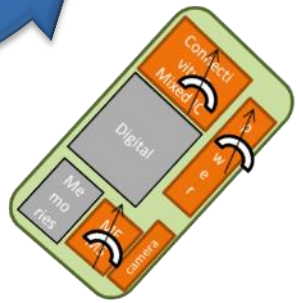


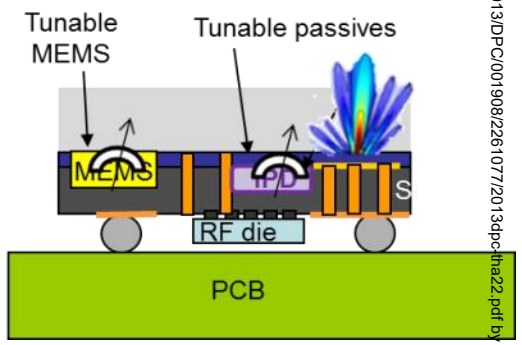


- MEMS integration
- Tunable passives

Smart interposer

Interactive module & tunability





Interposer: More than just a « piece of silicon »

LABORATOIRE D'ÉLECTRONIQUE
ET DE TECHNOLOGIES
DE L'INFORMATION

CEA-Leti
MINATEC Campus, 17 rue des Martyrs
38054 GRENOBLE Cedex 9
Tel. +33 4 38 78 36 25

www.leti.fr

Thank you for your attention

yann.lamy@cea.fr