Advanced Packaging & Systems
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Innovative yet Cost - effective technologies

Stacked 3-D package with Improved Bandwidth & Power Efficiency

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Summary

- **TSV based 3-d stacks achieve high bandwidth and power efficiency because TSVs allow great increase in interconnect density and number while at the same time shorten the interconnect length and parasitics**
- **But TSV technology is still immature with low yield and high cost, is far from adoption in consumer electronics like Smart Phones**
- **We have developed an alternative approach to reduce interconnect parasitics w/o requiring TSVs, no TSVs have to be created on active dice !**
- **by using our method Conventional stacked packages used in SmartPhones can be improved – the result is SuperPoP, capable of delivering a Bandwidth of 12.8 GBps and saving at least 55 % of the power dissipated in package interconnect.**
- **It is no longer necessary to “drill” holes in perfectly good wafers !**

Outline

- **Main message : it is not necessary to drill holes in active devices to achieve high Bandwidth, power efficiency**
- JEDEC (user) feedback / roadmap on Wide I/O
- Device performance concerns with TSV, Wide I / O
- Potential major applications of Wide I / O, trends in SoC and Memory
- PoP packages
- Potential future benefits of TSV based 3-D stacks
- Limits to performance of PoP packages
- **MAGIC Chips, a novel approach to enhance PoP performance w/o having to create TSV s in functional chips**

JEDEC on Wide I/O for Memory (Fall 2012)

JEDEC *LPDDR3 Symposium 2012*

October 29, 2012

San Jose

" The Trends of Future Mobile Memory DRAMs "

Mian Quddus,
Chairman, BOD, JEDEC

2013 : LPDDR2 → LPDDR3

2014 : LPDDR3 → LPDDR3E

2015 : LPDDR3E → WIDE I/O (2)

2015 : LPDDR3E → LPDDR4

So what made JEDEC change their roadmap for Wide I / O, postpone introduction ??

Stacked 3-D package with Improved Bandwidth & Power Efficiency

ISHM (IMAPS) 1995, Proc. IEEE - ECTC 1994, Trans. IEEE – CPMT 1995, …

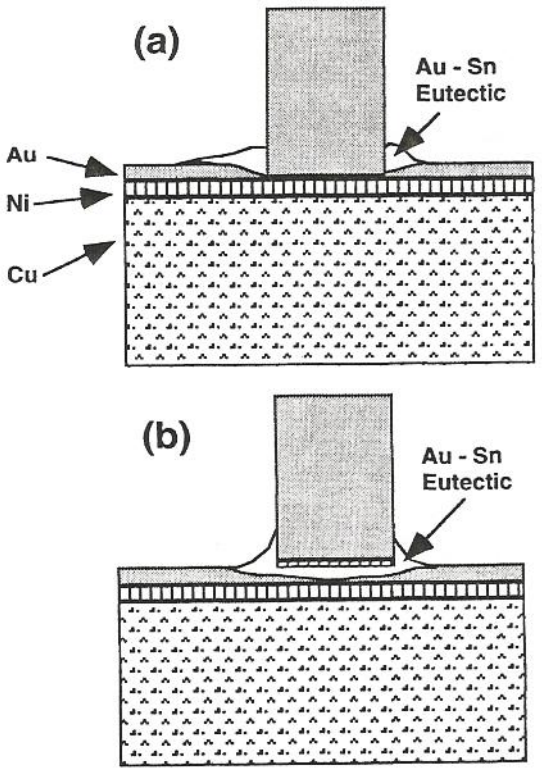


Figure 2: Bond structures for (a) 'old' baseline bonding process , and (b) ideal bonding process which would produce bonds with well - developed fillets and an eutectic layer between the bump and the substrate.

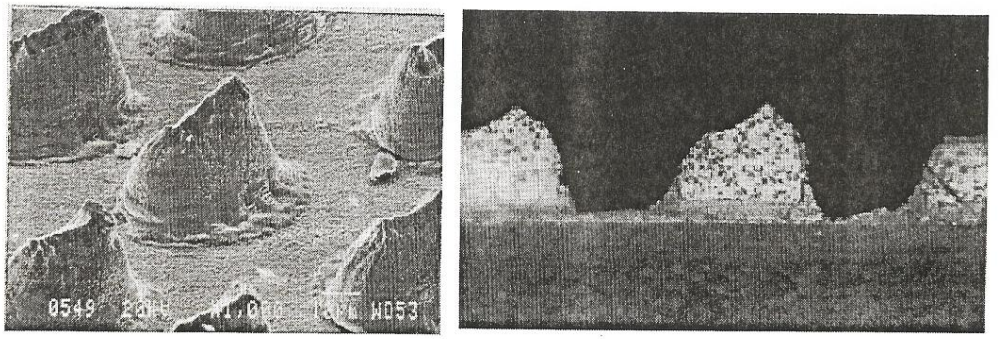
heat sinking effect of the unheated chip tool was removed

Development & early production (1996) of Micro - Pillar (45 um pitch) FC with Sn capped bumps

Motorola **'GoldFinger' pillar bumps implemented in GaAs FETs for PAs in Mobile Phones**

Manage the flow of molten Sn in reflow & TC bond during pressure bonding by changing its viscosity
Too much pressure applied by thermode to improve heat transfer (/ melting) may impede formation of reliable joints!

Control thermode temperature & pressure profiles

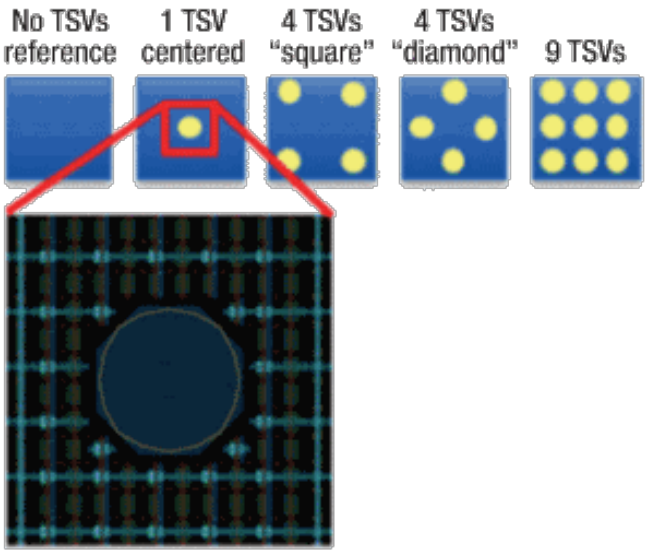


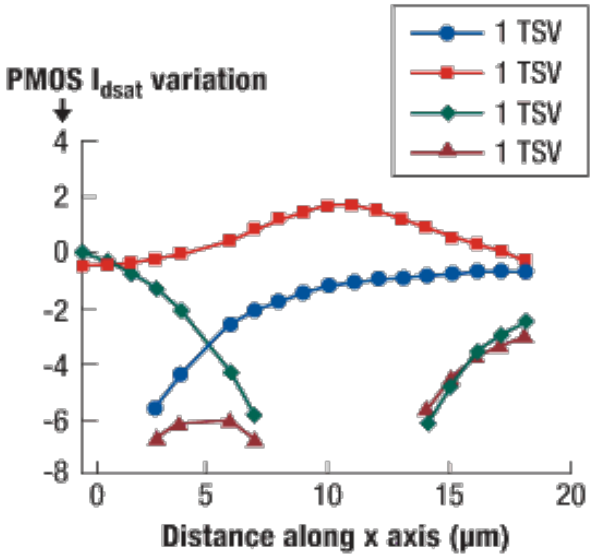
(a) (b)

Figure 7: Fillet formation around the bumps bonded after infrared reflow. Also shown (b) cross - section of such bonds indicating not just well formed fillets on the sides of the bumps but eutectic layer between the bump and the substrate. Compare structure with that postulated in Figure 7b [13].

FEASIBILITY OF BONDING REFLOWED Au - Sn BUMPS

Stress & Thermal effects in die stacks with TSVs





Effects of TSV induced Stress on Device performance (simulation, circa 2011) :

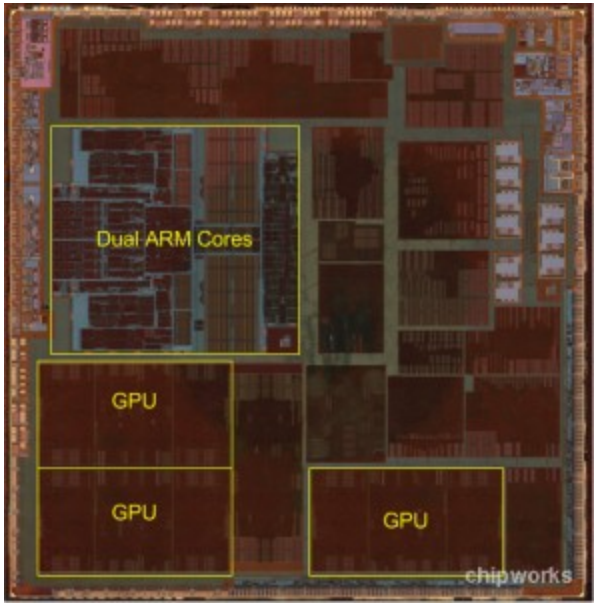
associated Idsat variation for Short-channel transistors are up to 9%.

depending on the number of TSVs in the matrix the Keep Out Zone (KOZ) can range :
- **digital devices : 6 - 20μm**
- **analog devices : 20 - 200μm**

These are substantial silicon real estate to be set aside for stress relief.

Unlike in Memory, for SoCs the distribution of TSV may have to be quite random

Trends in SoC and Memory in SmartPhones



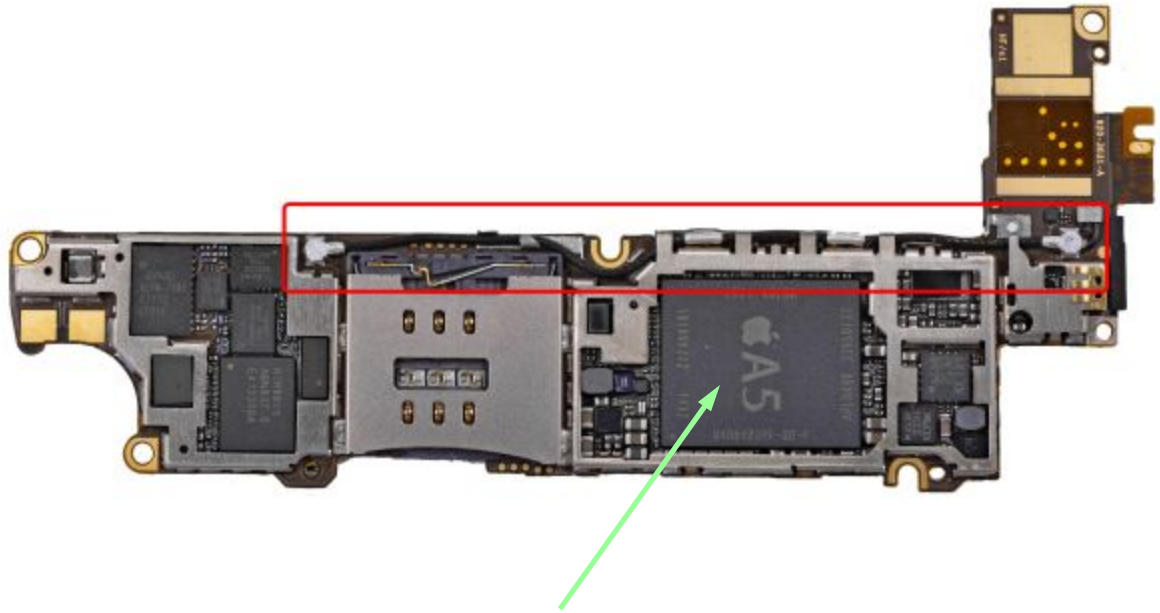
courtesy ChipWorks

Multi – core A6 die in iPhone 5

32 nm HKMG, Dual Core, 3 GPUs, 10 mm sq. die

- SoCs (processors) with increasing number of GPUs to drive ever larger displays of higher resolution at faster refresh rates
- Performance of Multicore processors depend on parallel access to Memory
- LP DDR (Dual Data Rate) 32 bit memory, 1 to 2 GB in 2 chips over the SoC in a PoP with 200 to 260 I/O s
- At present SoC to Memory data transfer at a Clock Rate of 400 MHz via Dual channel (2 x 32 bits) but in future Quad channel (parallelism)
- LP DDR 3 Package interconnect Power losses rising to 30 %

Major application of PoP packages and their potential replacement by Wide I / O

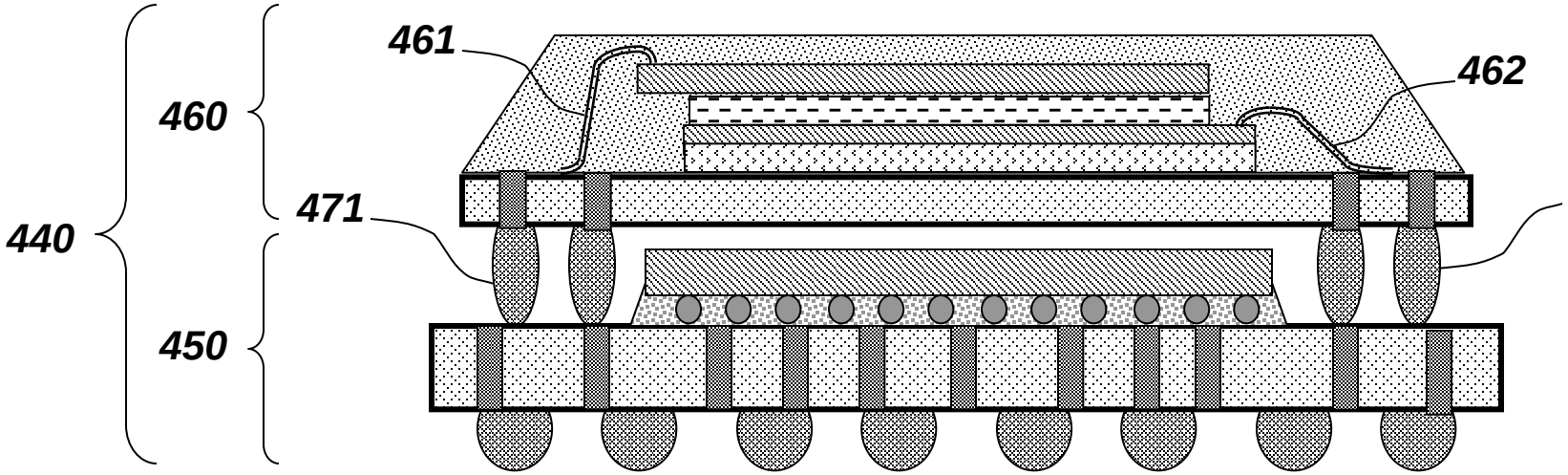


A5 processor with LP DDR 2 Memory in a PoP

Smart Phones (> 700 million units per year) SoC – Memory :
PoP remains an universal package solution

Tablets : PoP quite common with one major exception

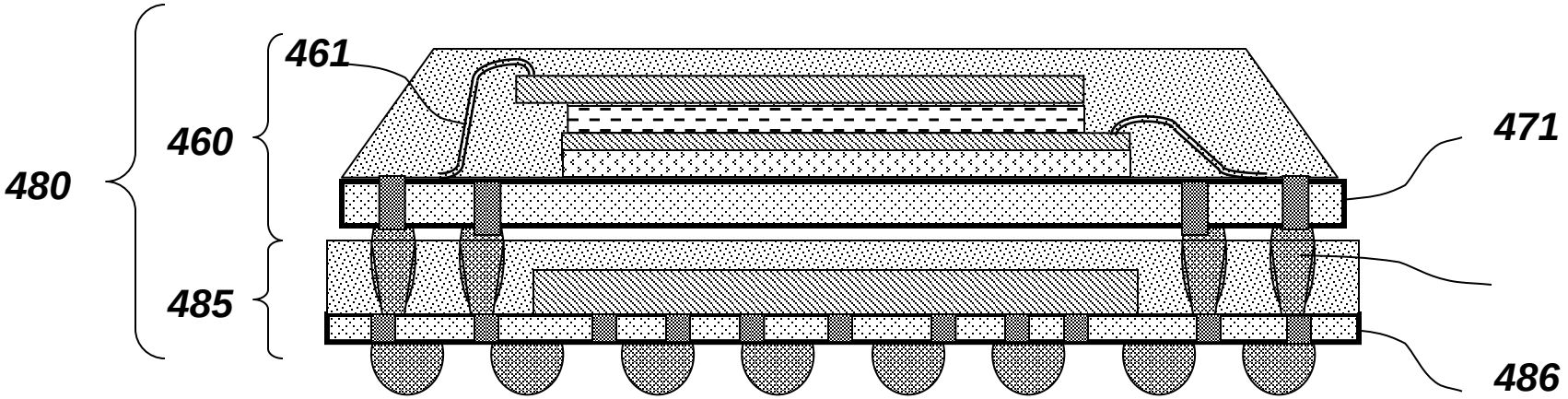
Major application of PoP packages



PoP package showing Processor with Memory stacked on top

Stacked 3-D package with Improved Bandwidth & Power Efficiency

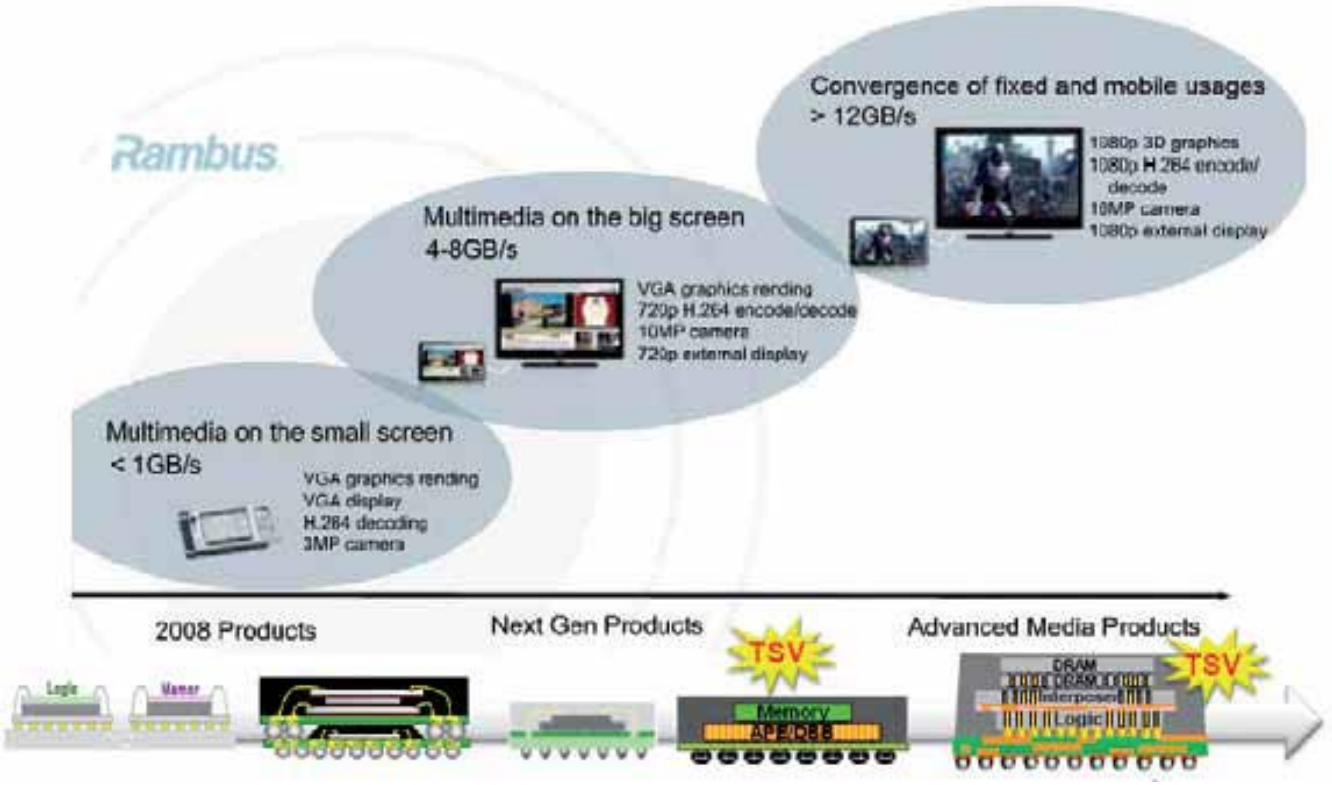
Major application of PoP packages



PoP with processor in eWLB type package at bottom

Stacked 3-D package with Improved Bandwidth & Power Efficiency

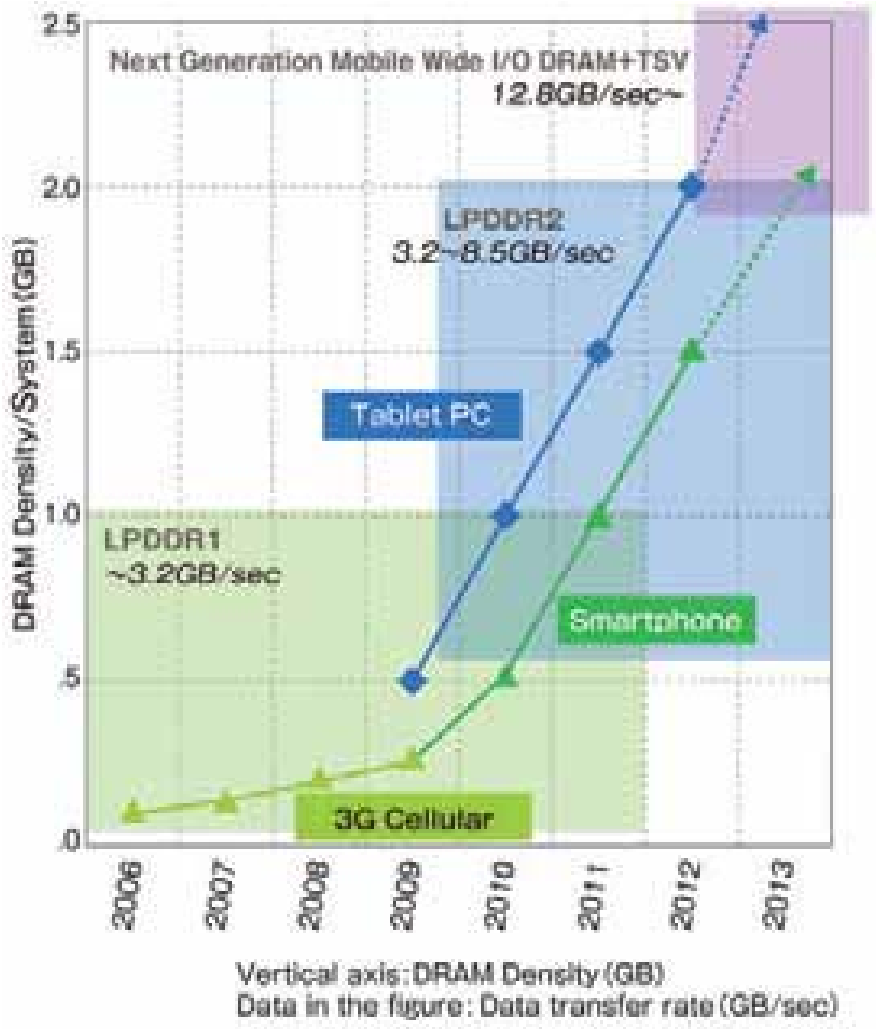
5. Incumbent technologies & their limits



Propagation Delays in conventional Packaging will hold up Games and Movies !!

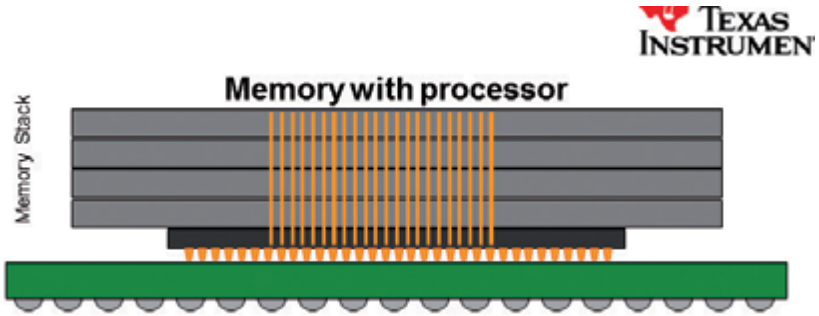
Stacked 3-D package with Improved Bandwidth & Power Efficiency

Drivers & expected applications of 3D

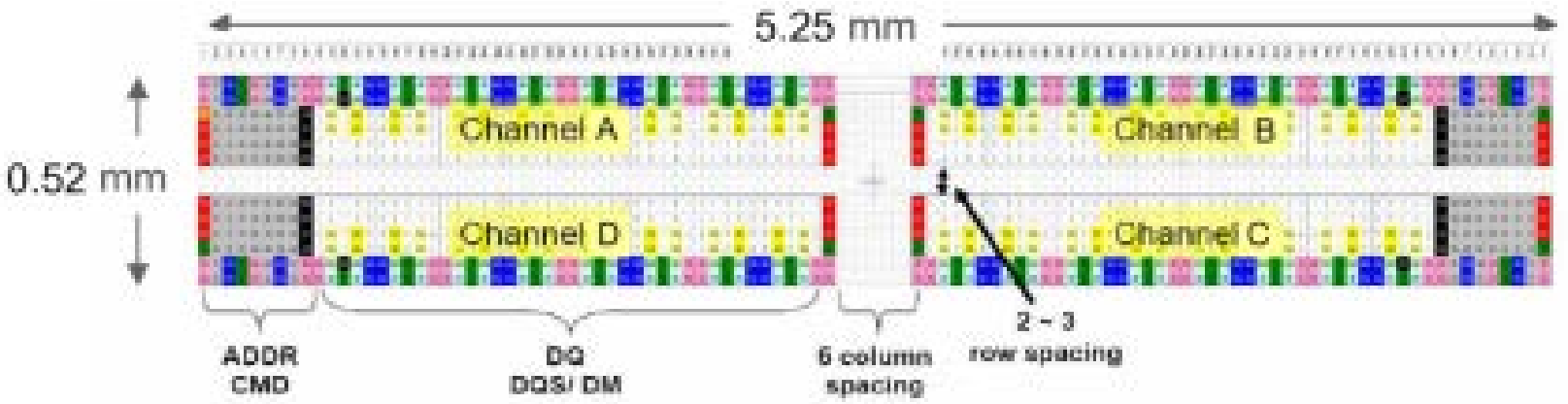


LTE (up to 20 GB / sec) will drive transition to TSV for SoC / DRAM (LP DDR3) / NAND module from PoP

Potential future benefits of TSV based 3-D stacks

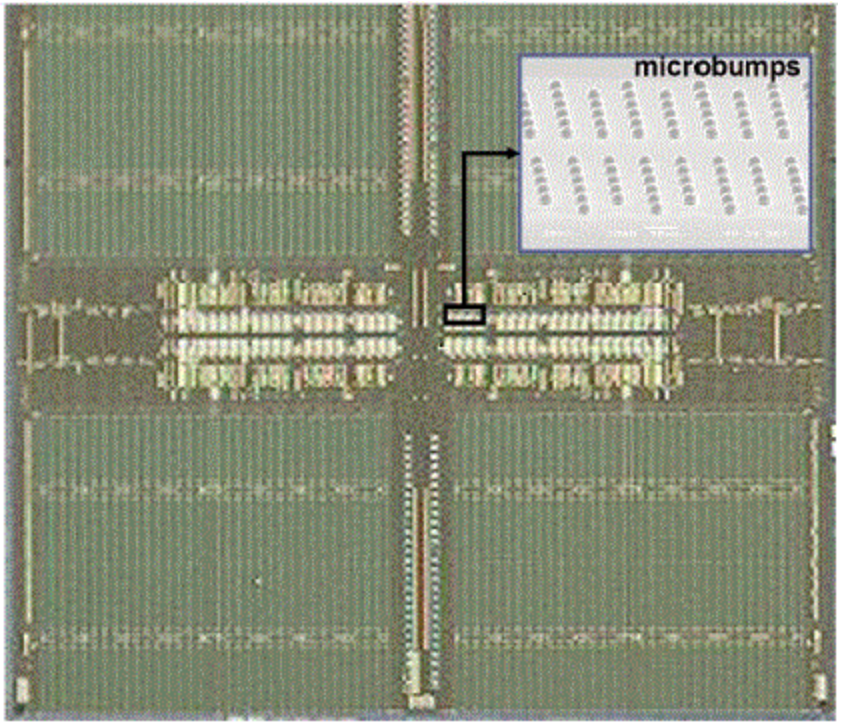


Memory Stacks w/ TSVs



Details of Wide I/O Bus located in the middle of Memory chips stacked in 3D (per JEDEC)

Stacked 3-D package with Improved Bandwidth & Power Efficiency

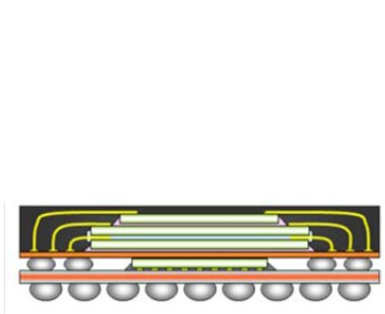


Samsung Wide I/O Memory Demo (Fall 2010)

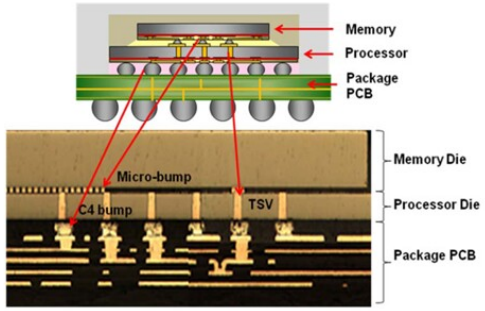
- The whole chip is made up of 4 symmetric partitions of 4 × 64Mb arrays, peripheral circuits and microbumps.
- To reduce power consumption and support high data bandwidth, I/O driver loading is reduced by adoption of **44 × 6 microbump pads per channel,** located in the **middle of the chip**.
- **Die area** is 64.34 sq. mm (25% larger than 1Gb LPDDR2).
- The **TSV**s are 7.5 µm in diameter, with resistance 0.22 to 0.24Ω and capacitance of 47.4 fF
- The **microbumps are 20 × 17µm2 on 50µm pitch** and consists of **Sn caps on Cu pedestals**

3-d stack bonding reuses Thermo-compression Flip Chip Bonding of Sn capped Micro – Pillar Bumps (Motorola, 1994)

Potential future benefits of TSV based 3-D stacks for SoC & Memory

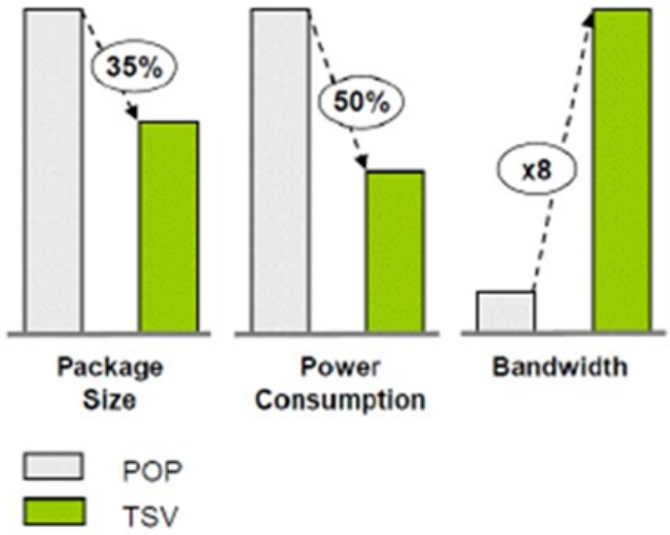


FC PoP



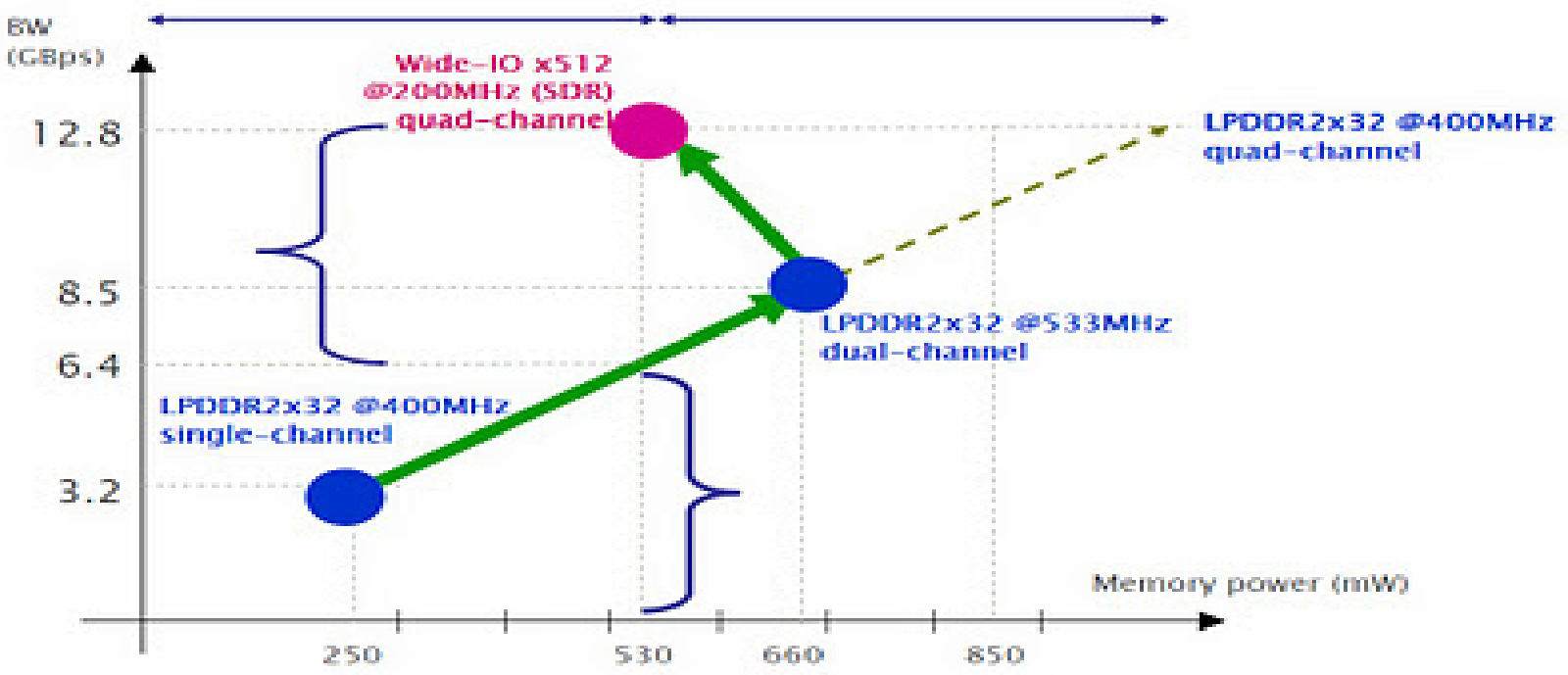
TSV-SiP with wide IO DRAM

	Conventional 3D Package (FC-PoP) with LPDDR2	TSV-SIP with Wide IO memory
Memory I/O Power Consumption	176 mW	44 mW



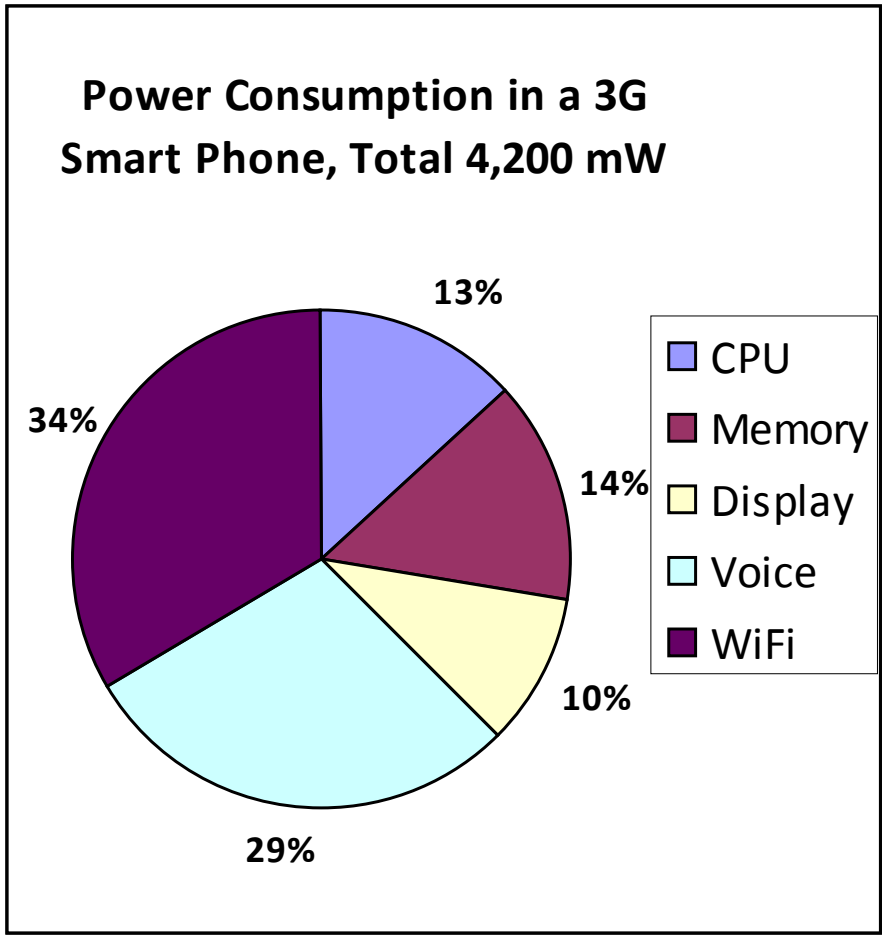
Bandwidth & Power Savings

Bandwidth and Power trends



So what is keeping Portable electronics from switching to TSVs ?

4G LTE phones are Battery hogs !



- To increase Bandwidth, LTE 4G phones operate on multiple wave-lengths (10 +) simultaneously
- Such operation require keeping multiple RF circuits turned ON.
- LTE Smart phones consume from 5 to 20 % more power compared to 3G Smart Phones

Power Dissipation in Digital / Switching Circuits

Power to drive I/O

$$P = n * T * f * C * V^2 \qquad (1)$$

where, T is the Toggle Rate = 2 for DDR memories

On the other hand the Bandwidth

$$B = n * T * f \qquad (2)$$

Increasing ***n****, the no. of signal lines allows maintaining the Bandwidth* ***B*** *at a lower frequency* ***f***

Operation at a lower frequency makes Signal Integrity less critical *and enables error free operation.*

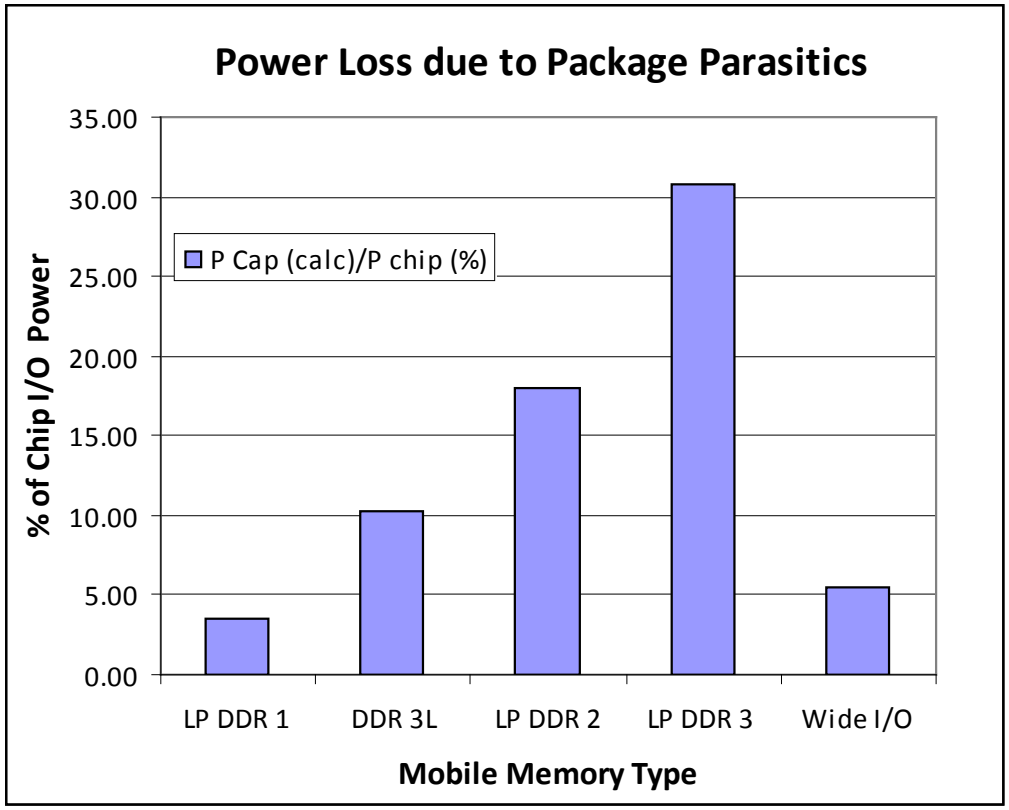
However as can be seen below it ***does not reduce the Power to drive I/O****.*

P*, the power to drive I/O lines, defined by Eq. (1), can be re-written as directly proportional to Bandwidth* ***B*** *(per Eq. 2) as follows.*

$$P = B * C * V^2 \qquad (3)$$

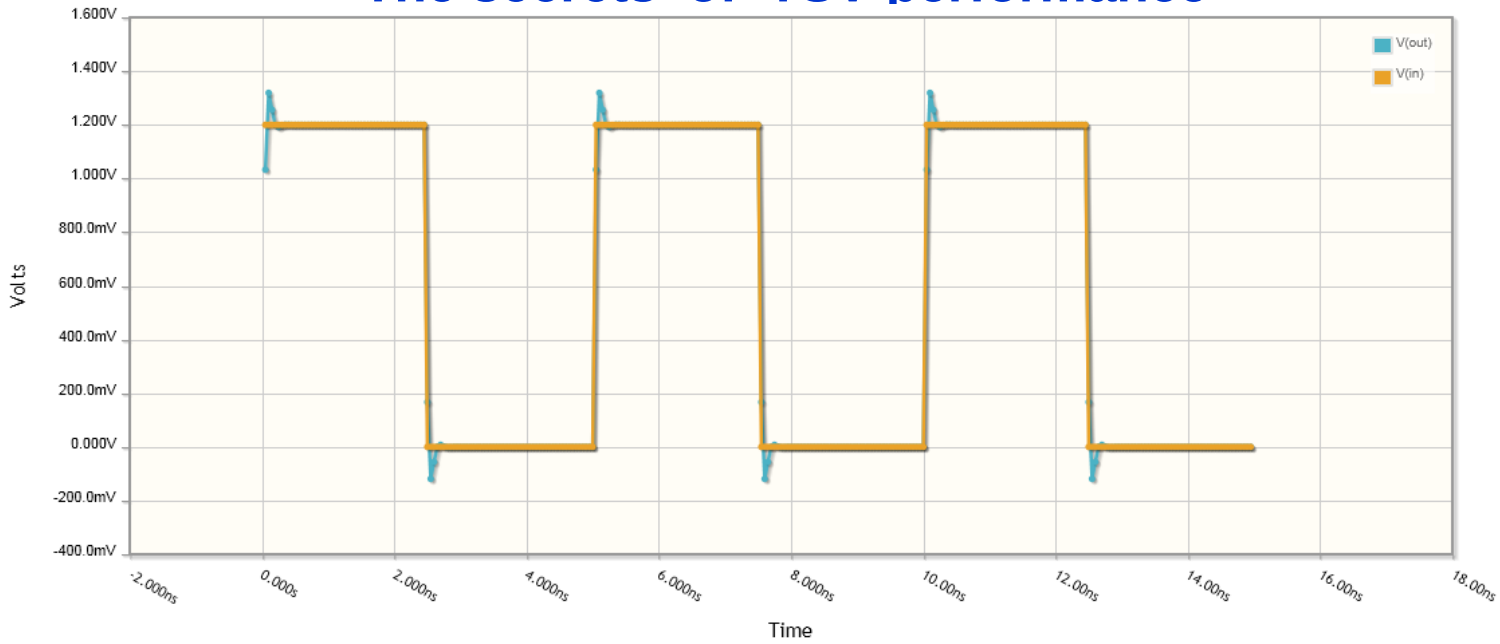
To reduce Power Loss at a constant Bandwidth, have to reduce C or drop the V - dd

Power Loss due to Package Parasitics in a Smart Phone



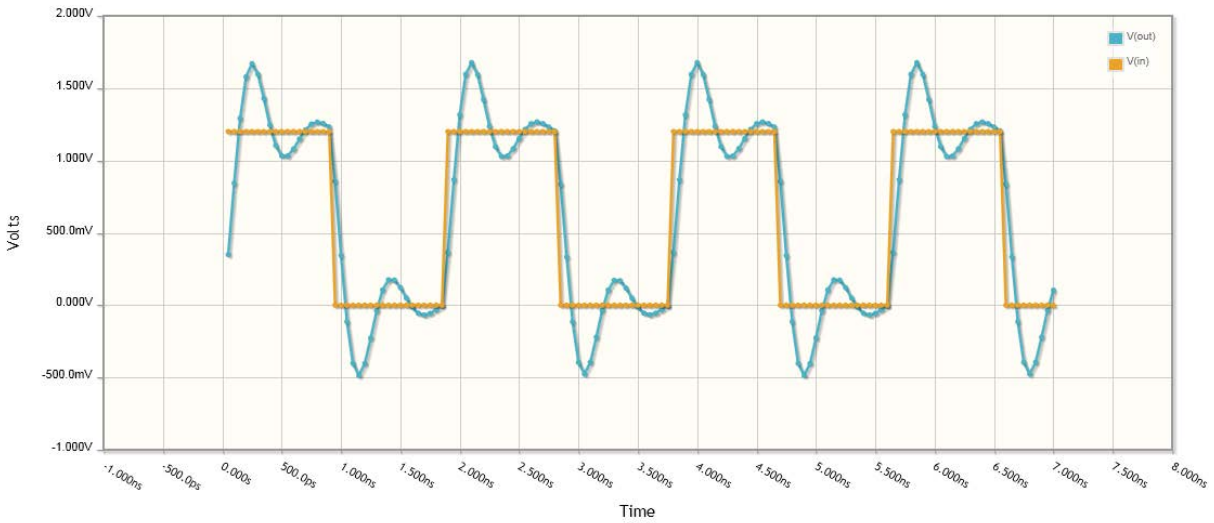
As the parasitics in Memory I/O Buffer is improved in successive generations (e,g. LP DDR 3 vs LP DDR 2), the Power Loss due to parasitics in PoP package become ever more significant !! Compare LP DDR 3 in PoP vs Wide I/O

The secrets of TSV performance



- The very sharp & clean output waveform at 200 MHz from chips stacked in 3D using TSVs and Wide I/O interconnection.
- The use of TSVs dramatically increases the density of interconnects between chips, reduces the length of interconnect between chips thus enabling Wide I/O bus with low parasitics
- Wide I / O can accommodate 4 data channels ea. 128 bit wide and even at a slow Clock Rate of just 200 MHz can deliver a Bandwidth of 12.8 GBps.
- Low parasitics of Wide I / O interconnect (e,g. C < 75 fF vs 500 fF for the trace on FC Organic Substrate in a PoP) reduce the power dissipated in interconnects (packages) by 2x

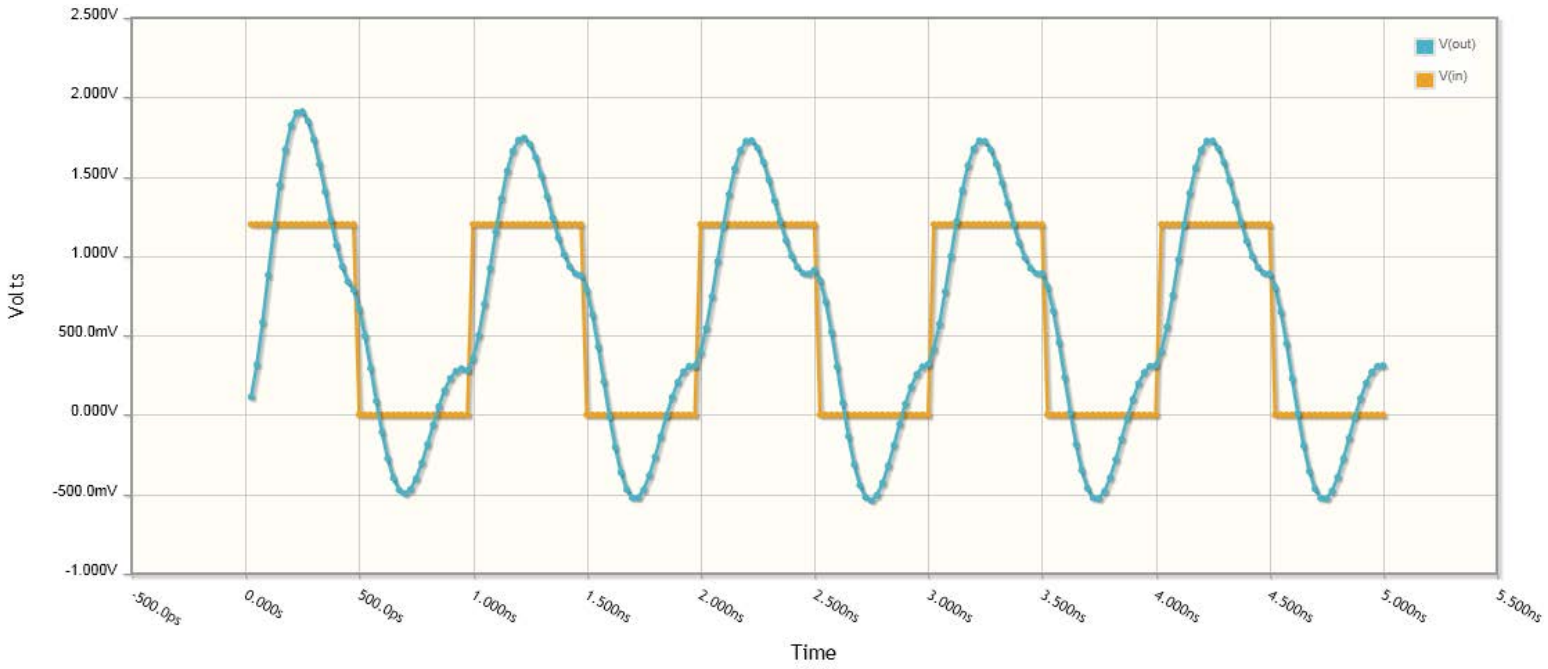
Current Performance limits of PoP



Simulated output signal in a PoP package with Processor & Memory chips communicating at a Clock Rate of 533 MHz (current max.) and delivering a bandwidth of 2 GB per sec

Some oscillations at both logic “high” and “low” levels but still usable for digital operation

Baseline PoP can't deliver 12.8 GBps



LP DDR 2 memories at Clock Rate of 800 MHz (needed for Bandwidth of 12.8 GBps) : a severe degradation of waveform (Input : Rectangular but Output : almost Sinusoidal) & unstable logic levels at input buffer

Degradation due to the parasitics contributed by both I / O Buffer on die and Package interconnect

even for LP DDR 3 (input buffer with lower capacitance) : Waveform "borderline"

"Magic" chip with Active devices inserted into PoP

Instead of pursuing the **conceptually simple but physically complex route of TSV s and tight vertical stacking of dice** to reduce interconnect length and thus control Package parasitics, we introduce the **novel concept of compensating for Package Parasitics by inserting low – cost Signal Conditioning** into the interconnect, including long ones**.**

The required Signal Conditioning is implemented in a **"Magic" Chip** which caters to a large number of interconnects (> 100 no.s) at a pitch as low as 300 um.

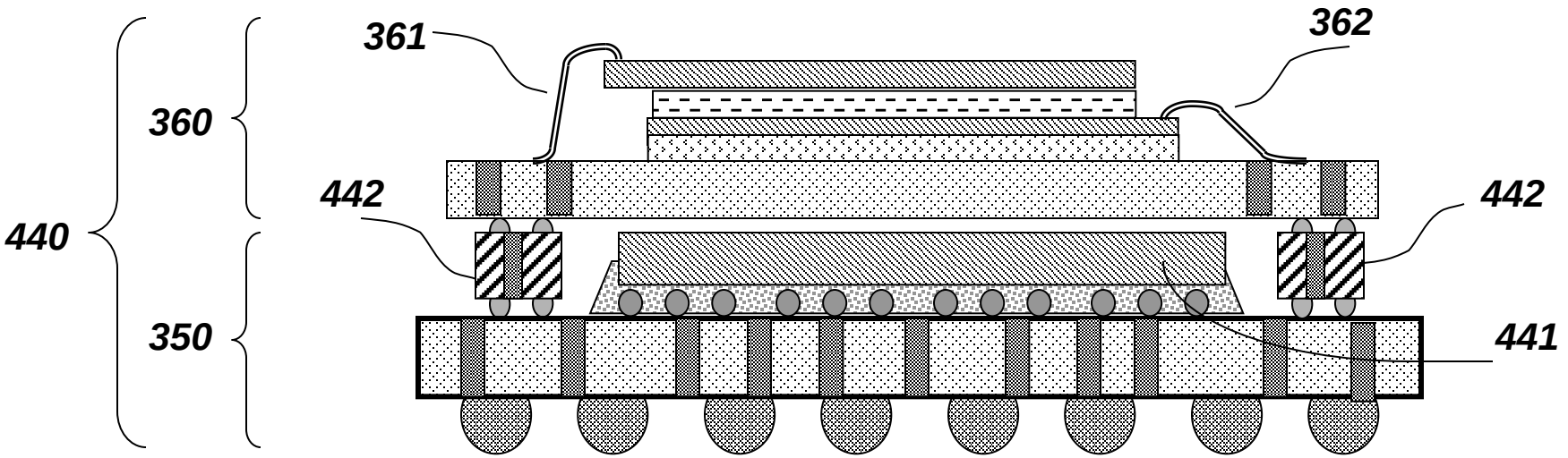
Magic Chips can be inserted, one a side, into the **periphery of a traditional PoP package** to improve their Bandwidth and Power Efficiency.

As ea. Magic Chip can cater to a large number interconnects, even a **traditional 14 mm PoP package** modified with them would provide enough vertical interconnects (approx. 500+) needed for 4 channels of 32 - bit memory and non – multiplexed 30 - bit wide memory bus to attain **parity w/ Wide I/O in terms of Bandwidth as well as Power Efficiency**.

The use of **Magic Chips allows side – stepping the problems of the TSV route** (the still immature process of drilling TSVs into already finished wafers, electrical performance issues of dice with TSVs due to heat and stress once they are stacked).

Three (3) different device technologies (all commercially available) are being pursued to build the Magic Chip.

Baseline PoP with " magic" chip inserted

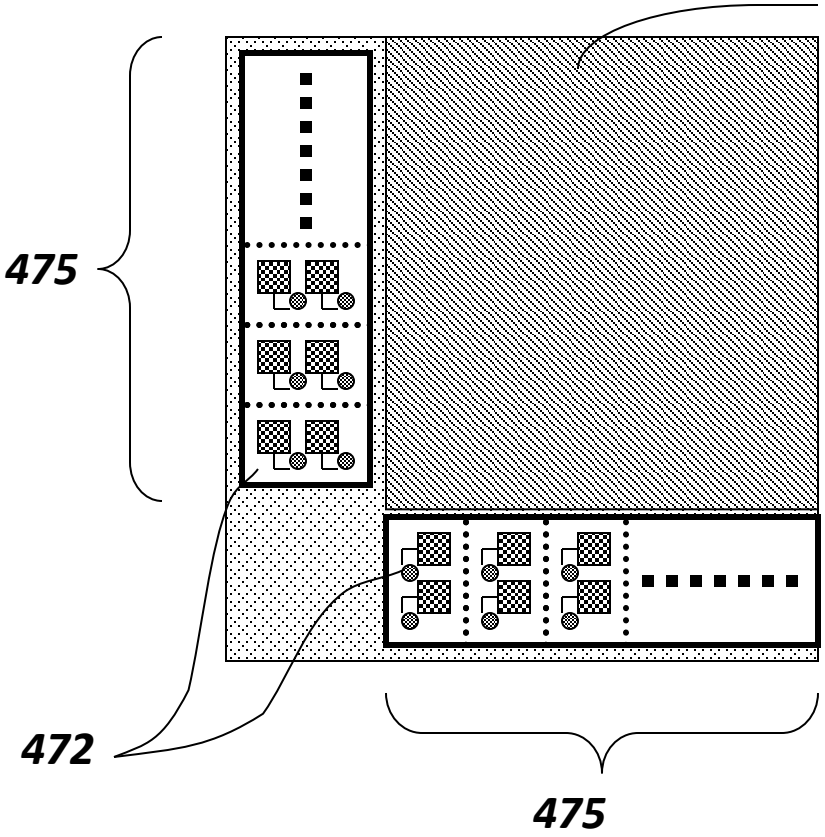


Item 442 is "Magic" chip with compensation features

Inserted between top and bottom layers of PoP, replaces the traditional vertical interconnect (solder) in baseline PoP

In this case the "Magic" chip does have TSVs, but TSVs with only coarse pitch (0.4 or 0.3 mm) of a low aspect ratio (1:7) or even PTH will suffice !!

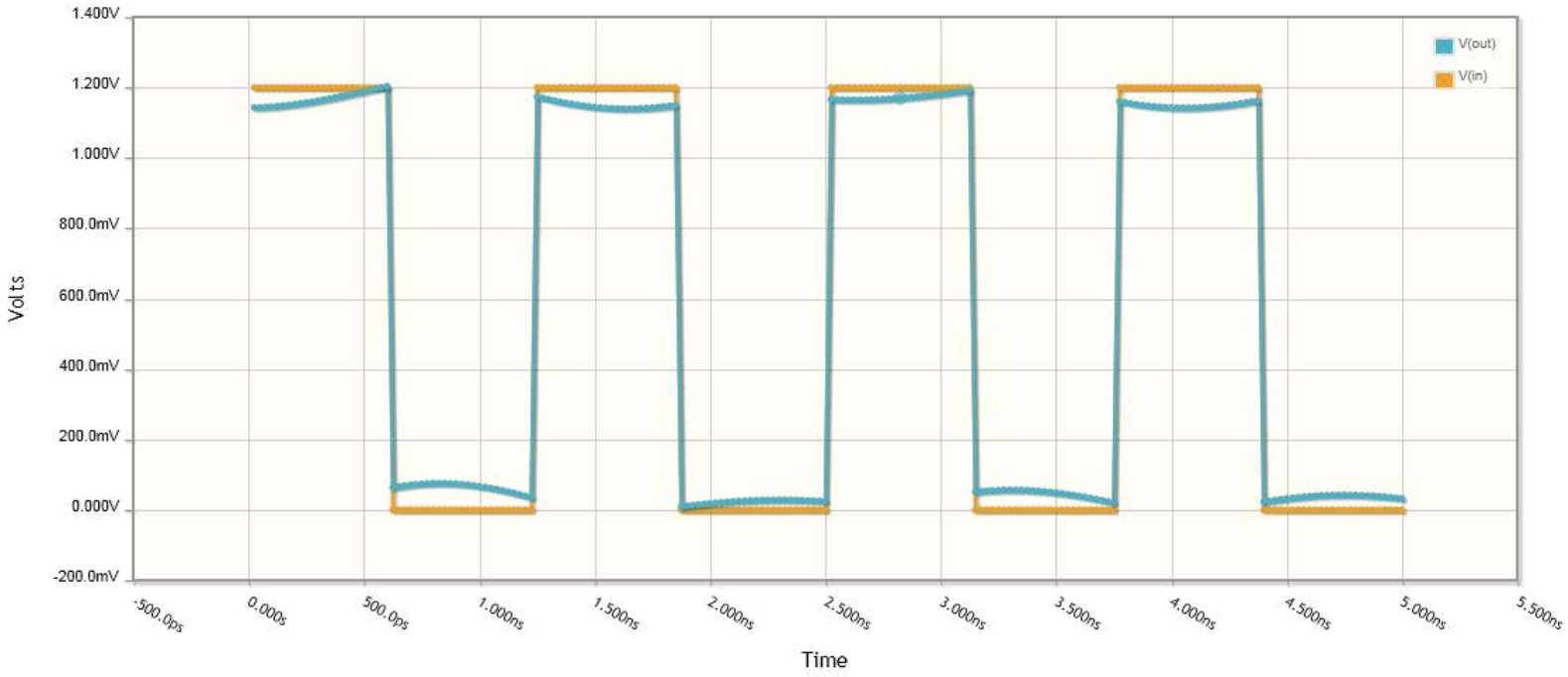
Baseline PoP with " Magic" chip inserted (Plan view)



Compensation features (# 472) for ea. Vertical interconnect in PoP

Width of "Magic" chip is 0.8 mm (leaving enough room for underfill fillet in a 14 mm sq. PoP w/ a 10 mm sq. SoC)

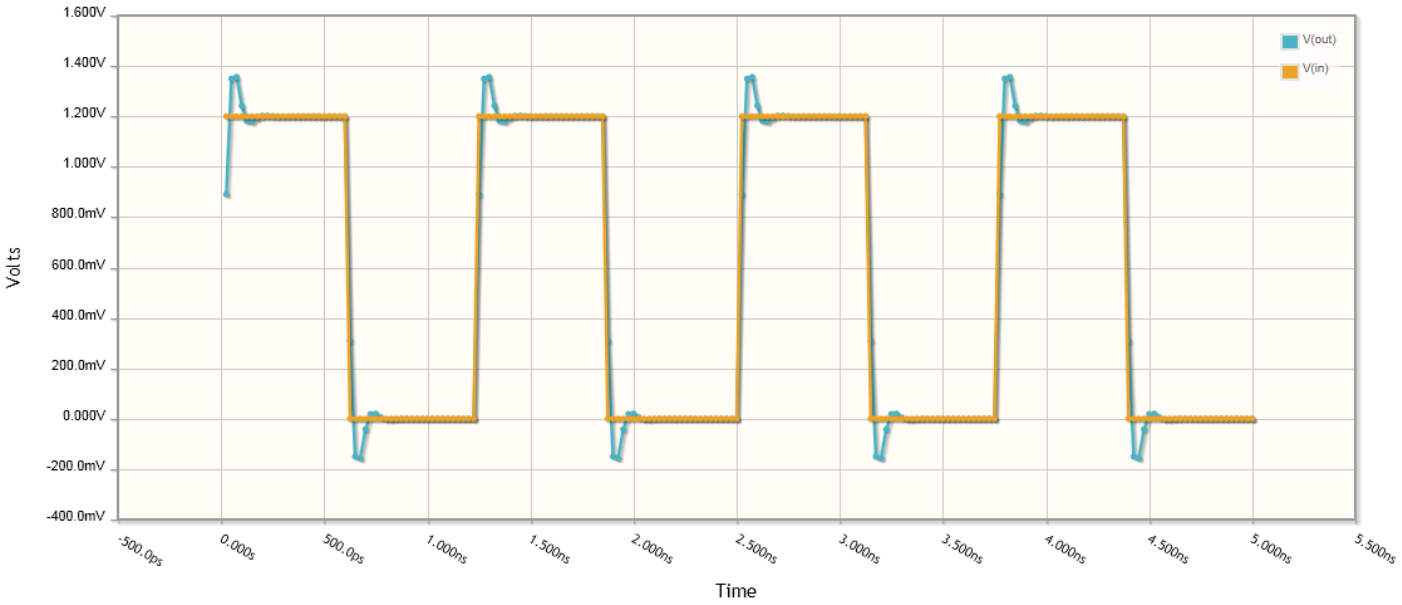
"Magic" ?!* Device Option 1



At 800 MHz LP DDR 2 would deliver the bandwidth (12.8 GB per sec) & power efficiency of a 3D – TSV package with Wide I/O.

With the addition of "Magic" chips, even a traditional PoP with Memory bus limited to 64 - bits width (2 x 32 per Chn) can compete with wide I/O w/ TSVs at 200 MHz

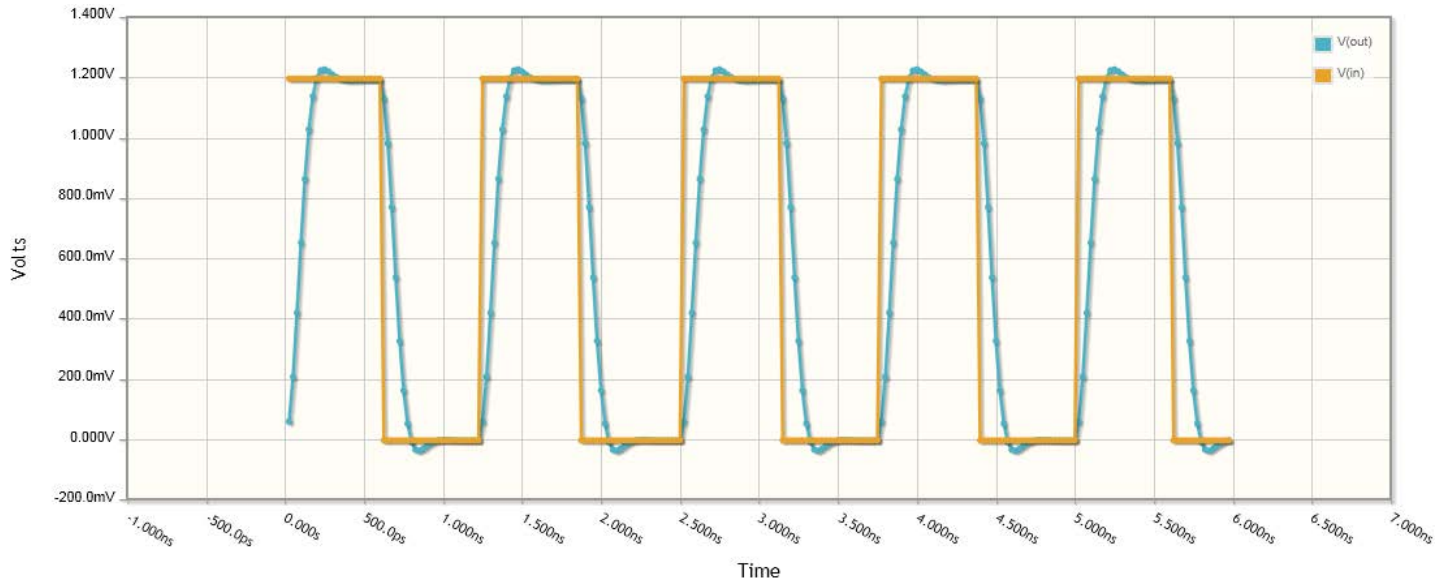
"Magic" ?!** Device : Option 2



Output waveform (" in Blue ") at 800 MHz of a PoP Package improved by inserting "Magic" Chip Option 2.

Now even a PoP package with SoC and Memory chips can deliver a Bandwidth (12.8 GB per sec) & Power Efficiency of a 3D – TSV package with Wide I/O.

"Magic" chip Option 3 : simpler, lower cost



- Simpler components, easier to implement w/ a variety of technologies, cheaper
- Compared to Options 1 and 2 somewhat slower transients (at 800 MHz a Rise Time of 170 pSec)
- Power Loss in Package Interconnect can be reduced by up to 70 % (model)
- Measured Power Dissipation due to Package Interconnect Parasitics in off – the shelf Smart Phones exercised I/O by Software, measured Battery life (compared Smart Phone Modified w/ Option 3 vs Baseline) : Power Loss in Package reduced by 55 %

Conclusions

- Development of complex Technology approached from first principles and modeling (rather than continuing complex Process Development) so as to define simpler & elegant solution
- PoP with " Magic" chip (any of the 3 Options) would not require TSVs in the functional chips themselves, thus side-stepping the issues of TSVs and 3-d stacking of active dies
- Simulation shows "Magic" chip approach (Options 1 & 2) would deliver the Bandwidth and Power Efficiency of Wide I/O with TSVs
- Magic Chip Option 3 is simpler & cheaper and would deliver 70 % of savings possible with "costlier" Options 1 & 2
- Early " proof of concept " testing using "homebuilt" Option 3 shows 55 % of expected Power savings
- Builds in progress, validation to follow
- Magic Chip approach applicable to 2-d modules as well, especially those with long interconnects on "lossy" substrates