POL and LDO for Harsh Environment Applications

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Abstract

Harsh Environment approved components/ designs require high reliability as well as availability of power to meet their system needs. The paper will explore the various design constrains imposed on the high temperature designs. Down hole oil and gas industry requires high reliability components that can withstand high temperature.
Discrete component selection, packaging and constrains imposed by various specification requirements to meet harsh environment approval are critical aspect of high-temp designs. High temperature PCB material, PCB layout techniques, trace characteristics are an important aspect of high-temperature PCB design and will be explored in the article. Buck Converters are the basic building blocks, but in order to meet system requirements to power FPGA's where low output voltage and high currents are required. Converter must be able to provide wider step down ratios with high transient response so buck converters are used. The paper with explore the various features of a buck-based POL converter design. Low noise forces the need for Low-dropout (LDO) Regulators that can operate at high Temperatures up to 210°C. This paper will address the power requirements to meet system needs.

Key words: DC-DC Power Conversion, MOSFETs, High Temperature, controller, current mode control, LDO

I. INTRODUCTION

In order to meet power requirements of FPGA's for high temperature applications up to 210°C, DC-DC converters must comply with various standards that impose size and quality constraints on both discrete and integrated parts that can be used in a design. The design must be able to meet performance criteria imposed by high altitude and high temperature without degradation in circuit performance and still maintain high efficiency.

Field Programmable Gate Array (FPGAs) need to be operational at voltages as low as 1V for the core and 2.5V for the interface input output (I/O) circuitry. FPGAs continue to require the need to be operational at lower voltages and higher currents to meet their system needs. Some of the complex system needs are: rapid transient response, high slew rate, small foot print and a well defined power supply sequence.

Among the various circuit topologies that produce step-down conversion, one topology that has high efficiency and low component count, is the buck converter. This is the approach that will be discussed here.

II. EFFICIENCY

Efficiency is an important performance metric in system design. A high efficiency part has higher power available at the output to be delivered to the load and wastes less power as heat. Fig.1. shows a plot of output power versus efficiency improvement. As shown in Fig.1, if the system efficiency were to increase from 85% to 92%, the output power delivered to the load will increase from 40W to 80W while maintaining a fixed power loss.

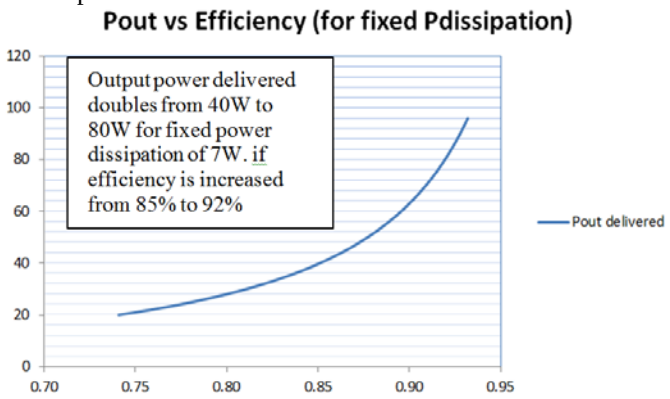

Fig.1. Output power versus efficiency improvement

III. SPECIFICATION CONSTRAINTS

In order for the final system to be small, most of the components must be integrated and at the same time provide the end-user the flexibility in selecting the operating frequency and the required compensation scheme.

In TPS50301-HT both the high side and low side MOSFETS are integrated in the integrated circuit. With large thermal PAD incorporated in the IC, thermal management is

kept in check allowing heat to be distributed evenly on the PCB thus leading to higher efficiency.

We must have the flexibility to operate at high frequency as it allows the magnetic component sizes to be reduced. This provides the end user the flexibility to make trade-offs between operating frequency/ size and efficiency to meet their system needs.

IV. BUCK CONVERTER TOPOLOGY

Shown in Fig. 2. is a typical synchronous buck converter diagram. The basic design contains five main components. These are the capacitor (C_{o1}), the inductor (L_O), the high-side switch (in series with V_{in}), the low-side switch and the Pulse Width Modulator (PWM). Each of these components has special requirements and different vulnerabilities to the environment.

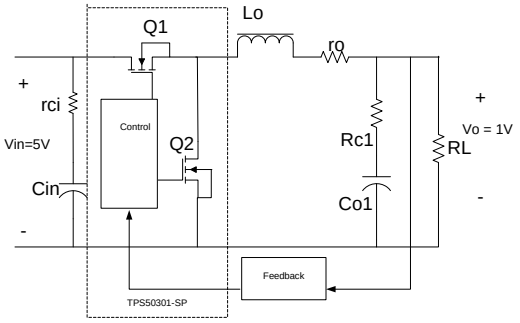

Fig.2. Synchronous Buck Converter illustrating the components. The switching frequency up to 1MHz

In some designs, an additional component such as a MOSFET driver is used to change the switch state rapidly. TPS50301-HT integrates all the basic components such as high and low side MOSFET's, drivers, PWM controller in a single device thus improving overall system reliabilility.

Inductor selection dictates that we use inductors that can support a high peak current and have low core losses. Ferrite cores are an excellent choice to meet these criteria. Ferrite cores are acceptable for commercial applications where ambient temperature is limited to a maximum of 85°C. For extended temperature range applications such as low altitude avionics where ambient temperature can be as high as 150°C inductors with iron and other composite material are available to meet the needs from various vendors. When we target even higher temperatures such as 210°C, then the choices get limited. Molypermalloy (MPP) cores with high curie temperature are an excellent choice for these environments. We must also select inductors that have low inductance value in order to meet fast transient response.

For V_{in}= 5V and V_{out} = 1V, a 1µH inductor was selected for the application making di/dt = 4A/µS. One drawback of having small inductor is that it will result in higher pk-pk ripple current, thus it will require low ESR output capacitor in order to meet the ripple voltage requirements. Trade-offs between inductor size, inductor cost, DCR of inductor, transient response and efficiency must be weighted out in selecting the inductor.

Small output inductor results in improved transient response, higher inductor current slew rate but at the expense of higher output ripple. Smaller output inductance will typically have lower DCR thus lower copper losses. Whereas larger output inductance value inductor will result in lower pk-pk ripple current and reduced core losses.

With the increased need for oil and gas in deeper wells, there is need of components that can operate at high temperatures. Downhole applications where the ambient temperature can be as high as 210°C, impose a different set of constraints on design. TPS50301-HT is designed to meet the high temperature challenge.

A non-synchronous buck converter is designed to operate in CCM mode in order to have lower peak currents in the switches.

1) Operating the non-synchronous converter in CCM mode results in higher inductance value.
2) Magnetic material must have high curie temperatures, and thus as the Mollypermalloy core (MMP) cores is selected. Toroid cores also help in Electromagnetic emission (EMI) as the flux in contained within the core and there is no fringing. Coating on the core is rated for 200°C. For high temperature applications, a magnetic core must be covered with Teflon tape, or use triple-insulated wire in winding the inductor.
3) For high temperature applications, the magnet wire must have a special coating to ensure high-temperature operation. PYRE-ML wire enamel, based on polyimide material is thermally stable up to 240°C [5].
4) Capacitors also must be selected that are rated to operate at high temperature, Ceramic capacitors from a number of vendors i.e. SMX or THH series from AVX is one such choice.
5) Tantalum capacitors can provide higher capacitance per unit volume. However tantalum capacitors must be de-rated with regards to its voltage rating. However Manganese Oxide (MnO2) based tantalum capacitors must be de-rated down to 33% of its rated voltage. Thus a 10V capacitor can only be used up to 3.3V when operated at higher temperature.
6) THJ series with extension to 200°C is one such tantalum capacitor that can be used in high temperature environment.
7) For resistors used in high temperature/ harsh environment down hole applications end of life tolerance is critical, as it dictates the stability of the part over temperature.
8) For high temperature applications, semiconductors such as MOSFETs and Diodes must be packaged in ceramic packages. Even though the silicon chip (Die) can operate at higher temperature, plastic package will degrade when subjected to excess of 200° C temperatures.
9) Plastic packages are rated up to 175°C temperature for automotive applications. For higher temperature, plastic package is subject to moisture absorption, and can result in popcorn effect and thus reduced reliability.
10) For operation at 210°C parts are packaged in ceramic packages, thus providing a reliable solution.

11) Precaution must be taken when using schottky diodes in high temperature environment. As the leakage current on schottky will double for every 10°C rise in temperature.
12) Ultra fast diodes with higher voltage rating are typically selected for high temperature applications, as the leakage current is significantly less at the operating condition that the part is subjected to.
13) Silicon die can operate at 210°C reliably. However in conjunction with ceramic package the part can work reliably at higher temperatures.
14) Lifetime of design in high temperature applications is typically 1000 hours maximum and can be as low as 200hours. Lifetime of the design at high temperature is dictated by the life of discrete external components such as wet-tantalum capacitors.

Various PCB materials such as FR4 are flame retardant and have a glass transition temperature up to 180°C. For high temperature applications, polyimide laminate material is used. Polyimide has high glass transition temperature up to 260°C. It also has lower z-axis coefficient of thermal expansion that allows higher aspect ratio holes to be plated and processed.

The solder material used for typical applications (Pb85 Sb10 Sn5) that is 85% lead, 10% antimony, and 5% tin that is solid at 245°C and liquid at 255°C. However for lead free high temperature applications, Sn95 Sb5 material, that is 95% tin and 5% antimony is used (solid at 232°C and liquid at 240°C) [3].

Another important consideration at high temperature applications is solder-joint mismatch between components being used. The coefficient of thermal expansion (CTE) between components and PCB is a critical factor that can result in failure at high temperature, especially during temperature cycling. Component leads comprised of kovar, which is iron-nickel-cobalt, provide thermal expansion comparable to ceramic. Thus using a gull-wing-shaped leads provide compliance or flexibility to the component, thus extending component life under high temperature applications [3].

Electromigration is another important aspect that affects the reliability of devices at high temperature. Electromigration (EM) is the transport of material caused by the gradual movement of the ions in a conductor due to the movement transfer between conducting electrons and diffusing metal atoms. Major Electromigration (EM) failure modes are voiding and extrusion. Void failure along the line can result in breaking of the line. Once Voiding has started it causes the current density to increase in the vicinity resulting in current crowding. Current crowding results in localized heating resulting in failure.

Once the stress in lines is greater than void formation, it results in diffusive displacement at the terminals that can destroy electrical contacts and this is referred to as extrusion.

V. PCB LAYOUT

Switching power supplies generate radiated and conducted electromagnetic emission (EMI). With fast varying voltage and currents that are characteristics of switching power supplies proper layout is critical in any switching converter. It is best to stop or minimize the noise at the source rather than try to shield it at the receiver end.

A poor layout not only leads to unwanted voltage and current spikes but also results in generation of EMI that must be addressed at the system level.

PCB traces have resistance, self inductance, mutual inductance and capacitance to the adjacent traces. Ground plane can be referred to as reference if there is zero current flowing thru it. If there is any current then, there will be voltage drop gradient in the plan. If there are two circuits connected on the plane then they will see different reference potential. Thus it is critical to keep noisy ground current out of system ground plane.

First thing in proper layout is to identify the source of noise. Loops of high di/dt should be identified and ensure that the loop area is kept small to reduce inductance. Source current and return should be on top of each other or adjacent to each other in order to minimize the loop area. With the current flowing in the trace it generates magnetic fields, thus reducing loop area reduces inductance and unwanted voltage spikes.

Loop area is composed of input capacitor, Q_1 and Q_2 .As large currents are switched when Q_1 is switched during on time, the loop comprising from C_{in}, Q_1 to switch node is high di/dt loop area. Similarly when Q_1 turns off, and Q_2 is turned on current flowing in Q_2, C_1 return, Q_2 to switch node is again a large di/dt loop area. Thus it is critical that loop comprising of C1, Q_1 and Q_2 should be as small as possible with C_1 return being tied to Q_2 source. Since Q_1 and Q_2 are integrated in the TPS50301-HT package this loop is optimized. However routing of Sync MOSFET (Q_2) source to input capacitor return is critical in minimizing the high di/dt loop area.

High impedance node such as switch node (junction of Q_1 source, Q_2 drain and output inductor) will cause electric field which can be addressed by firstly keeping the switch node area as small as possible. Adding a low impedance trace such as ground trace or plane between the source generating noise and critical circuit picking up the noise minimizes the EMI generation area. Low impedance trace should be tied to switch node return path.

For high temperature applications, copper traces should be made as large as possible, minimum recommended trace width should be 30mil where possible [6].

Control circuitry with its associated components should be kept away from power ground. Isolating the control circuitry on an isolated ground and then tying the isolated ground to the rest of system at one point is preferred [7].

Feedback resistors should be placed physically placed close to the feedback pin.

Vias are important for high current applications and are used to parallel multiple layers. Vias should be filled with solder or thermally conductive via filler compound. This helps in taking heat away from the IC. However, main

drawback of thermally conductive via filler is the coefficient of thermal expansion (CTE) between fill material and the surrounding laminate material. This may cause fracture between pads and hole walls. Note copper alleyways in the direction of current flow should be left between then as shown below. Improper use of vias can turn them into antennas and or raise the return path impedance.

Enclosed magnetic structure reduces flux fringing that can result in EMI generation.

Second Layer should be a solid ground plane that can be used as high DC current path. High di/dt current paths and analog ground should be kept out of this plane

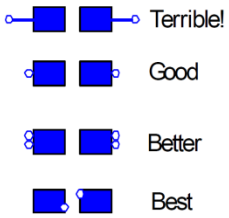

Fig.3. Bypass capacitor highlighting reduced inductance and loop area

Minimizing inductance is critical for high frequency bypass capacitors to work effectively. Long thin traces connecting to bypass capacitors introduces inductances thus isolating bypass capacitor from the load. Whereas minimizing the inductance by placing via's on the inside of capacitor pads provides the optimum solution, as the loop area is minimized. Though surface mount components are used where feasible due to size of the component. In order to meet shock and vibration thru-hole components are generally preferred.

As switching frequencies increase, it becomes more critical to use proper measurements techniques to ensure data measured is accurate and reliable. Using a Tektronix probe tip (often referred to as a cold-nose probe) for output noise measurements provide reliable and predictable measurements. This measurement technique ensures that the ground loop is minimized [4].

VI. CONTROL METHODS

The Pulse Width Modulator (PWM) provides control and regulation in the buck converter. The requirement for the PWM is to provide sufficient current with fast rise/fall times to quickly change the state of the upper and lower switches.

Various control Schemes are employed in typical buck converter designs, namely (VM) Voltage Mode, Current Mode (CM), Hysteretic and Constant-on-time (COT) control.

Current mode control is the most favored since it allows simple loop compensation, MOSFET switch protection due to inherent short circuit protection and its inherent line feed-forward compensation.

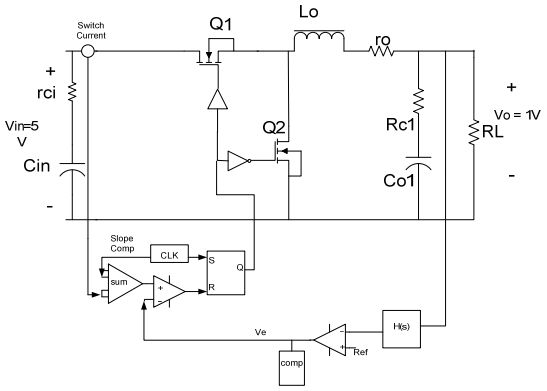

Fig.4. Synchronous Buck Converter with current mode control

Voltage Mode control forces output voltage to be equal to reference voltage and requires additional circuitry for over current protection.

Current mode Control is a dual loop system. It employs an inductor current feedback loop (inner loop) in addition to the output voltage loop (outer loop). It uses inductor current which is sensed at high side switch for TPS50301-HT and is compared to the control voltage which is the output of Error Amplifier derived from an output voltage error. Mode of operation is as follows: A clock input at the set terminal of RS Flip Flop initiates the switching cycle i.e. High side FET is turned on. When control voltage equals the sensed switch current high side switch is turned-off. Block diagram is illustrated in Fig. 4 [2]. When the high side FET turns on and the body diode of Sync FET turns off, a large reverse recovery current flows. (Reverse recovery results when the forward conduction diode is taken from forward to reverse bias.) This current can trip the PWM comparator. Thus a leading edge blanking is incorporated in order to prevent premature tripping of the PWM. A number of methods are incorporated in order to reduce the effect of reverse recovery such as by decreasing the slope di/dt by slowing down the turn-on time of the control MOSFET. This may reduce the reverse recovery but can results in higher losses due to slower turn-on of MOSFET. Another method will be to minimize the dead time, this can result in reduced reverse recovery by limiting the energy stored in body diode and associated parasitics. A method commonly used is to add a Schottky diode (which is a majority carrier device and has low reverse recovery charge) from Phase node to ground.

As duty cycle approaches 50%, current mode control exhibits sub harmonic oscillations. Thus a fixed ramp signal (slope compensation) is added to the current ramp signal to address the issue.

However, if too much slope compensation is added then current mode behaves like voltage mode control. This is due to the fact that current signal becomes a smaller portion of the overall signal and artificial ramp (slope compensation) masks the current signal. Thus it is important that adequate current signal is introduced in the circuit.

In Current mode control current signal is used to modulate the duty cycle. If the pk-pk ripple is small, then a small perturbation in control signal can result in big perturbation in duty cycle. This behavior makes current mode control

sensitive to noise. Thus the converter must be designed with a minimum pk-pk ripple current to endure noise immunity.

Current mode control is a single pole system. Due to current loop, the pole of the output LC filter splits into two real poles, thus resulting in output inductor pole to be at much higher frequency. The current loop monitors and controls the inductor current, thus forcing the inductor to act as constant current source. Thus loop remains as a single pole system regardless of the conduction mode.

Current mode control has an inherent feed forward path since inductor current ramp is a function of input voltage. Thus any change in input voltage immediately changes the modulator ramp slope and corrects the duty cycle without the need for the regulation loop to react.

Current mode control also provides ability to current share multiple modules, thus paralleling the output of two converters can be done easily without any additional circuitry, by simply connecting the compensation pins and sense pins of two converters together. Only one feedback control loop is necessary for the functionality.

Output overload protection can also be implemented by clamping the compensation pin.

VII. TRANSIENT RESPONSE

Step load on the output of a DC-DC buck converter is a means of evaluating the transient performance of the converter. FPGA can demand high current typically 20A/µS. Converters must be designed to address the needs by proper selection of

a. Output capacitors
b. Output inductor
c. Control Bandwidth

During transient response with high slew rate of 20A/µS the output capacitors provide the energy during this transition. Having excessive capacitors on the output is one option, but this requires more board area as well as added cost.

A number of factors dictate the response. Small inductor size will allow the inductor current to ramp up faster to the operating point demanded by step load.

Switching at higher frequency as well as having large cross over frequency (loop bandwidth). Typically one can increase the loop bandwidth as high as $1/6^{th}$ of switching frequency. But having larger loop bandwidth will result in circuit being more susceptible to noise pickup. Thus proper choice of crossover frequency is based upon meeting system specifications.

Besides the items outlined above another factor that can help in meeting the requirements is “dynamic bias” where the control loop causes the trans conductance amplifier to slew at higher rate in response to change in input of the amplifier. This has the advantage of providing improved transient response with lower output capacitance. TPS50301-HT incorporates a fast error amplifier (with dynamic bias). This has the same effect as if the loop gain was suddenly increased during transient conditions. As shown in Fig 5, a step change in input of error amplifier, output of error amplifier changes in non-linear fashion. Thus loop bandwidth is increased during step-load response, since error amplifier gain increases during transient conditions. Fig. 6, highlights the improvement in step load response using dynamic bias [3].

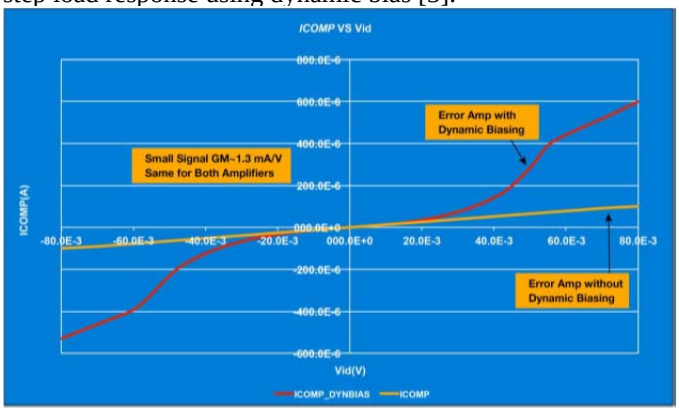

Fig.5. Icomp vs Vid comparison of error amplifier response with and without dynamic bias

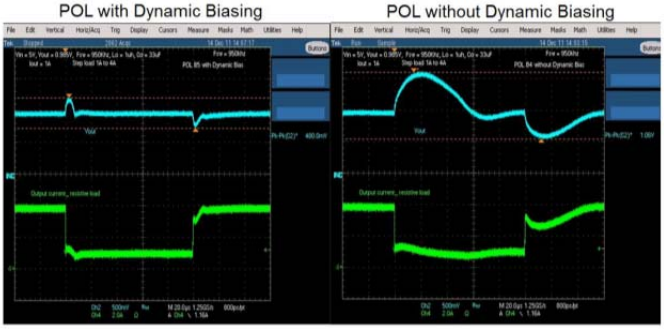

Fig.6. Improved transient response with dynamic bias

For higher power requirements, multiple TPS50301-HT POLs can be paralleled thus providing higher output current to meet system needs.

VIII. SYNCHRONIZATION

TPS50301-SP is capable of operating in Master / Slave mode. In this configuration RT pin is left open, internal oscillator is set to 500 kHz and SYNC pin is set as an output clock. Sync out signal level is same as V_{in} with 50% duty cycle. Sync out signal is in phase with the clock signal of the Master. Sync signal feeding the slave module which is in phase with the master clock gets internally inverter (180 degrees out of phase with the master clock) internally in the slave module [1].

With two modules out of phase with each other, it has the advantage of reduced input ripple current, thus the amount of input capacitor required is reduced to meet system requirements. TPS50301-SP can also be configured with external system clock. In this configuration the two modules can be synchronized with the external system clock. An inverter is required to invert the phase of one module. This ensures that the two modules are 180 degrees out of phase with each other. If no external clock signal is detected at the sync pin for approx 20usec, then TPS50301-SP transitions to its internal clock which is typically 500kHz. RT value of master and slave converter must be within +/-5% of the external synchronization frequency.

IX. OUTPUT VOLTAGE START UP

Monotonic rise of output voltage is a critical requirement for the FPGA's and ASIC's. FPGA's and ASICS can retain some voltage at shutdown. It is undesirable for the pre-existing voltage to cause the output of converter to droop during turn-on. One approach commonly implemented is to ensure that low side MOSFET (Sync FET) is disabled during pre-bias mode. Phase node of the converter is monitored during the off time of high side MOSFET. Controller phase detect circuit ensures that phase node stays below 0V during complete cycle of high side MOSFET off-time. Only then is the low side MOSFET (sync FET) allowed to turn on and start switching. However TPS50301-HT addresses this by monitoring the sink current in the bottom MOSFET. If the sink threshold is triggered, then bottom (sync) MOSFET is turned off for the rest of the switching cycle. Thus monotonic start-up behavior of the converter is guaranteed.

X. LOW DROP OUT REGULATOR (LDO)

For systems requiring low noise applications such as RF components, Receivers, ADC's where it is crucial that they be powered from a low noise supply. Low Drop Out regulators (LDO) that can operate at high temperatures are necessary to provide this clean supply. Typically, any linear regulator with a drop out voltage less than 1V is termed as LDO.In an LDO V_{out} provides feedback to internal error amplifier, where V_{out} is compared to the internal reference to modulate the pass element. Pass element for high temperature LDO TPS7H1201-HT is a P-MOSFET. P-MOSFET is typically selected as the pass element as it is easy to drive the V_{gs} to turn the MOSFET on.

Drop out occurs when V_{in} gets close to V_{out}. In drop out condition, LDO cannot regulate the output voltage anymore as V_{in} is decreased. TPS7H1201-HT P-MOSFET rds-on is typically 50mohm and package resistance is 25mohm. This allows one to achieve drop out voltage of 73mVolt at full load of 0.5A at 210°C.

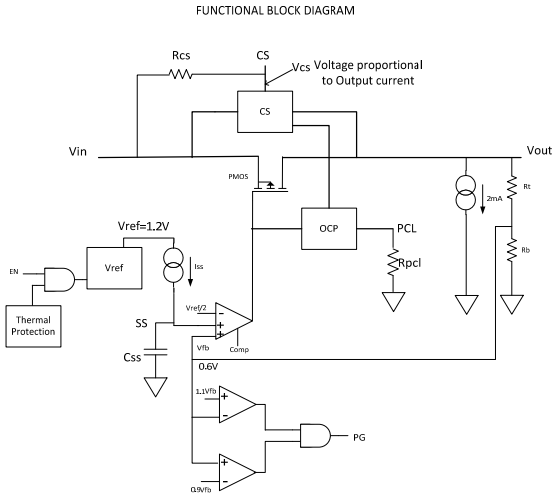

Fig.7. TPS7H1201-HT Low Drop Out Regulator (LDO) block diagram

TPS7H1201-HT is packaged in 16 pin ceramic package to operate at 210°C. Functional block diagram of LDO is highlighted in Fig 7. It incorporates a number of features.

1) Programmable soft start is implemented by selecting the value of Css.
2) High side current monitor – Voltage at C_S pin can be monitored to provide voltage proportional to the output current.
3) Power good functionality to provide indication of the status of the output voltage.
4) Programmable current limit. A resistor connected from P_{CL} pin to ground can set the current limit trip point. This provides overload protection.
5) Current fold back, with C_S pin tied high to V_{in}. It activates the fold back current limit. This results in reduced power dissipation during fault conditions.

Features highlighted above are incorporated to address system reliability when operating at high temperature device. Similarly over current protection with current fold back ensures that power dissipation in the device is reduced under fault conditions. Current sharing can be achieved by connecting programmable current limit (PCL) pin of LDO 1 to current sense (CS) pin of LDO 2 and connecting PCL pin of LDO 2 to CS pin of LDO 1. Thus daisy chain implementation can allow one to parallel multiple LDOs.

In current sharing mode it provides higher reliability (MTBF), with reduced stress on components. Heat is also spread over multiple devices thus resulting better thermal management.

High DC gain of the LDO ensures excellent line and load regulation. TPS50301-HT EVM Fig 8, showcases the high temperature solution incorporating TPS50301-HT POL along with secondary current limit followed by TPS7H1201-HT LDO to address high temperature applications.

Fig.8. TPS50301-HT (POL) followed by TPS7H1201-HT (LDO)

XI. SYSTEM LEVEL PROTECTION

Connecting multiple POL outputs in order to increase the load capacity is commonly achieved using schottky Diode to perform the "OR" function. Using an OR diode has its drawbacks mainly reduction in efficiency, thus most commonly one uses a MOSFET as an OR diode. In current mode control design multiple POLs can be tied together to provide higher output power. By connecting compensation pins and feedback pins together, two POLs share current, with one common feedback network.

If low side/ Sync MOSFET or output capacitor of buck converter were to fail short, then it will bring down the main output voltage bus. Thus having an OR function to isolate POLs from the main bus is necessary to provide high system reliability.

In buck converters one of the main concerns that the system architect has is to protect the load in case of high side MOSFET failure. If the High Side MOSFET fails shorts, then

input voltage will be present at the output, thus resulting in damage to the load such as FPGA. Thus there is a need to isolate the load from the active power source. Load Switch with active thermal protection is one such option.

Input level protections that is generally implemented at the system level are –

1) Reverse polarity protection, hot swap (controlling/ limiting the input charge current to the capacitor bank.
2) Having an electronic fuse at the input.

Features like input level protection as well as isolating POL from load under fault conditions are necessary, so the reliability of the system is not compromised.

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