Precision Analog Signal Conditioning Semiconductors for Operation in Very High Temperature Environments

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Abstract— **When designing signal chains for systems exposed to high temperature environments, analog signal processing ICs are needed to enable precision sensor measurements. However, as ambient operating temperatures increase beyond the typical extended-industrial +125˚C limit, the performance characteristics of analog semiconductors are strongly impacted by the effects of temperature on circuit design, packaging, and the underlying fabrication process. In this paper we introduce two new precision analog components, an operational amplifier and voltage reference, rated for very high temperature operation. We then discuss the steps taken to ensure their performance at high temperature is robust and can be maintained over a limited lifetime. Finally, we demonstrate these devices utilized in an example application: a constant current source for temperature sensor signal conditioning.**

Keywords—High Temperature Electronics; Signal Conditioning; Semiconductors; Operational Amplifier; Voltage Reference

I. INTRODUCTION

Building on the successful introduction of a high performance instrumentation amplifier designed specifically for high temperature operation [1], Analog Devices, Inc. (ADI) continues to develop components rated for operation at extreme temperatures. This paper introduces a new precision operational amplifier and voltage reference that demonstrate it is possible to take analog circuit intellectual property (IP) on suitable fabrication processes and, with enhancements for performance and reliability, characterize and qualify the new devices for operation at temperatures above 200˚C.

II. HISTORIC PERSPECTIVE

Since the early 1960s there has been a need for high temperature (HT) electronics for precision sensor measurements during oil drilling. There are also emerging applications for HT components in aerospace engine monitoring, industrial process controls, nuclear power plant control systems, and electric power conversion where both the sensor and the electronics are collocated in the harsh environment. All of these applications call for the kind of electronic components which are commonly available in the industrial temperature range operation. Unfortunately, most commercially produced components suffer from severely degraded performance and reliability at elevated temperature that can make them unusable. Historically, this led to specialized ICs designed for HT operation from the ground up, preventing the reuse of existing IP. From the component vendor's perspective, the investments required for these types of projects could be prohibitive given the size of the market.

Until recently analog designers in HT applications often needed to use commercially available electronics and self-certify them for operation beyond the absolute maximum rating, or select from the few HT rated ICs available from a handful of specialty vendors. Self-certifying commercial products is expensive and risk-laden: it consumes valuable engineering resources, increases time to market, increases chances of field failures and carries no guarantee of reliability. The cost of repair and downtime are high for most of these applications, so while this path was once popular due to necessity, it is certainly not desirable [2]. Some specialty vendors have more recently offered HT components tested and rated with useful lifetimes above 200˚C, however the selection of analog ICs is limited and mostly fabricated on CMOS processes that are not ideal for high performance analog signal processing.

Given the intensified downhole drilling activity in deep, HT wells and increased emphasis on more electronics in avionics systems, the need for HT electronics has never been larger. With advances in design, layout, fabrication processes, and packaging we can leverage proven high performance IP to develop the ICs needed to design robust systems for HT applications.

III. NEW HIGH TEMPERATURE PRODUCT DEVELOPMENTS

A. AD8634 Precision Dual Operational Amplifier

A conventional three stage topology was chosen for the AD8634 HT precision operational amplifier, which includes an input stage composed of NPN and PNP transistors, a folded cascode gain stage, and a rail-to-rail output stage, as shown in Fig. 1. This combination gives very good bandwidth and low noise without the need to burn a lot of power in the gain stage to achieve high open loop gain. This type of amplifier is versatile as it can solve many differing analog signal processing challenges with a single component, as evidenced in the specifications described in Table 1.

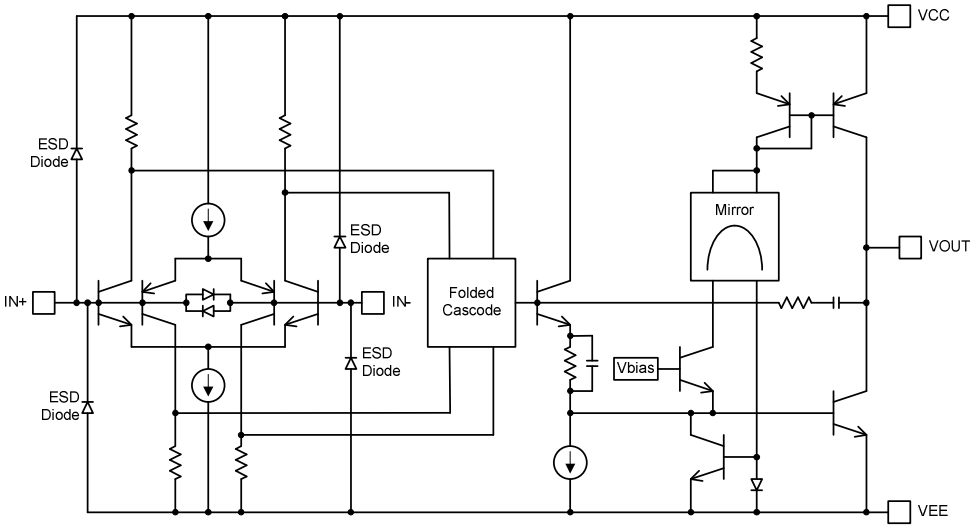

Fig. 1. Precision HT Operational amplifier Simplified Block Diagram

TABLE I. AD8634 OPERATIONAL AMPLIFIER KEY SPECIFICATIONS

Parameter	Value	Units, Conditions
Temperature Range	-40˚C to +175˚C -40˚C to +210˚C	SOIC Package Ceramic Flat Pack
Gain Bandwidth Product	10	MHz, Av=100
Input Voltage Noise	4	nV/√Hz (typ)
Input Offset	200	µV (max)
Slew Rate	2.5	V/µs
Supply Current/Channel	1.0 1.3	Vsy = ±15V, Ta = 25˚C Vsy = ±15V, Ta = 210˚C
Supply Voltage Range	3 to 30 +/- 1.5 to +/- 15	V
Unity Gain Stable		
Rail to Rail Output		

One disadvantage of this scheme is that it does require a relatively high input bias current which, depending on the application could require that upstream sources be of fairly low output impedance to minimize errors associated with the leakage. Typically analog designers would look to amplifiers with CMOS or JFET input transistors to remedy this problem. However, using these in a HT application does exact a toll on their performance; their input bias current are much more sensitive to temperature than bipolar. In practice at elevated temperatures the advantage swings to the bipolar design and so in this case an initial limitation becomes a benefit when considering the application.

When analyzing the performance of the amplifier over the wider temperature range compared to standard temperature ranges, the following effects are observed:

- The effects of Solder Heat Resistance, (SHR), which is the systemic change in the offset voltage of the operational amplifier with exposure to solder reflow cycles, increased at higher temperatures which increased the voltage offset specification.
- Offset voltage matching improves with higher temperatures within the specified common mode range
- Common mode rejection close to the rails decreases due to steeper turn off characteristics of the input transistors limiting the input voltage range
- Input bias current is highest at cold temperatures and lower at higher temperatures
- Maintain a minimum load of 10 kΩ or less on the output to prevent higher than expected supply currents

B. ADR225 Low Power, Low Drift Voltage Reference

The choice of the ADR225 voltage reference topology was driven by focusing on low power while still giving excellent accuracy, drift, and noise performance. Table II summarizes the key specifications.

TABLE II. ADR225 VOLTAGE REFERENCE KEY SPECIFICATIONS

Parameter	Value	Units, Conditions
Temperature Range	-40˚C to +175˚C -40˚C to +210˚C	SOIC Package Ceramic Flat Pack
Temperature Coefficient	10 ppm/°C 20 ppm/°C	SOIC Package Ceramic Flat Pack
Output Current	10	mA
Supply Current	35	µA
Initial Accuracy	+/- 2	mV
Drop Out Voltage	1.0	V
Voltage Noise	25	µV p-p

The reference was designed for low power; see the simplified block diagram in Fig. 2. One way to measure the power efficiency of a voltage reference is to simply count the number of current paths from the positive power supply terminal to ground at the schematic level; this is not possible in Fig. 2 but at the schematic level there are only four paths total

for this design. It consists of a Bandgap Cell/1st Gain Stage, 2nd Gain Stage/Level Shift, Output Driver, and a Start-up circuit.

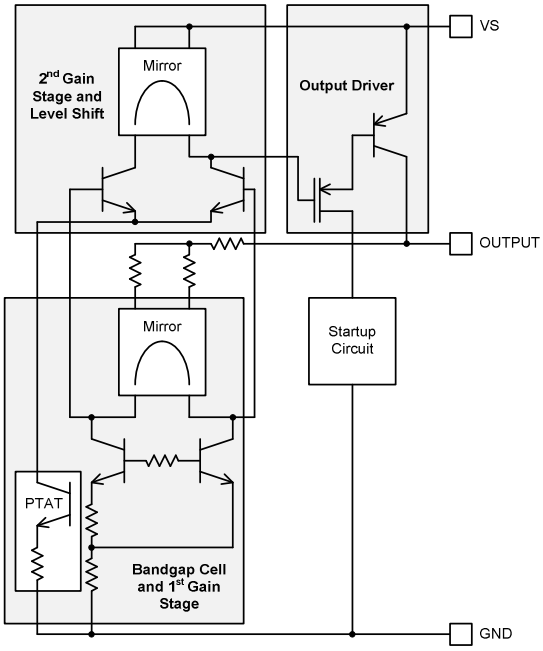

Fig. 2. Precision HT Reference Simplified Block Diagram

The Bandgap Cell/1st Gain Stage is composed of five identical transistors (three shown): two are arranged as a Brokaw-Bandgap voltage cell, two are a matching set to correct for the substrate-collector leakage of the bandgap transistors, and one is a Proportional To Absolute Temperature, (PTAT) current source with which to control the gain of the second stage in order to make it more immune to temperature changes. The current mirror in this block is ideal for input bias current compensation of the bipolar transistors and makes an ideal driver for the 2nd Gain Stage/Level Shifter. It also provides the first stage of line regulation to help make the output stable over changes in power supply voltage.

The 2nd Gain Stage/Level Shifter uses a differential current mirror approach to take advantage of the matching of currents while providing a single-ended output to drive the Output Driver. This design is used to further enhance the power supply rejection of the reference due to the fact that both sides of the mirror track with the power supply voltage. The Output Driver is sized to provide the needed 10 mA output current capability at 210˚C while being matched to the capabilities of the 2nd Gain Stage Current Mirror.

The Start-up circuit provides the infrastructure to ensure proper operation without latch-up at power up.

The design also provides all the necessary features to make a complete voltage reference system: components for curvature correction of the bandgap, output current limits, short circuit protection, and zener/laser trimming for accuracy.

When analyzing the performance of the voltage reference over temperature, the following effects are observed:

- The effects of SHR widened with the higher temperatures so that the initial Vo accuracy spec was widened
- The load regulation at high temperature required a wider specification
- Output load current is limited to 10 mA at high temperature to reduce the potential for electro migration failures
- Supply current increases proportionally to temperature at a rate of about 0.14 µA/˚C

IV. Technical Advances That Enable HT Solutions

There are multiple considerations to operating silicon-based analog integrated circuits at elevated temperatures that must be addressed in order to maintain performance. Not to be ignored is reliability over the lifetime of the devices. We will examine the following aspects of the HT design and process flow as they relate to the new HT amplifier and reference:

- Product Definition
- Design
- Process
- Layout
- Packaging
- Interconnect
- Characterization
- Qualification / Reliability Testing
- Production Testing

A. Product Definition

For ADI's first HT precision operational amplifier several topologies were considered and, after consulting with customers, flexibility in solving a wide variety of problems was prioritized as one of the selection criteria in order to supply a precision operational amplifier that would be useful in the widest range of designs. This lead to the definition of the AD8634, a precision, low noise, moderate speed bipolar operational amplifier with wide input voltage range and rail to rail output capability.

A similar thought process was used to pick the target for the voltage reference as well, with an emphasis on low power consumption. Compared to the operational amplifier, a reference serves a more fixed function and we do not need to balance as many trade-offs. We focused on low power applications concerned with long battery life and low self-heating resulted, which resulted in the definition of the ADR225: a device that consumes only 10% the supply current of the competitive offerings while still offering excellent drift, accuracy and noise specifications.

B. Design

The design choices made to produce a new commercial analog IC are generally driven by a product definition as discussed above. There are many choices to be made in "features" such as rail-to-rail input/output, zero-drift, and other options that drive the design of the operational amplifier into various topologies that are further linked to the process choice. Parametric performance also factors into the design choices that must be made because certain relationships cannot be altered without choosing a different process or topology. For example, there are inherent links between the speed of an operational amplifier and the supply and noise. To make a design faster, within a given process and topology, more supply current is required which also results in lower noise. The speed is proportional to supply current so that doubling the supply current roughly doubles the slew rate and bandwidth while the noise is a square root relationship requiring a 4X increase in supply current to cut the noise by one-half.

C. Process

The product definition also drives the choice of process which has a profound effect on how the device performance varies over temperature. Analog Devices' designs analog ICs in CMOS, Bipolar, and Silicon Germanium processes with a variant of the bipolar process offering JFET transistors used as the input transistors for operational amplifiers. For operational amplifiers a FET input transistor offers an advantage in lower input bias currents compared to a bipolar input transistor. However, the downside of a FET input is that their input currents generally double for every 10˚C rise in temperature. The result is that by 125˚C they have little advantage compared to the bipolar input transistor whose bias current is decreasing with temperature.

For the AD8634 HT operational amplifier, a bipolar process was used based on the factors identified in the product definition. The process is a variant of our production HVBP2 using Silicon-on-Insulator, (SOI) as a starting material. SOI reduces leakage currents to the substrate, improves latch-up immunity, enables higher speed/power ratios, and offers other advantages needed by a precision operational amplifier that derive from a fully dielectrically isolated process. Fig. 3 shows a cross sectional diagram highlighting the differences between NPN transistors in both full dielectrically isolated (SOI) and junction-isolated (non-SOI) processes and the resulting leakage paths for both. When designing a high performance, precision operational amplifier minimizing and eliminating these leakage paths is a critical advantage as many of them tend to get worse with temperature. The use of SOI for the AD8634 makes it possible to achieve a level of capability not easily duplicated otherwise.

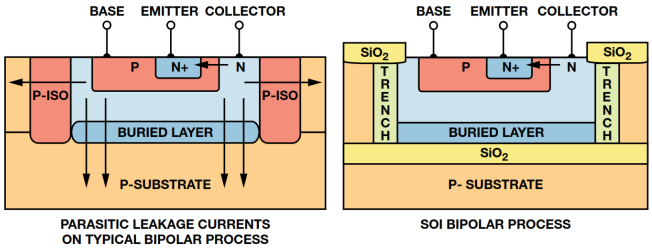

Fig. 3. Junction Isolated vs SOI NPN Transistors

For the voltage reference an established Complementary Bipolar CMOS process called CBCMOS2 was used, see Fig. 4 for an example cross sectional drawing of isolated PMOS and NMOS transistors. This process was used for a variety of reasons including the fact that the reference does not need 30V capability, so the performance limitations of a high voltage process can be avoided. A Bi-CMOS process was needed in order to have good analog performance in both Bipolar and CMOS transistors.

Normally a 5V MOS transistor must be kept within 5V of the substrate which limits the capability of a reference when trying to tolerate a wide range of input voltages. With the isolated pocket approach shown in Fig. 4 the operating voltage of the transistors can be isolated from the substrate and from other transistors operating at a lower voltage. This enables a high voltage and low voltage section to operate simultaneously on a single, monolithic substrate such as the ADR225 uses.

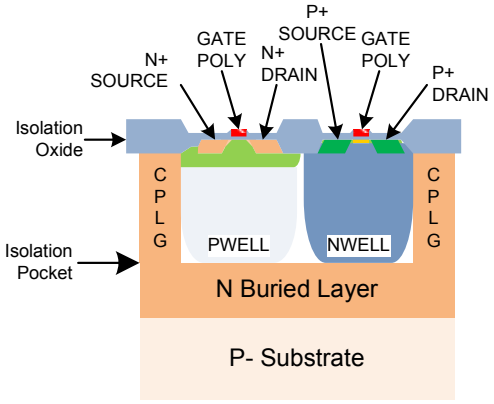

Fig. 4. Example of an Isolated PMOS/NMOS

The leakages associated with a non-SOI process are not as detrimental to the operation of a voltage reference as they are for an operational amplifier; the precision of an operational amplifier can be as high as three orders of magnitude better than that of a reference. Reference drift is compensated with the on board PTAT circuit. This process also provides thin film resistors, (TFR), and zener zap capability for in-package trimming and setting the reference to the needed operating parameters.

One final comment on process choice for these components is that they both use TFR to provide the required accuracy. TFR's superior precision, matching, and thermal drift performance cannot easily be replicated with the typical diffusion and poly resistors available to other capable analog

processes, it could be said that one of the ways to tell if a process is capable of precision analog would be the presence of TFR as an option. TFR also provides for the laser trimming needed to make fine adjustments. The TFR used in these components is proprietary to ADI and is used on many of our ICs where there is no better alternative to obtain the necessary precision, thus this is an enabling technology.

D. Layout

The physical arrangements of the transistors, capacitors, resistors, metal traces, vias, and other elements of the design, called the "layout," can have a profound effect on the parametric performance of the design and the lifetime of the device operating at high temperature.

1) Location and Layout of Stress Sensitive Devices

During the layout of a precision analog IC it is critical to place the input transistors with in order to achieve the needed precision and eliminate potential errors sources that could adversely impact the specification performance over temperature. The layout of the input transistors is key to getting good initial offset and low input bias current while keeping the temperature drifts to a minimum. Many of the best practices used are common sense but most of them come from experience gained over the design of many products all with their own lessons to teach. Some of these best practices are to minimize mechanical stresses of the packaging and board mount, some to minimize drifts associated with temperature, and some of them are used in the reference as well where component matching matters. The techniques used in the AD8634 represent the latest practices used at ADI for precision, rail-to-rail bipolar transistor operational amplifiers.

2) Matched Devices

The input transistors are made up of many individual, multi emitter transistors laid out in stripes to minimize die area while maintaining good matching characteristics. This is not just for cost reasons but also keeping the die area small minimizes the mechanical stresses on the components. The multi-emitters also keep the emitter current spread throughout all the stripes to ensure even current density throughout the entire transistor resulting in a predictable current gain for the device as a whole.

The layout of the individual transistors is only one aspect of matching; the other is how they are arranged when interconnected to form the input pairs of an amplifier. Fig. 5 shows two layout examples for comparison. The top one is in a parallel arrangement which is used to save die area but which results in inferior matching when process variation, thermal stress, and mechanical stresses are considered. The bottom one is a "cross-coupled pair" [3] in which the variations are better matched and cancelled out.

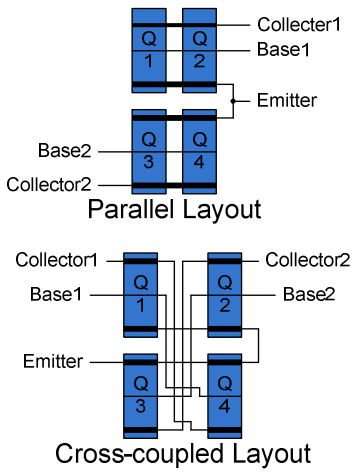

Fig. 5. Matched Device Layout Examples

3) Thermal Centerlines

All matched circuit components are laid out so that they have the same aspect ratio with the long axis kept parallel to the thermal centerline of the die. This is to keep any heat gradients generated uniform to both structures so that any heating effects are cancelled by summation of equal but opposite errors. This comes from the elementary relationship between the V_{BE} of bipolar transistors that for a 1°C difference in temperature will result in a 2 mV change. Going further, the inputs are designed such that they are kept as far away as can be from the output stage (of either channel) to keep thermal effects of the outputs from impacting the input offsets.

Fig. 6 shows two example layouts one where the thermal centerlines are not balanced (upper) and the other where they are balanced (lower). In the case of an unbalanced layout the resulting amplifier design would exhibit a high level of thermal drift. Additionally, the inputs of one channel are closer to the output of the opposite channel which generates a "thermal cross-talk" condition where the offset of one channel is influenced by the output loading conditions of the opposite channel.

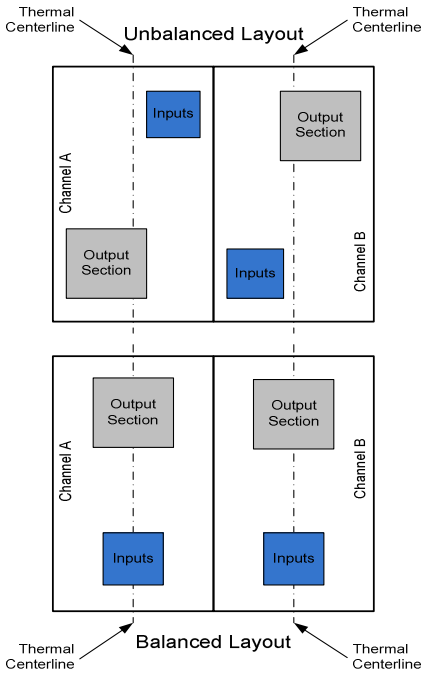

Fig. 6. Thermal Centerline Layout Examples

4) Matched Metal Traces

Resistive drops known as I^2R losses occur anytime current flows through a non-ideal conductor like the metallization used in IC manufacturing. Keeping the drops consistent throughout the input stage of the device is another key to good precision and matching. The critical currents are not so much the input to the base, but the higher currents of the collector and emitter of the transistor. These should be matched so that, again, we get cancellation of errors by summing of equal but opposite magnitudes. Fig. 7 shows two examples that describe the simplified metal trace routing for the collectors and emitters of two NPN transistors that are to be used as the inputs for a precision operational amplifier. The upper diagram shows the routing impact that minimizes die area at the expense of matched metal routing. The lower one shows the routing for a high precision matched metal trace arrangement.

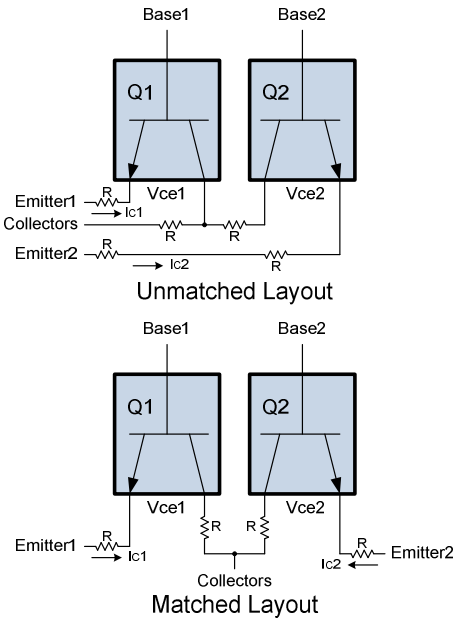

Fig. 7. Matched Metal Trace Layout Examples

If the inputs are balanced ($V_{IN+} = V_{IN-}$) and the devices are perfectly matched so that their current gains are equal, then the base currents should be equal as well and the resulting emitter currents will be equal. However, in the unmatched case the collector-to-emitter voltages (V_{CE}) are not equal as the voltage drops through the metal traces to Q2 includes additional resistance and therefore voltage drop. In the matched layout the routing is of equal length for each connection and so the voltage drop associated with the current flowing in the traces are equal.

5) Metal Plating As Protection from Mechanical Stress

In the AD8634, JFETs are used as a non-critical startup circuit current source. JFETS are large surface devices that can act like a strain gauge which would negatively influence offset and drift specifications. This could introduce overheating of other components if the resulting currents became too high which could shorten device lifetime. By putting upper level metal above the gate-channel region of the JFET, held at the gate potential, provides a mechanical protection to minimize the surface stresses transmitted to the top of the JFET and a Gauss shield to prevent capacitive coupling of stray signals to the gate of the JFET. Fig. 8 shows a cross sectional drawing of a typical JFET without the top gate. Fig. 9 shows the same drawing but for a JFET with the top gate metal and Fig. 10 shows the top view of the corresponding layout.

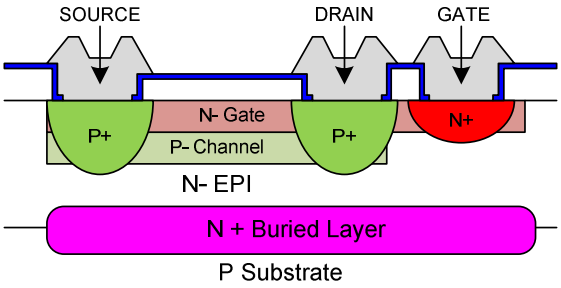

Fig. 8. JFET Cross Section without Top Gate Shield

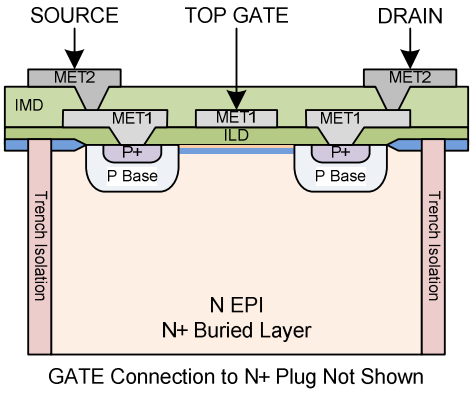

Fig. 9. JFET Cross Section showing Top Gate Shield

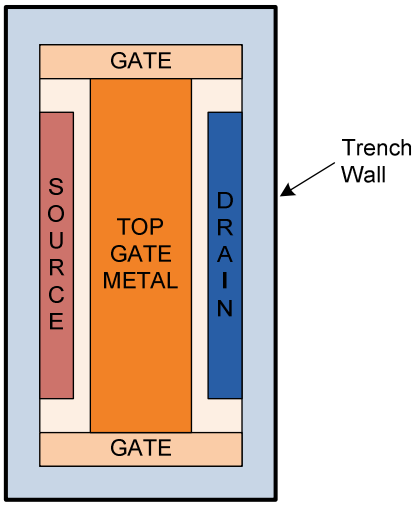

Fig. 10. JFET with Top Gate Shield Layout View

6) Thin Film Placement and Orientation

In order to minimize the mechanical stresses across the critical thin film resistors it is best to keep them away from the edge of the die where the stress gradients can be large. The orientation of matched resistors matters as well, by designing them as mirror images with current flows in the same direction; a stress gradient across the resistors will result in errors of equal magnitude but opposite direction again making them easy to cancel out in a summation. In order to take advantage of these precision enhancements the die area is typically larger; Fig. 11 shows the impact of these in terms of die area impact.

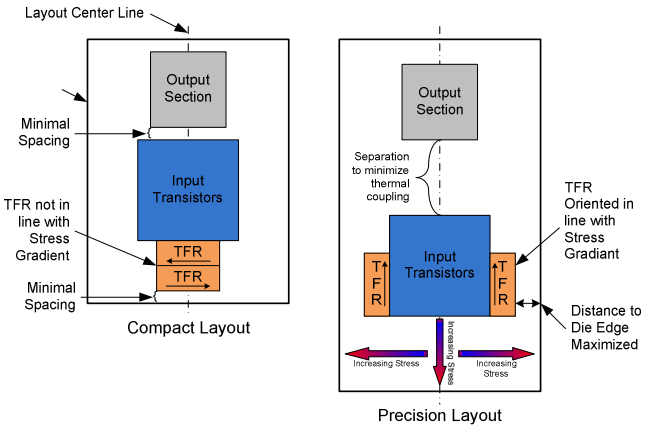

Fig. 11. Die Area Impact in Precision Layouts

7) Placement of Capacitors

Unlike TFR, poly-oxide-poly capacitors are inherently less sensitive to thermal and mechanical stress gradients. They are therefore ideal to place at the periphery of the IC to make the best possible use of the space. These capacitors are often used for the amplifier's compensation and are therefore a required component of the IC.

8) Thin Film Resistor Interconnection

Noise and heat can be generated when thin film resistors are connected directly to a ICs metallization system. A low ohmic barrier metal is introduced between the aluminum of the metal system and the contact of the TFR in order to reduce the contact resistance between the two materials and eliminate this problem.

E. Packaging

Packaging for the IC can consist of wide range of options from bare die to plastic molded commercial packages to hermetically sealed ceramic and metal packages. Up to 175˚C a plastic package can be used assuming that appropriate wire bonding processes are applied, see the interconnect section for more details. Fig. 12 shows the package diagram of the eight pin Small Outline IC, (SOIC_N), package used for the AD8634 and ADR225.

For 210˚C operation the AD8634 and ADR225, ADI is using surface mountable ceramic flat packs which provide the right combination of a hermetic seal, resistance to temperature effects, minimized mechanical stress, and protection from external environmental contamination that can cause corrosion and degrade device lifetimes. See Fig. 13 for the drawing of the eight lead ceramic flat pack, (CFP), the package used for these devices.

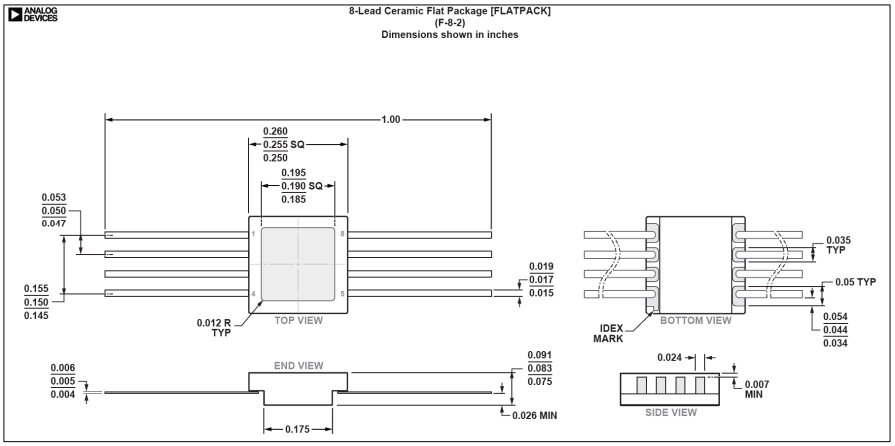

Fig. 13. 8 Lead Ceramic Flat Package

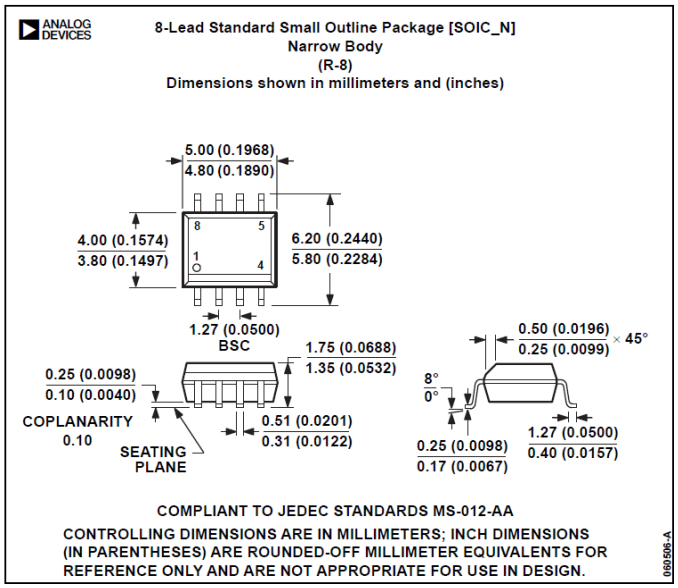

Fig. 12. 8 Lead SOIC Plastic Package

In a commercial application the thermal resistance of the package, Theta JA, (θ_{JA}), (defined as the ratio of temperature rise of junction of the IC per unit Watt that the IC generates), is typically a key concern as it results in a significant difference between ambient temperatures and the internal junction temperature which must not exceed a maximum temperature rating for safe operation. This is due to the fact that the IC is subject to various failure modes should the junction temperatures exceed the absolute maximum rating of the part.

In a HT application the self-heating represents only a small addition to the overall junction temperature so the majority impact is from ambient conditions. So θ_{JA} becomes less of a concern than the glass transition temperature, (T_G), of the molding compound used in the plastic package or the ceramic used in the hermetically sealed packages. For a ceramic package, the materials used are capable of withstanding temperatures in excess of 200°C and are selected to match the mission profile for these reasons.

F. Interconnect

Wire bonding is generally considered the most cost-effective and flexible interconnect technology available to the semiconductor industry and is used to assemble the vast majority of semiconductor packages. Current industry standard wire bond interconnect for plastic packaging uses a Gold, (Au), wire ball bonding on an Aluminium, (Al), bond pad surface.

The process of wire bonding brings the Au wire and Al pad into contact and, with the combined application of temperature, energy, and force, initiates a process of diffusion between the metals. This in turns seeds the formation of a thin layer of AuAl Intermetallic Compound, (IMC), at the bond to pad interface, thus forming an electro-mechanical bond. The images in Fig. 14 illustrates: (a) wire bond interconnects between a die and a lead frame substrate, (b) ball bonds on pads, and (c) a cross-section of a ball bond showing IMC at the bond-to-pad interface.

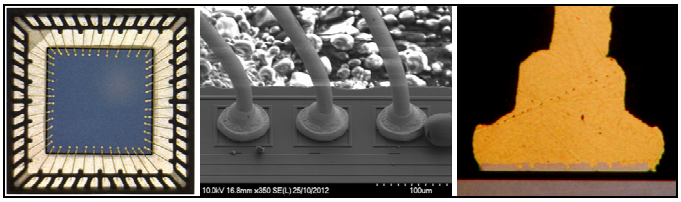

Fig. 14. Wire bond illustrations

The AuAl IMC layer continues to grow over time, drawing in and incorporating the Au and Al in the immediate vicinity of the IMC layer. The growth rate of the IMC layer is influenced by temperature, accelerating significantly at increased temperatures. Constrained diffusion paths, or accelerated diffusion rates result in the formation of voids at the Bond to Pad interface. The development of voids can lead to increased contact resistance, and reduced mechanical strength of the bond, contributing to bond failure. Fig. 15 shows the degradation in mechanical attachment strength of the bond, as assessed by Bond Shear Test, (BST), over time and across multiple temperature ranges. A BST is a test of the mechanical strength of the ball bond conducted by measuring the force required to shear a ball bond from the pad by exerting a

horizontal force at the midpoint of the ball bond and increasing the force until the bond fails using a machine known as a bond shear tester [4].

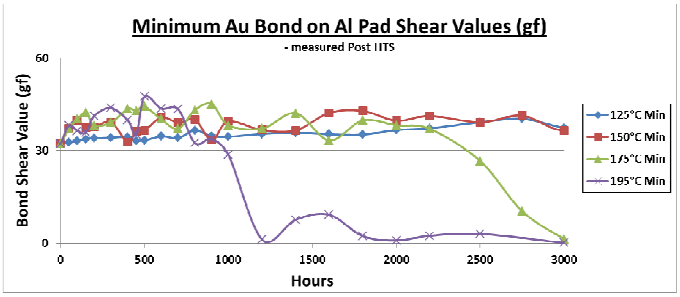

Fig. 15. AuAl Ball Bond Shear Test Results

The results show that for a typical AuAl bond pad, there is no significant degradation in bond strength at 125˚C and 150˚C over the 3000 hours which is typical of a commercial product. At 175˚C the BST shows degradation after approximately 2,200 hours and essentially a complete loss of bond strength at about 3,000 hours. This is an operating condition beyond what is expected for a commercial IC and one of the reasons that special bill-of-materials must be used in packaging for HT semiconductors. At 195˚C the IMC growth rate accelerates further so that degradation can be seen at 1,000 hours and by 1,200 hours AuAl bond failure can be anticipated.

With the increasing cost of Au and the development of finer processing controls for Cu wire bonding in recent years, Cu wire bonding now presents an alternative to Au wire. The CuAl IMC presents reduced growth rates across all relevant temperature ranges. Fig. 16 shows data illustrating IMC growth rates, over time at 150°C, for different bond wire materials (Au and Cu). Note that Cu wire bonding has not been used on these devices at this time as the long term qualification of Cu wire bonding is still in process.

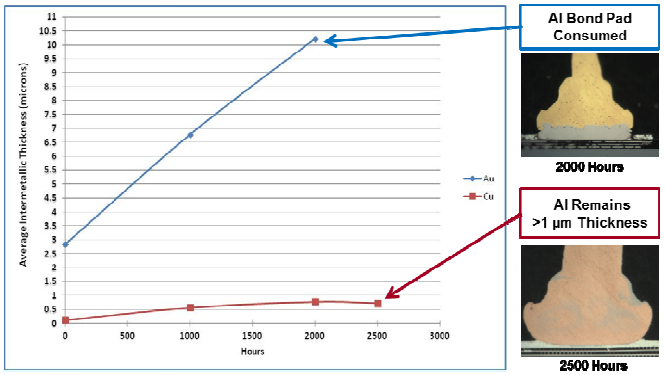

Fig. 16. IMC Growth rate for Au and Cu wire

The type of bond failures discussed here can be avoided by using a mono-metallic system. Bond pad surfacing technologies, such as Over Pad Metallization (OPM), provides an Au surface for bonding Au wire. This eliminates the formation of IMC and avoids the ageing complications of the previous wire bond structures. Fig. 17 shows cross-section images that contrast the AuAl IMC on the left, and absence of same with the OPM structure on the right, through similar storage temperatures. We can see that the AuAl bond has significant IMC and void formation after only 500 hours, while the OPM solution maintains integrity after 6000 hours.

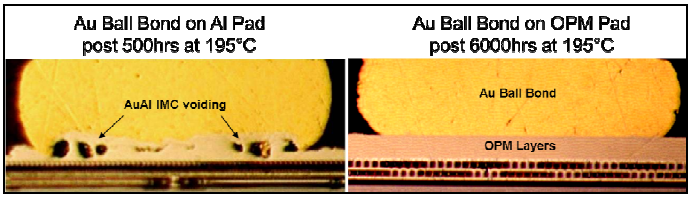

Fig. 17. OPM vs non-OPM IMC growth

The data acquired on the progression of wire bond IMC formation over time and temperature can be used to support selection of optimal IC package materials that maximize the bond interconnect lifetime. Additionally, the use of halide-free molding compounds, while addressing environmental concerns, also helps to promote wire bond reliability by eliminating the well-understood interconnect failures associated with halogens at high ambient temperatures.

For hermetic packaging, i.e. the ceramic flat pack shown in Fig. 13, Al bond wire is used with the native Al bond pad on the die. As with the OPM solution for plastic packages, this monometallic system does not suffer from formation of IMC and the associated bond fatigue.

G. *Chacterization*

To characterize these devices we started with a preliminary design evaluation test based on initial silicon to determine if the temperature performance would meet the needs for the application. This small sample size test was used only as an initial indication of viability and was the first gate in the process of qualifying the devices for HT operation.

Automated test equipment, (ATE) was used in order to run a larger sample size to characterize the device's DC specifications at elevated temperature in order to generate statistically valid sample sizes. This approach is aligned with ADI's standards for all new product characterization to reflect expected variations over the production lifetime.

AC characterization was done on the bench in order to test the dynamic performance of the devices over temperature. Many of the datasheet graphs are based on this work where the ATE cannot measure with the needed precision and accuracy. This is why most AC performance parameters are typical values and not guaranteed by minimum and maximum limits. In many cases the AC performance is assured by a set of related DC specifications that are tested on ATE at final test such as supply current which is proportional to bandwidth; if the supply current is within specification than the bandwidth will be as well.

H. Qualification / Reliability Testing

In order to qualify a device as suitable for a HT application comprehensive reliability testing must be performed. Some of these tests include:

- Electrostatic Discharge (Field Induced Charge Device Model, Human Body Model, and Machine Model)
- Latch-up Immunity
- High Temperature Operating Life (HTOL)
- Solder Heat Resistance
- Temperature Cycling
- Wire Pull Testing
- High Temperature Storage
- Group D Mechanical Integrity
- Autoclave
- Highly Accelerated Stress Test (HAST)

Product lifetimes at extended operating temperature are obtained using the HTOL test, which is performed to JEDEC JESD22-A108 specifications. Lifetimes are predicted from the Arrhenius equation, taking into account potential design and manufacturing failure mechanism assumptions. A minimum of three assembly lots for each IC were processed through HTOL at the maximum operating temperature. Fig. 18 shows the graph of predicted lifetime versus operating temperature associated with a hermetic packaged device based on 1000 hours of HTOL testing at 210˚C.

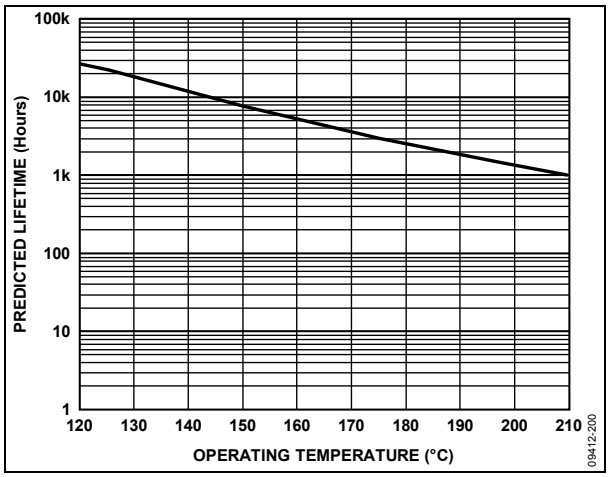

Fig. 18. Predicted Lifetime vs. Operating Temperature

I. Production Testing

It is not enough to simply qualify a device and release it to the market; production testing is required to guarantee performance. For these products a specialized version of the production test hardware and software was created so the products could be tested at elevated temperature. All die are probed at 175˚C prior to assembly, with an elevated temperature of 150˚C used for plastic packaged devices and at 210˚C for hermetic packages at final test.

V. EXAMPLE APPLICATION: SENSOR SIGNAL CONDITIONING

When operating electronics in harsh environments, temperature is often a key parameter that is measured for a variety of reasons. A precise, stable measurement of the ambient temperature may be of interest, such as the case when monitoring the temperature in a producing oil well over a long period of time. Alternatively, we may be interested in the local temperature of a sensor so that we can calibrate its performance; thus accuracy, repeatability and close physical coupling are important. An example of this would be using a temperature sensor to calibrate the zero bias drift of an accelerometer, such as the ADXL206. Finally, another common application is measuring the system temperature for diagnostics purposes, to ensure that device operation is within the intended specifications.

A. Temperature Sensor Technology

When temperatures outside of the operating range of the electronics must be measured, remote probes are normally used. However, when the signal conditioning electronics must be co-located in the elevated temperature environment, as is the case in many downhole, engine monitoring and other previously described harsh environment applications, it poses a challenge to obtain an accurate, high resolution temperature measurement. Some sensor technologies cannot be used in this situation. Thermocouples, for instance, rely on a known reference temperature (the “cold junction”) which would not be present in this case.

However, there are several temperature sensor technologies that are appropriate for these types of environments: quartz, resistive and silicon are three common ones. Quartz crystal temperature sensors have extremely high accuracy and a very linear response, and thus are used in applications with the most stringent requirements. However, these types of sensors are not widely available rated for high temperature and require a second low drift reference clock source, adding complexity, cost and increased power consumption to the system.

Silicon temp sensors, such as the 150˚C rated AD590 and 175˚C rated ADT7312, offer low power, smaller footprint and ease of use with accuracy as good as +/ 1.0˚C over the rated temperature range. For applications that need higher accuracy than silicon, resistive temperature sensors such as platinum RTDs are a good choice. These sensors are widely available, offer excellent stability and repeatability, and can have accuracy better than +/- 1.0°C @ 200˚C. However, RTDs can be a challenge to use, especially over a wide temperature range, because they require a stable excitation source, precision signal conditioning, and errors due to lead wire resistance must be overcome.

B. RTD Signal Conditioning

There are many well-known and proven excitation and signal conditioning circuits for resistive sensors, applying a variety of techniques that trade off parameters such as precision, flexibility, complexity and cost [5]. Wheatstone bridges are commonly used with resistive sensors such as strain gauges, thermistors, and RTDs. However, it is widely

acknowledged that direct current excitation of the RTD with a 4-wire Kelvin connection is preferred for the highest accuracy applications, as shown in Fig. 19.

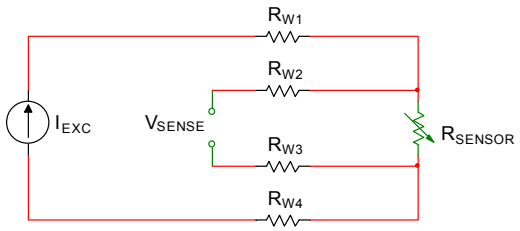

Fig. 19. 4-wire (force/sense) sensor configuration

The unbalanced Wheatstone bridge configuration works well with sensors, such as strain gauges that only vary a few percent across the measurement range. RTDs vary a large amount over the measurement range and, even in a 3-wire configuration, lead wire resistance can cause significant errors [6]. The 4-wire method avoids these errors and also errors due to mismatched resistance between the leads because we have dedicated sense connections that do not carry any significant current. Even in cases where the lead length is negligible, the bridge circuit requires 3 additional precision resistors, and we will see that in the 4-wire implementation we use, only one is needed. In addition, the bridge method creates a non-linear relationship between the output voltage and the voltage across the RTD. In the 4-wire method the output voltage is directly proportional to the RTD voltage (although the RTD resistance-temperature relationship itself is very slightly non-linear, correctable using the Callendar-Van Dusen equation).

C. Design for High Temperature Operation

When designing electronics for use elevated temperature environments, we must often design around electrical parameters that have a wide drift or variance. It is therefore advantageous to minimize the number of error sources (and normally number of components) in the circuit and use ratiometric techniques where possible. The circuit shown in Fig. 20 uses the ADR225 voltage reference and AD8634 operational amplifier to create a simple constant current source suitable for RTD excitation capable of running from a single supply. With the exception of capacitors for reference stability and bypass, only one additional passive component is necessary – current setting resistor Rset.

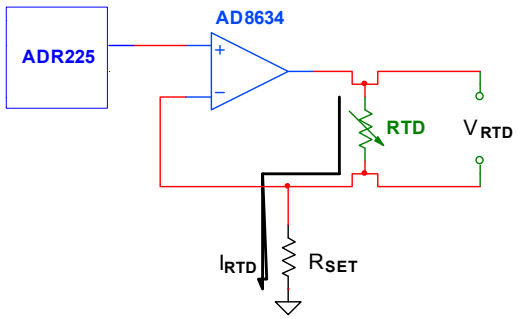

Fig. 20. Constant current source using single operational amplifier and voltage reference

In this circuit, $I_{RTD} = V_{REF}/R_{SET}$. The dominant source of errors are the reference initial accuracy and drift, amplifier offset, and Rset tolerance and drift. However, if we assume that the voltage reference will also be used with an ADC that will be measuring V_{RTD}, the measurement is ratiometric and the error will cancel out. AD8634 is a good fit for the amplifier because it has excellent DC precision specifications (while still being flexible enough to be used in a variety of other applications elsewhere in the signal chain that may require low noise and higher bandwidth).

We must choose Rset to select an excitation current within the RTD specifications so that self-heating does not create errors. With regard to the RTD selection, for the highest accuracy/resolution applications PT1000 sensors are preferred over the more common PT100s due their higher sensitivity. A PT100 sensor is 100Ω at 0˚C, and has an average temperature coefficient α = 0.385Ω/˚C. A PT1000 sensor has an initial value and sensitivity 10 times larger. Either sensor can be used successfully in this circuit.

In order to measure the voltage across the RTD, we need an amplifier with very high input impedance so that no current flows through the sense lines. We also want the ability to reject common mode noise that may be present, especially in the case of long leads. The 210˚C rated AD8229 instrumentation amplifier is an ideal choice to meet these requirements. The AD8229 is a complete monolithic solution that requires only one additional gain setting resistor, unless the unity gain configuration is selected. This makes it very easy to add to our RTD excitation circuit, as shown in Fig. 21.

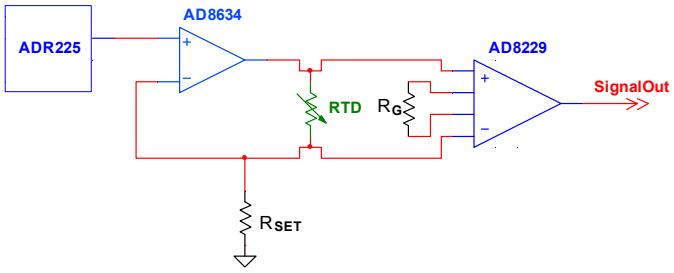

Fig. 21. Constant current source with instrumentation amplifier for RTD voltage measurement

The AD8229 is a very low noise, high precision amplifier that requires at least 8V across the supply rails. We can configure our RTD signal conditioning circuit to use +/-5V supplies and adjust the biasing to allow for input headroom to the in-amp. Fig. 22 shows the complete circuit with these modifications and also includes all additional passives. We have added a resistive divider after the reference in order to lower the common mode voltage seen by the instrumentation amplifier, so the voltage at the non-inverting input of the AD8634 is 1.25V. These resistors, R2 and R3, should be matched. We pick R1, the current setting resistor, to be 2.5kΩ to give us 500uA of current through the RTD. R1 should be high precision and very low drift. Assuming that a PT1000 sensor is used and the maximum temperature that we will need to measure is 300˚C, this gives us a maximum RTD resistance of about 2.1kΩ, and voltage at the non-inverting input of the

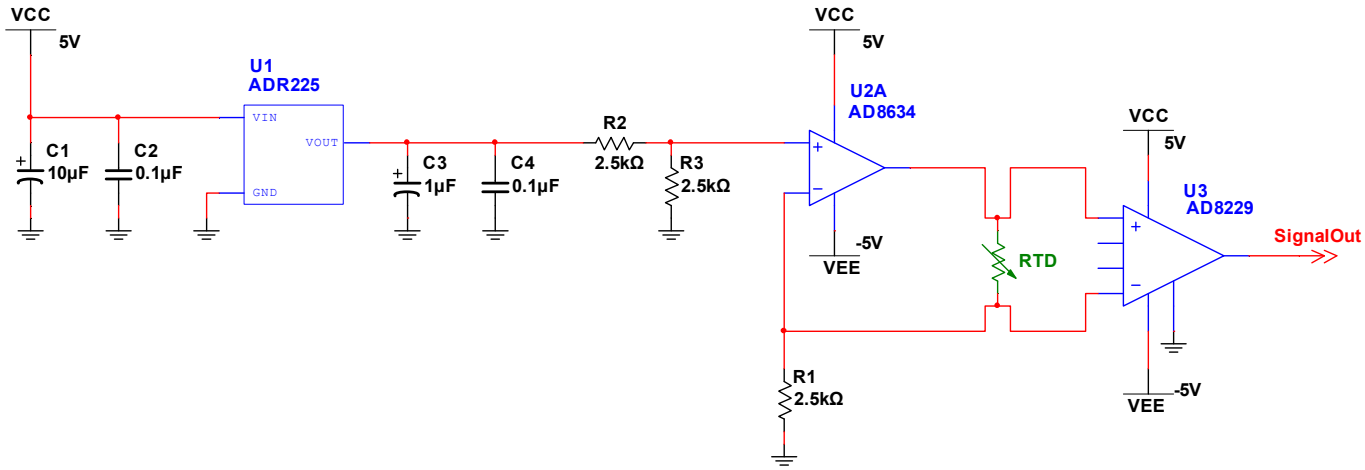

Fig. 22: Complete RTD Signal Conditioning Circuit

AD8229 of 2.25V – within the specified IVR with +/-5V supplies.

Assuming the next block in the signal chain is an ADC; its input range determines how much gain we need from the in-amp. The PT1000 with 500uA of excitation current gives us a relatively large voltage drop and, depending on the ADC input range and resolution requirements, we may be able to use the instrumentation amplifier in unity gain configuration and omit the precision gain setting resistor (and avoid the associated gain drift error due to TCR mismatch with resistors internal to the AD8229). The output of the AD8229 could be connected directly to the ADC, or we could use the second unused AD8634 amplifier channel after it to create an active low pass filter. Also note that if a higher positive supply rail is available that the R2/R3 divider could be omitted (although the value R1 would need to change to maintain the same RTD current).

D. Error Budget Analysis

Another major advantage of using components rated and specified for extreme temperatures, instead of self-certifying standard semiconductors, is the ability to perform detailed error analysis based on trusted datasheet specifications which have been derived from the manufacturer's thorough characterization. To demonstrate this we will do a simplified error analysis of the DC parameters for the circuit shown in Fig. 20. The same procedures can be extended to the entire circuit and include a wider range of error sources if so desired.

For this analysis we are interested in the accuracy of the current through the RTD, I_{RTD}. We can refer to error in parts per million (ppm) referenced to the nominal value at 25˚C. We will categorize error sources into initial accuracy errors and errors due to drift over temperature, as shown in Table III. At the time of this publication these components are still unreleased and only preliminary typical specs were available, so that it what is used for the analysis. Refer to the Analog Devices website for the latest specifications.

Table III identifies the error source, the calculation to convert to PPM, the error in PPM and the "effective error",

TABLE III. EXAMPLE ERROR ANALYSIS OF RTD CURRENT

Error Source	Circuit Calculation	Error Typ (ppm)	Effective Error Typ (ppm)
INITIAL ACCURACY AT T_A=25˚C			
Reference Initial Accuracy	2mV / 2.5V	800	0
Op Amp Initial Input Offset	25µV / 2.5V	10	10
Op Amp Offset from Input Bias Current	80nA*1000kΩ / 2.5V	32	32
Resistor Initial Error	.02%	200	200
	Total Initial Error	**1042**	**242**
DRIFT FROM T_A=25˚C TO T_A=210 ˚C			
Reference Drift	30 ppm / ˚C	5550	0
Op Amp Input Offset Drift	0.5 µV / °C (or 0.2ppm / ˚C)	37	37
Op Amp Input Bias Drift	(-0.24nA / °C) (or -0.096 ppm / °C)	-18	-18
Resistor Drift	2.5 ppm / °C	463	463
	Total Drift Error	**6032**	**482**
	Grand Total Error	**7074**	**724**

which is excludes errors that cancel out because they are ratiometric; in this case the reference voltage that is also connected to an ADC further down the signal chain. Indeed, we can see that the dominant error source is reference initial accuracy and drift so this is a technique worth exploiting. For the current setting resistor we chose to use an FRSH precision foil resistor from Vishay Precision group, which has 0.02% initial accuracy and 2.5ppm drift all the way up to 225˚C. After the voltage reference it is the next highest contributor of error. The FRSH series was chosen because it is available off the shelf in standard values; higher accuracy can be obtained using custom trimmed products.

From Table III we can see that we have an initial error of 242 PPM at 25˚C. This is error that can be easily calibrated out with a single point room temp measurement. We are then left with the drift error of 482 PPM. This is error that can be reduced with a multiple point calibration over temperature.

E. Test Results

The circuit from Fig. 20 was built and tested over the temperature range from 25˚C to 200˚C (limited by temperature rating of the capacitors available). The plot in Fig. 23 shows the RTD current error (green), the VREF error (red) and "effective" RTD current error assuming a ratiometric measurement (purple). We assume 0 PPM error at room temperature, as would be the case with a room temperature calibration. As expected, we see that the dominant error source is the voltage reference drift. When this is cancelled out, we are left with the "effective" RTD current error curve, which has a maximum error of approximately 400 PPM. This is comparable with what we expect from our error analysis in the previous section, total drift error of 482 PPM.

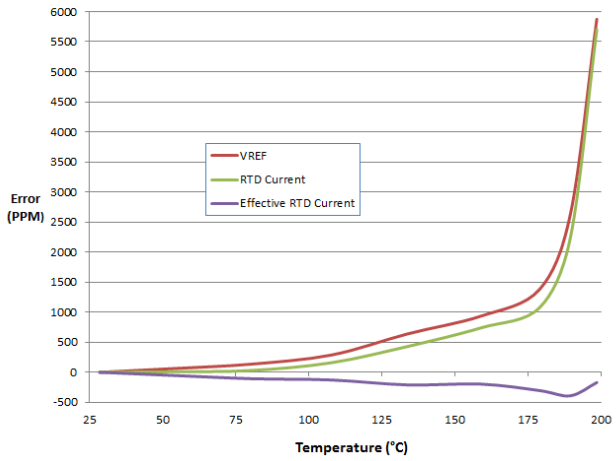

Fig. 23. RTD Current Error vs. Temperature

VI. SUMMARY

This paper examined precision analog signal conditioning semiconductors for high temperature applications in the context of two new devices; a HT rated operational amplifier and voltage reference. We discussed the process of taking a new HT component development from design through release, focusing on the necessary steps that must be taken to ensure high performance, reliable products are brought to market. Finally, an example application circuit was designed, analyzed and tested using Analog Devices HT components.

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