Effectiveness of Barrier Layer Metallisations in Long Term High Temperature Endurance Tests on Wire Bond Interconnections

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Abstract

Silicon on Insulator (SOI) device technology has been shown to be capable of functioning satisfactorily at operating temperatures of >200°C, with device lifetimes of 5 years at 225°C being declared. One of the key areas governing the lifetime of the packaged electronic devices is the reliability of the wire bond interconnection between the device and the package or substrate connection. Extended temperature storage testing at 250°C of packaged SOI devices has highlighted end of life failure modes associated with wire bond connections.

SOI devices are normally supplied with an aluminium based bond pad metallisation, which are not suitable for direct connection of Au wire at operating temperatures of >125°C, due to the formation of Au-Al intermetallics. It is possible to post-process silicon wafers to deposit barrier and connection materials to create a mono-metallic Au-Au joint at the surface. For long term endurance at temperatures >200°C, the effectiveness of the barrier layer in preventing diffusion of the aluminium bond pad metallisation to interact with the Au is a critical factor.

This paper presents results of studies carried out on two post-process metallisation systems Au/TiW and Au/Pd/Ni deposited onto aluminium bond pads, which have been Au wire bonded and exposed to 250°C temperature storage for up to 13,000 hours. The results have shown that the barrier layers are not effective in preventing diffusion of the aluminium bond pad metallisation to create Au-Al based intermetallics. The results are compared with Al-1%Si wire bonding to the aluminium bond pad, where the 2nd wedge bond is attached to a Au/Ni plated metallisation, where the degradation appears to be less severe. Recommendations for designing stable wire bond interconnection systems for extended high temperature operation will be presented.

Keywords: Silicon-on-Insulator devices, high temperature electronics packaging, intermetallics, wire bonding

Introduction

There is a growing desire to install electronic power and control systems in high temperature environments to improve the accuracy of critical measurements and reduce the cost of cabling from remote and hostile locations. Typical applications include down-hole petroleum/gas/geothermal exploration and production and turbine engines for aircraft propulsion and power generation.

This requirement has posed a challenge to the traditional limit of 125°C for high temperature exposure of electronics systems. The leap in operating temperature to above 200°C in combination with high pressures, vibrations and potentially corrosive environments means that different semiconductors, passives, circuit boards and assembly processes are needed to fulfil the target performance specifications.

Although silicon based electronics have been shown to function at temperatures of up to 200°C, the key problem is the performance degradation due to an increase in leakage currents at elevated temperatures. This problem can be virtually eliminated through the use of Silicon-on-Insulator (SOI) technology, where a monocrystalline film of silicon is deposited on top of an insulating layer. This technology has provided the main impetus for the development of high temperature electronic devices. Other materials such as Silicon Carbide (SiC) have promise for even higher temperature performance, and development is on-going to realise basic device functions for signal processing applications [1].

Although much attention has been paid to the development of semiconductor devices that can operate at higher temperatures, robust packaging and reliable interconnections are the key to the success of high temperature electronics systems. Alongside this integrated circuit development, packaging technologies for single chip and multi-chip modules for operation at 250°C for up to 2000 hours have been demonstrated, covering die attach, wire bond interconnect, passive attach materials and ceramic substrates [2].

Most of the reliability data on the high temperature endurance of the devices is generated on the device itself with little attention being paid to the packaging technology around the device. Similarly, most of the reliability data generated on high temperature packaging technologies uses testpieces rather than real devices, which restricts any conclusions on long term electrical performance of the devices. Previous papers have described results of endurance testing up to 11,088 hours at 250°C on SOI devices manufactured with high temperature electronics packaging technologies relevant to signal conditioning and processing functions [3, 4, 5]. These endurance studies have shown end of life effects in terms of changes in electrical performance on some of the functional blocks for the SOI devices. Examination of the failed devices also revealed whisker growth of what was believed to be degraded adhesive die attach material around bond pads.

This paper presents results of studies carried out on two post-process metallisation systems; Au/TiW and Au/Pd/Ni deposited onto aluminium bond pads, which have been Au wire bonded and exposed to 250°C temperature storage for up to 13,000 hours. The results are compared with Al-1%Si wire bonding to the aluminium bond pad, where the 2nd wedge bond is attached to a Au/Ni plated metallisation on a high temperature co-fired ceramic (HTCC) package. The effectiveness of these post-process metallisation systems for withstanding interdiffusion of the aluminium bond pad metallisation with the overlying metallisation and wire has been assessed.

This work was a continuation of the UPTEMP project which was set-up with support from UK Technology Strategy Board (TSB) Technology Programme and the EPSRC, which started in March 2007 and was completed in 2010. The project brought together a consortium of end-users (Sondex Wireline - representing down-well applications, Vibro-Meter UK - representing aeroengine applications), electronic module manufacturers (GE Aviation Systems - Newmarket) and material suppliers (Gwent Electronic Materials and Thermastrate Ltd) with Oxford University - Materials Department, a UK based high temperature electronics research centre providing the detailed analysis of the failure mechanisms.

High Temperature Endurance Studies on SOI Devices

Within the UPTEMP project, a SOI based integrated circuit based on the X-FAB 1µm SOI process has been designed and manufactured with analogue signal conditioning, ADC/DAC (Analogue to Digital Conversion/Digital to Analogue Conversion) and simple logic control functional blocks. The device had dimensions of 4.5mm x 4.0mm, see Fig. 1.

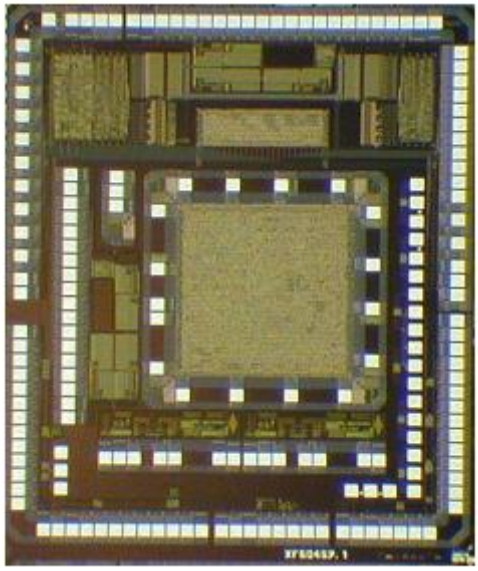

Fig 1. Silicon on Insulator device for high temperature operation developed in UPTEMP project

For the high temperature endurance study, samples using the SOI device have been assembled in HTCC packages, see Fig 2, with different bonding options to characterise the following device functions:

- Multiplexer
- N-Transistor
- Bandgap Voltage
- Oscillator
- Voltage Regulator

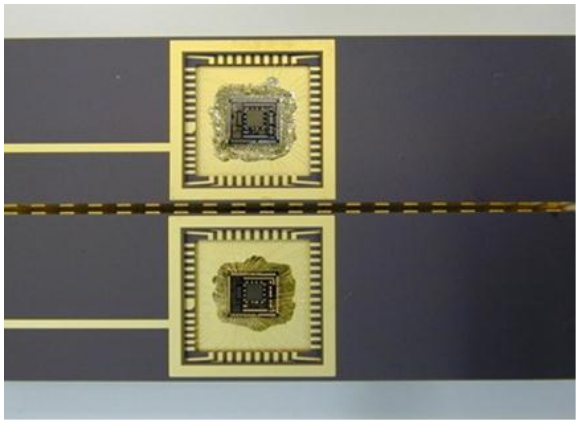

Fig 2. Samples of SOI devices assembled in HTCC package for assessment of electrical performance at 250°C

For wire bonding, Au bumping of aluminium bond pads with a barrier material to create a monometallic joint between the Au wire and Au bond pad surface is attractive. Au wire bonding to Au thick film on alumina has been shown to produce stable bonds up to at least 300°C for 2000 hours [6]. There are several options available commercially for the bumping of devices with Au surface metallisation but little work has been undertaken to examine the long term ageing characteristics of Au wire bonds with bumped devices. Two bumped metallisation options were selected for evaluation in this work, Au/TiW metallisation and Au/Pd/Ni metallisation, see Table 1.

Table 1. Bumped metallisation options for Au wire bonding

Batch	Bond Pad Metallisation	Die Attach
1	Au/TiW	Au-Si
		High T Adhesive
2	Au/Pd/Ni	High T Adhesive

Batch 1: Au/TiW Metallisation

The metallisation was applied to the aluminium bond pads on the SOI wafer through a two stage process, sputtering of a TiW layer (0.3µm thick)/Au (0.11 µm), followed by Au plating (12µm thick).

The devices were then Au wire bonded using 25 µm diameter wire using conditions established from previous work [6].

The assembled packages were submitted to temperature storage at 250°C for up to 11088 hours, with measurements performed at 25°C, 125°C and 250°C before high temperature storage (0 hours) and after storage at intervals up to11088 hours.

The results showed that in general stable performance was achieved for all the functions evaluated, which indicates that the device architecture and packaging technology can withstand the continuous 250°C environment for at least up to 7,056 hours exposure [4]. When the endurance tests were extended to 11,088 hours exposure, some of the devices that had performed satisfactorily showed deterioration in their functionality [5]. Failure analysis of the devices was undertaken to ascertain the degradation mechanisms that have occurred during the high temperature exposure. Some of the devices were assembled with a conductive high temperature adhesive, whilst others were assembled with Au-Si eutectic.

Samples Assembled with Adhesive Die Attach

The samples that had been assembled with a conductive high temperature adhesive had grown whiskers around the bond pad areas as shown in Fig. 3.

The whiskers appeared to grow randomly from the bond pads over the surface of the device and were present on unbonded pads and wire bonded pads.

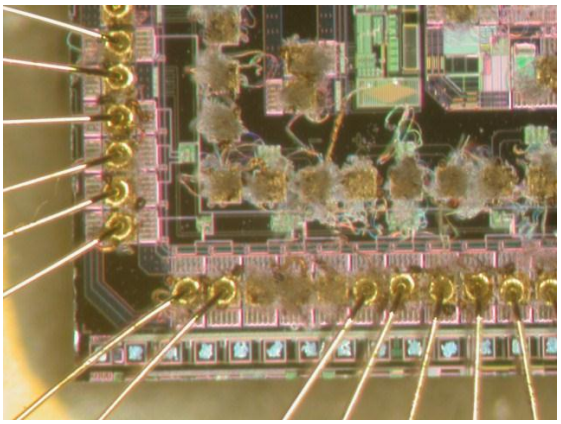

Fig 3. Optical micrograph of surface of adhesive bonded SOI devices after 11,088 hours exposure to 250°C showing whiskers centred around the bond pads

Further examination in a Scanning Electron Microscope (SEM) revealed that the bond pads had degraded and that the whiskers were organic based, but it has not been possible to identify particular chemical species. A typical unbonded bond pad is shown in Fig. 4.

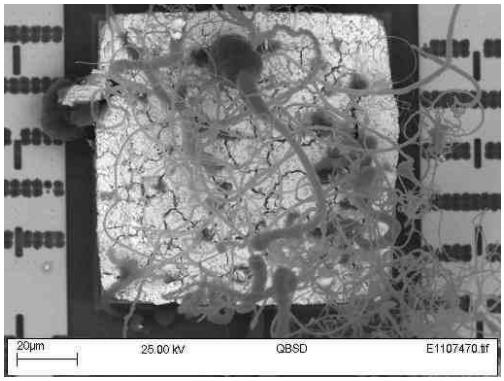

Fig 4. SEM picture of unbonded Au/TiW bond pad of adhesive bonded SOI device after 11,088 hours exposure to 250°C

A typical wire bonded bond pad is shown in Fig.5.

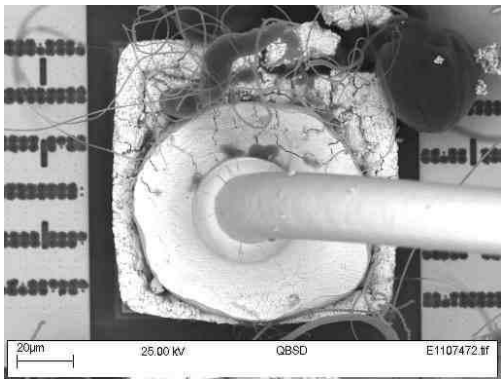

Fig 5. SEM picture of wirebonded Au/TiW bond pad of adhesive bonded SOI device after 11,088 hours exposure to 250°C

We postulate that a chemically activated process is occurring with the adhesive thermally degrading to produce a volatile species that complexes with the aluminium allowing it to migrate passed the TiW diffusion barrier and react with the overlying gold.

A cross-section of the bumped metallisation after 11,088 hours at 250°C is shown in Fig. 6. EDAX analysis showed that the bump structure was predominantly Au-Al intermetallic and that the barrier layer between the Au and Al layer had broken down.

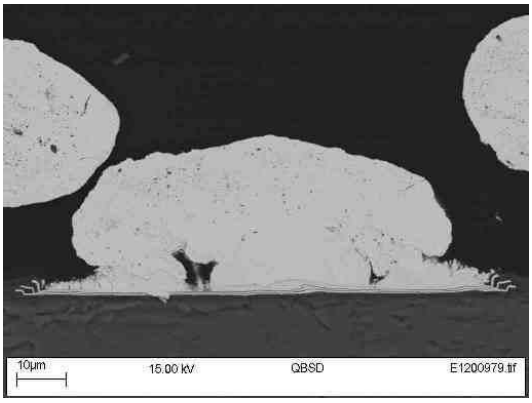

Fig 6. Cross-section of Au bumped device after 11,088 hours at 250°C

The temperature endurance tests continued on selected samples up to 13,000 hours exposure at 250°C. After this temperature/time exposure, several of the bond pads with wires attached became detached from the SOI device, as shown in Fig.7.

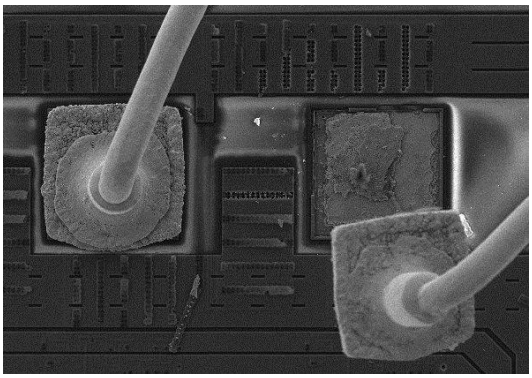

Fig. 7. SEM picture of wire bonded Au/TiW bond pad detached from SOI device after 13,000 hours exposure to 250°C

The underside of the detached bond pad is shown in Fig.8. EDAX analysis of the surface of the detached bond pad showed predominantly W, which is the underlying metallisation on the SOI device.

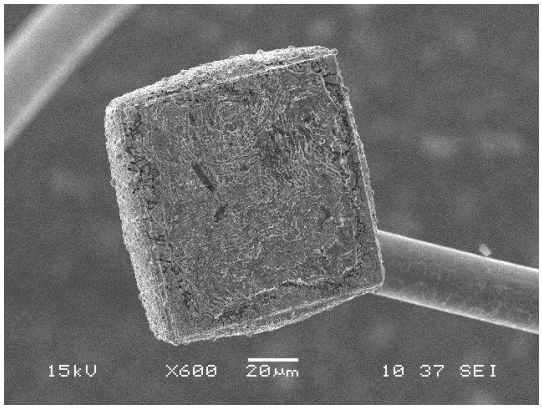

Fig. 8. SEM picture of underside of wire bonded Au/TiW bond pad detached from SOI device after 13,000 hours exposure to 250°C

Batch 2 Au/Pd/Ni Metallisation

The metallisation was applied to the aluminium bond pads on the SOI wafer through a plating process consisting of 5µm Ni, followed by 0.2µm Pd and 0.1µm Au.

The devices were then Au wire bonded using 25 µm diameter wire using conditions established from previous work [5].

The assembled packages were submitted to temperature storage at 250°C for up to 7056 hours, with same measurements performed as for the Batch 1 samples at 25°C, 125°C and 250°C before high temperature storage (0 hours) and after storage for 2016 hours, 5040 hours and 7056 hours.

Some of the devices had performed satisfactorily over the 7056 hours exposure to 250°C, whilst other had showed some deterioration in their functionality. Failure analysis of the devices has been undertaken to ascertain the degradation mechanisms that have occurred during the high temperature exposure.

Bond lifts from the devices were observed on several samples, as shown in Fig. 9.

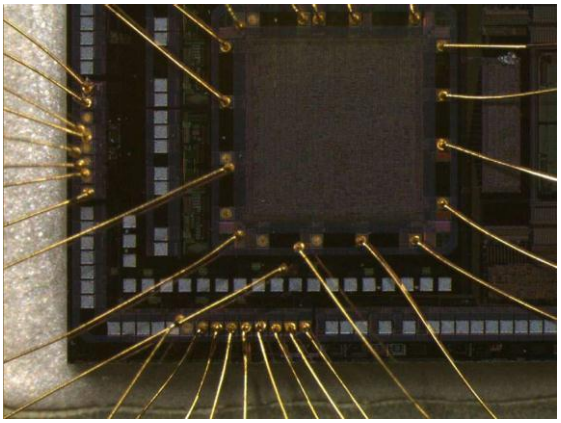

Fig. 9. Wire bond lifts from Au/Pd/Ni bond pad on SOI device after 7,056 hours at 250°C

The samples examined all showed the formation of Au-Al intermetallics around the wire bond after exposure to 7056 hours at 250°C, with the SEM picture presented in Fig. 9. and the EDAX analysis shown in Fig. 10.

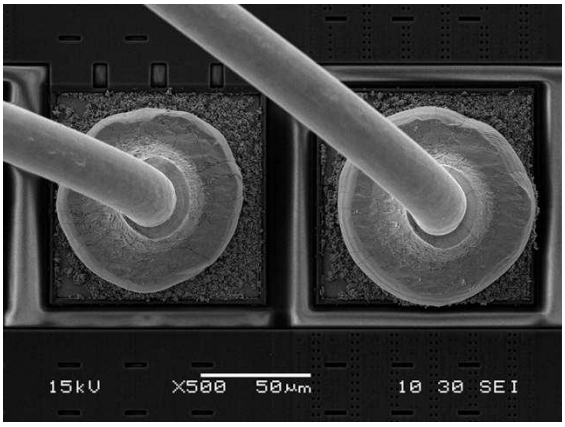

Fig 9. SEM picture of wire bonded Au/Pd/Ni bond pad after 7,056 hours at 250°C

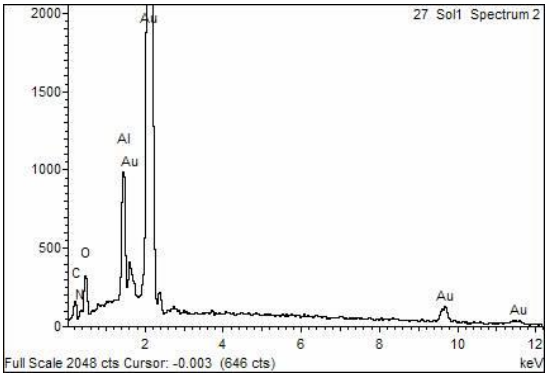

Fig. 10. EDAX analysis of Au/Pd/Ni bond pad showing Au/Al intermetallics after 7,056 hours at 250°C

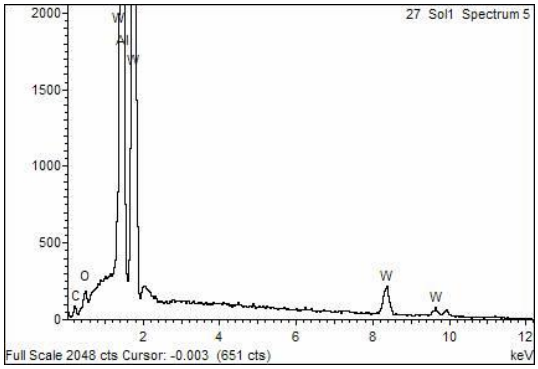

Fig.11. EDAX analysis of Au/Pd/Ni bond pad showing exposure of W after 7,056 hours at 250°C

The EDAX analysis also showed the presence of W in areas where there were no Au-Al intermetallics as shown in Fig.11.

These results indicated that the Au/Pd/Ni bond pad metallisation is consumed during the prolonged temperature exposure at 250°C, leading to the formation of Au-Al intermetallics.

Al-1%Si Wire Bonding to Al metallised SOI Devices

Parallel tests were performed using 25µm diameter Al-1%Si wire on the as-manufactured SOI devices with aluminium based bond pad metallisation. The first bond onto the aluminium bond pad metallisation did not show any evidence of degradation after 7,056 hours at 250°C, as shown in Fig. 12. Some evidence of intermetallic growth on the second bond to the Au/Ni plating on a W/Mo track on the HTCC package was noted, see Fig. 13.

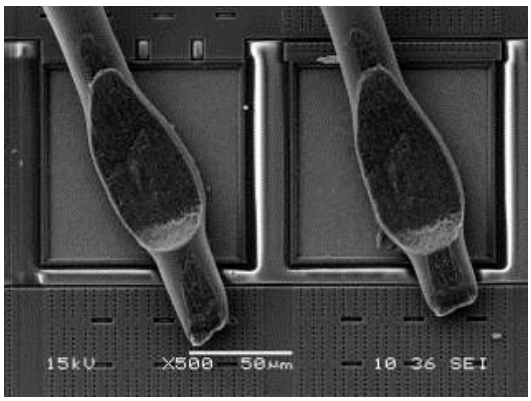

Fig. 12. Al-1%Si wire bonded to Al metallised bond pad on SOI device after 7,056 hours at 250°C

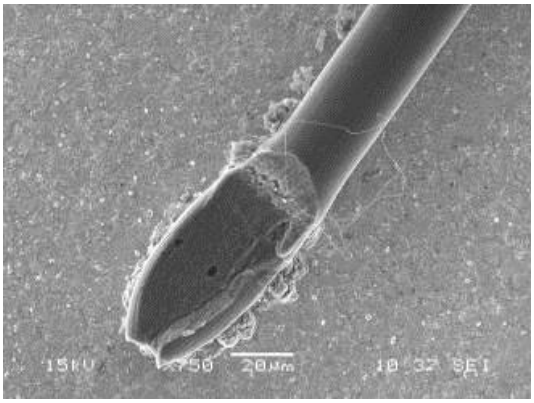

Fig. 13. Al-1%Si wire bonded to Au/Ni plated HTCC package after 7,056 hours at 250°C

Effectiveness of barrier layers metallisations for high temperature endurance

TiW/Au metallisation on Al bond pads

Titanium tungsten (Ti-W) barrier metallisations have been used extensively in the electronics industry for several decades. In addition to providing good adhesion, the refractory metal also functions as a diffusion barrier. Work has demonstrated that the Ti-W barrier layers are stable up to 600°C for silver metallisation [8]. However, the effectiveness of the Ti-W layer as a diffusion barrier to aluminium migration towards the Au overplating and wire bond in this work has been questionable. Further investigation of published literature has revealed that the barrier layer effectiveness depends on the sputtering conditions and the stress of the as-deposited films [9, 10]. Aluminium was shown to migrate through a Ti-W barrier metallisation in less than an hour at 250°C through grain boundary diffusion, the rate of migration was reduced by incorporation of nitrogen into the sputtering chamber. Excessive stresses on the Ti-W film can cause fracture of the film which would render the barrier layer ineffective. If the Ti-W barrier layer approach is to be demonstrated for long term high temperature products, further studies on the Ti-W deposition process need to be carried out.

Ni/Pd/Au metallisation on Al bond pads

The electroless Ni/electroless Pd/immersion Au plating process has been demonstrated on ceramic substrates for Au and Al wire bonding for 2000 hours at 150°C, with no evidence of wire bond strengths decreasing below accepted standards [11]. The addition of Pd into the plating sequence has been shown to reduce the diffusion of Ni through to the Au top surface, which can affect wire bondability when oxidised [12].

The Ni plating layer does not have any specific barrier layer characteristics against the migration of aluminium. Although inter-diffusion rates are low at room temperature, over time a range of NiAl based intermetallics will form. Similarly with Pd, Al-Pd intermetallics will form over time. From the work carried out here, it is clear that over a period of 7,000 hours at 250°C, complete intermixing of the elements has taken place with the extensive formation of Au-Al intermetallics and eventual bond lift-offs. For long life high temperature products, operating up to 250°C, the NiPdAu metallisation over aluminium bond pads does not offer a long term solution to the avoidance of Au-Al intermetallic formation.

At the storage temperatures used in this study grain boundary diffusion predominates. However, with TiW as a diffusion barrier one would expect Al to only penetrate 10 nm into the diffusion barrier after 10,000 hrs at 250°C. We would expect complete diffusion of Au through Pd:Ni in ca. 4,000 hrs at 250°C.

The use of a Pt capping layer may offer an improved performance.

Al-1%Si wire bonds to Au metallisations on substrates

Although Al-1%Si wire bonding to the Al based metallisation on the bond pads on SOI devices was not the original focus of the work, it appears that the joint between the Al-1%Si wire and the Al bond pad is more stable than the Au based over-metallisations. However, the attention on the possible degradation mechanisms switches to the second bond, which may be a thin film, thick film or plated surface depending of the choice of substrate type and conductor metallisation.

The work carried out in this project has indicated that the Al-1%Si wire bonded to Au/Ni plating W/Mo tracks on HTCC did not show any bond lifts up to 7056 hours at 250°C, although there were signs of intermetallic formation. Other work [13], has shown that Au/Ni plating with a top surface Au thickness of <1µm to be stable, although lifetimes may be limited to a few years at 250°C. The resistance of the wire bonded joints will increase over time and the wire bond pull strengths will diminish as the Al-1%Si wire will exhibit annealing and recrystallisation. The Au-Al intermetallic formation may also be accelerated due to reactions with outgassed materials within the package cavity.

Routes to Achieving Long Term Stable Performance at 250°C

For Au wire bonding, the bond pad metallisation on the device needs to prevent aluminium migration through any barrier layer to the Au layer. This can be achieved by not having or by removing the aluminium from the bond pad on the device or creating an effective barrier layer. Although it may be possible to specify metallisation systems with semiconductor manufacturers for bespoke components (normally with high non-recurring engineering charges) it is unlikely that this can be achieved with standard parts. Post-processing of the devices (preferably at the wafer level) by etching of the aluminium and replacement with a plated/sputtered metallisation will be necessary. Formation of a more effective barrier layer with aluminium still present on the bond pad will require optimisation of the deposition conditions for materials such as Ti-W, including controlling gas composition within the sputtering chamber and investigating any possible chemically activated mechanisms with outgassed materials within the cavity.

For Al-1%Si wire bonding, the standard Al based bond pad metallisation for SOI devices forms a mono-metallic joint on the device side. The bond to the substrate or package needs then to be considered, where thin (<1µm) Au metallisations are capable of surviving a few years at 250°C, even there will be Au-Al intermetallic growth, which will ultimately cause bond failure. For longer term stability, further work needs to be directed towards optimising the metallisation system, such as aluminium thin film metallised ceramics.

Theoretical studies of the interdiffusion between elements on the wire bond pads have indicated that the TiW layer should have been sufficient to prevent intermetallic reactions occurring. Clearly the experimental data contradicts this which must indicate that an accelerant is present – the degradation products from the adhesive breakdown.

The Ni/Pd/Au system is unlikely to prevent intermetallic reaction beyond ca. 4,000 hrs. The use of a further diffusion layer such as Pt may delay this.

Conclusions

For Au wire bonding, Au bumping of aluminium bond pads with a barrier material to create a monometallic joint between the Au wire and Au bond pad surface is attractive. However, the

stability of the bumped bond pad with its barrier metal over the 13,000 hours exposure at 250°C in this study does not appear to have prevented the formation of Au-Al intermetallics on the bond pad, with the barrier layer breaking down on both Au/TiW and AuPdNi metallisations. The use of Al-1%Si wire bonded to the aluminium bond pad metallisation does not appear to show evidence of degradation, although the second bond to a Au/Ni plated Mo/W track in a HTCC package did show signs of intermetallic formation after 7056 hours at 250°C.

Acknowledgements

This work is a continuation of the UPTEMP project that was supported by UK Technology Strategy Board (www.innovateuk.org) and the UK EPSRC (www.epsrc.ac.uk). The UPTEMP project involved Sondex Wireline, Vibro-meter UK, Gwent Electronic Materials and Thermastrate Ltd.

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