Tunable Ferroelectric Ceramic Components for Reconfigurable Wireless Communications

Y. Zheng[1], M. Sazegar[1], H. Maune[1], J. R. Binder[2], X. Zhou[1,2], C. Kohler[1,2], M. Nikfalazar[1], A. Mehmood[1], R. Jakoby[1]

[1] Institute of Microwave Engineering and Photonics, Technische Universität Darmstadt, Merckstr. 25, 64283 Darmstadt, Germany
[2] IAM-WPT, Karlsruhe Institute of Technology, Hermann-von-Helmholtz-Platz 1, 76344 Eggenstein-Leopoldshafen, Germany
zheng@imp.tu-darmstadt.de

Abstract

This paper focuses on the technology evolvement and novel concepts of ferroelectric microwave components. They aim to enable reconfigurable wireless frontends for frequency-agile, software-defined and cognitive radios. Such components are an emerging technology based on the nonlinear solid state ferroelectric materials like Barium-Strontium-Titanate namely BST thick-films. They are expected to cope with the demands of multiband and multi-standard operation. Processing and integration technologies are revised to enable multilayer component realization, including selective sol-gel printing and vertical connection through laser drilling. Several novel kernel frontend components based on ferroelectric thick-film ceramic are addressed then. The challenging trend of antennas towards compactness with wider spectrum coverage is coped with several tunable resonant modes in the antennas with integrated BST varactors. The optimized prototype for frequency division duplex services covers $1.47\,\mathrm{GHz}$ *to* $1.76\,\mathrm{GHz}$ *with a variable distance between up- and down-link channels. The environmental impact on antennas can be compensated by tunable matching networks. In the commercial frequency range from* $1.8\,\mathrm{GHz}$ *to* $2.1\,\mathrm{GHz}$*, a demonstrative module exhibits an insertion loss less than* $0.98\,\mathrm{dB}$*, in a compact multilayer package. A compact bandpass filter is enabled by an evanescent mode substrate integrated waveguide cavity in ferroelectric ceramics, integrated with tunable complementary split ring resonator scatterers and tunable matching networks. The compact module covers* $2.95\,\mathrm{GHz}$ *to* $3.57\,\mathrm{GHz}$ *with a comparatively low insertion loss.*

I. Introduction

In last few decades the development of wireless technology has enabled the exciting growth in mobile telecommunications. The endless pursuit of wider bandwidth, higher frequency and better efficiency has driven the innovations of micro- and millimeter wave systems and devices. The challenge of multiband and multi-standard operation is expected to be met by the frequency-agile, software-defined and cognitive radios. Through a dynamical reconfiguration of the high frequency frontend, the system's operation frequency, bandwidth, power level, as well as spatial diversity can be adapted to cope with the time and regional variations of traffic demands. As an enabling technology, the underlying tunable devices have been attracting increasing research efforts. The ferroelectric devices are an emerging technology which grounds on the nonlinear solid state ferroelectric materials. Such materials exhibit a variable permittivity depending on external electric field. Among the various ferroelectric material systems, the Barium-Strontium-Titanate $\mathrm{Ba}_x\mathrm{Sr}_{1-x}\mathrm{TiO}_3$, or namely BST, has shown a mediate permittivity, adequate tunability and dielectric loss, and low leakage current, which are indispensable for compact passive tunable devices. In the meantime, BST can be realized in several technologies like ceramic thick-film and crystal thin-film, which can be flexibly adapted to applications. The tunable devices generally consist of the ferroelectric films, metallic circuitries and additional functional layers. The innovation of such devices encompasses both fundamental materials, circuitry concepts and integration techniques.

This paper illustrates the investigation of micro processing technologies and recent developments of novel RF components. Several technologies for material deposition and component realization, e.g. selective screen printing and vertical connections through BST films are revised. Based on the technologies, tunable ferroelectric devices including multiband tunable antenna, tunable matching network and tunable substrate integrated waveguide filter are demonstrated. Novel antenna design with integrated ferroelectric varactors provides not only a tunable center operating frequency, but also a variable frequency separation

between downlink and uplink channels. The environmental impact and frequency dependence of antennas can be compensated by the tunable matching network based on BST varactors. It can not only stabilize the antenna impedance, maintain the transducer gain, but also increase the frequency coverage. Aiming at a bandpass filter, an evanescent mode substrate integrated waveguide cavity in ferroelectric ceramics is proposed. It is loaded with a pair of complementary split ring resonators, which are tuned through embedded varactors.

II. Processing of Multilayer Ceramic

Ferroelectric materials are processed through various techniques and afterwards integrated into components. On one hand, the synthesis and fabrication of materials eventually determine the topology and performance of the components. On the other hand, the design and integration of components shall be optimized to efficiently utilize the materials' potential. In last decades, bulk and film components have been proposed and investigated. The early research focuses on bulk ceramic process [1], [2]. Afterwards, aiming at higher integration density and lower cost, film components privilege nowadays. The exemplary process can be sol-gel for porous ceramic films. Typically such processes consist of the paste synthesis, target preparation, deposition, and afterwards combined with components technologies such as photolithographic structuring, metalization, passivation and integration etc.

As depicted in Fig. 1, the standard process starts with the synthesis of ferroelectric powder of hundreds-nm diameter dielectric crystal grains. A paste is then prepared consisting of the powder, thinners and binders. The paste is then uniformly pushed onto the substrate surface through a woven mesh screen or a stencil by a squeegee. Both the thickness and the pattern of the film are determined in this step. Finally, the paste is dried and sintered in an oven to form connection between crystal grains.

The screen printing is done by a semiautomatic screen printing machine. The critical process parameters include the distance between the substrate and the screen, the feeding speed of the squeegee, and the pressure of the squeegee. The Al_2O_3 substrate is mounted on printing table by vacuum pressure. The prepared paste is squeezed onto the substrate through a woven mesh. The fineness of the mesh determines the smoothness and thickness of the printed film. Fineness refers to the mesh fineness, wire diameter and mesh diameter.

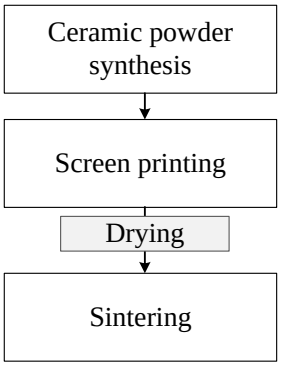
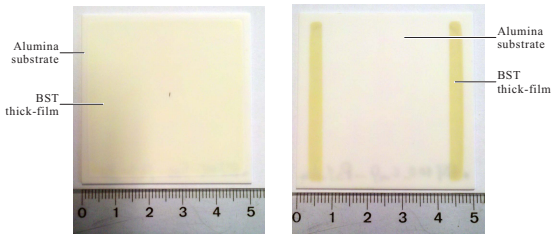


Figure 1. Process of screen-printed thick-film ceramics.

The exemplary parameters are $325 mesh/inch$ mesh, $30\,\mu\mathrm{m}$ diameter wire and $50\,\mu\mathrm{m}$ diameter mesh. The printed film is leveled at room temperature under acetone atmosphere, and afterwards in normal atmosphere under cover. The film is dried finally in convection oven at $60\,^{\circ}\mathrm{C}$. The possible dry cracks of the thick-film can be recovered before sintering by cold isostatic condensation at $300\,\mathrm{MPa}$. As depicted in Fig. 2(a), a $Ba_{0.6}Sr_{0.4}TiO_3$ film is printed on a $50\,\mathrm{mm} \times 50\,\mathrm{mm}$ Al_2O_3 substrate, the printed area is a $48\,\mathrm{mm} \times 48\,\mathrm{mm}$ rectangular.



(a) Homogenouse printing. (b) Selectrive printing of strips.

Figure 2. Screen printed $Ba_{0.6}Sr_{0.4}TiO_3$ on a $50\,\mathrm{mm} \times 50\,\mathrm{mm}$ Al_2O_3 substrate.

In the heterogeneously integrated circuit, where ferroelectric components are one part of a system including also MEMS or semiconductor components, the patterning of the ferroelectric film is indispensable. Selective printing allows the printing of the thick-film only within defined locations. In the standard screen printing process, an additional paste blocking stencil is introduced above the woven mesh. The desired film pattern is then imposed on the substrate instead of a homogeneous coverage, while the remaining steps are maintained as the standard method above. In Fig. 2(b), strips of thick-film is realized on an Al_2O_3 substrate only where the varactors are to be implemented. For the $4\,\mathrm{mm}$ wide strip, there is about $0.5\,\mathrm{mm}$ edges on both sides where the thickness of the film reduces

gradually to zero. The slopes on the one hand reduce the resolution of the printing, on the other hand improve the metallic conduction from the circuitries on alumina substrate to the circuitries on top of the film. The selectively printed thick-films are to be utilized later in section III.

The sinter temperature, i.e. from 650 °C to 1300 °C, constrains the implementation of highly conductive metallic circuitries beneath the thick-film. Therefore planar circuitries on top of the thick-film are typically realized in the form of a single layer metalization. The method is also applicable in the full ceramic components, where there is no possibility to insert metal parts in the ceramic volume. The process flow is depicted in Fig. 3, illustrating major steps.

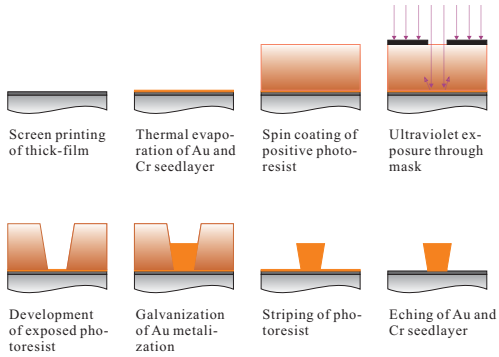
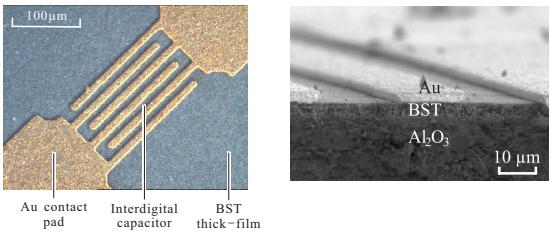


Figure 3. Process flow chart of structuring planar metalization on thick-film ceramics, through photolithography and galvanization.

The process starts with cleaning of the screen printed thick-film substrate. In order to provide the electric connection over the whole substrate surface for later galvanization, a metallic seed layer is evaporated in vacuum. The layer consists of sequentially 20 nm Cr and 60 nm Au where the very thin Cr layer promotes the adhesion between the Au and the porous BST thick-film. Considering the skin depth in the µm range, the reduction of conductivity by the very thin Cr layer is negligible. A positive photoresist is then coated on the seed layer. The seed layer can also be Ni, in order to galvanize Cu later above. Depending on the target thickness of the final metalization, the thickness of the photoresist shall be larger than that of the metal, e.g. 1 µm to 6 µm. It is baked under 90 °C to 105 °C before ultraviolet exposure to harden the photoresist. The purpose is to increase the aspect ratio during development of the photoresist. A photo mask is attached to the top of the photoresist, which shade the ultraviolet on the desired locations. The wavelength and power density of the ultraviolet, exposure time, kind of photoresist, roughness of the seed layer, bake temperature and time determine the quality of the exposure. A feature resolution of 3 µm is achievable. The exposed photoresist exhibit about drastically higher reaction speed than the unexposed part in alkaline solution, e.g. the photoresist developer made from KOH solution [3]. Therefore, the high selectivity of the developer guarantee the removal of exposed photoresist while reducing the etching of the unexposed part to the minimum. Additionally, oxygen ion etching can also help to clean the atom layer residual in the opened areas. Afterwards, Au or Cu are galvanized above. The photoresist functions as a mask here. The metalization deposits only in the open areas, while the photoresist coated area is isolated from the electrolyte and therefore unplated. For specific total open area, the galvanization current is to be balanced for both deposition speed and roughness. The high voltage introduced by too high current would even damage the photoresist. The photoresist function as isolation not only in acidic electrolyte but also in acidic etchant through which the seed layer is removed. Therefore after the target metal thickness is achieved during galvanization, the photoresist mask is removed by either acetone or specific photoresist striper, where the latter kind provides a smooth edge cleaning. Additional oxygen ion etching can also applied here for fine cleaning. The plated circuitries with thick Au or Cu metalization are then isolated during the etching of the seed layer. An exemplary interdigital capacitor (IDC) realized by this process is shown in Fig. 4. The gap width between digits is 8 µm. The Au thickness is 3 µm. The electric field can be established between the digits, which penetrates into the ferroelectric field and the substrate beneath. The high permittivity ferroelectrics dominate the capacitance between the digits. Such IDC is the groundwork of the tunable devices in chapter III.



(a) Interdigital capacitor with contact pads. (b) SEM image of the cross section.

Figure 4. Structured interdigital capacitor on BST thick-film.

The above planar circuitries are easy to fabricate. However, the lack of vertical connections

reduces the integration density. As an example, when realizing spiral inductor an internal grounding is indispensable. It can be realized through a long bonding wire which introduces additional parasitics and reduce reliability. Another solution is to form a via by drilling through the substrate and afterward metalizing it, which is flexible in allocation. By controlling the diameter, height and the resistivity of metalization, the parasitics can be controlled. Laser has been proposed and studied for drilling ceramics [4]. In experiments, when the laser drills from the BST side, the opening on the BST side is larger than the opening on the Al_2O_3 side, which unnecessarily increases the footprint. Considering that the circuitries are typically patterned on the BST side, where small feature size is of higher interest, the laser drills from the bottom side of the Al_2O_3 substrate as illustrated in Fig. 5 is preferable.

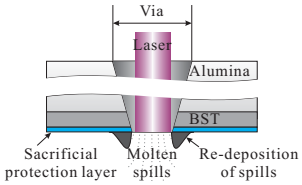
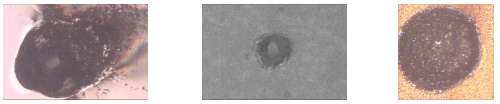


Figure 5. Laser drilling of Al_2O_3 substrate with BST thick-film. Re-deposition of the molten spills reduces the feature resolution of circuitries.



(a) Laser drilled before removal of photoresist sacrificial layer.

(b) After removal of photoresist.

(c) Metallized via.

Figure 6. Using photoresist layer to protect the thick-film against spills during laser drilling.

However, different from single layer ceramics, the Al_2O_3 substrate with BST thick-film coating suffers from their discrepant melting point, namely $1350\,^{\circ}\mathrm{C}$ for BST and $2072\,^{\circ}\mathrm{C}$ for Al_2O_3 [5]. Therefore, when the laser opens the Al_2O_3 substrate, the hot molten Al_2O_3 very quickly melt the BST, and leads to a spill over to the surrounding of the via and redeposition there. Several sacrificial layers have been investigated for the protection of the BST thick-film. As in Fig 5, such layer is desired to isolate the redeposited spills. In Fig. 6, during the drilling of a $0.3\,\mathrm{mm}$ diameter via, the performance of $6\,\mu\mathrm{m}$ photoresist is depicted. The photoresist is first carbonized in a large area around the via shown in Fig. 6(a). It protects efficiently the BST thick-film beneath. After removal of the photoresist in Fig. 6(b), the via shows a clean edge and small foot print. Metallic layers such as Ni, Au and Cr are investigated for protection layer too. However, they melts under the hot spills. The redeposition appears at the openings of the metallic layer. The redeposition increase drastically the total footprint around the via.

The optimized process is summarized in Fig. 7. After the laser drilling, conductive polymer is filled in the via by compressed air from the bottom side. The polymer paste is then curred with hot air. A metalized via is depicted in Fig. 6(c). With a $640\,\mu\mathrm{m}$ thick Al_2O_3 substrate, the via exhibits a lossy inductance. The performance is then modeled as a serial connection of inductor and resistor. With a $0.3\,\mathrm{mm}$ diameter, the inductance is $0.35\,\mathrm{nH}$ and the resistance is $0.02\,\Omega$. This technique is later utilized in drilling vias in the substrate integrated waveguide filter in section III.

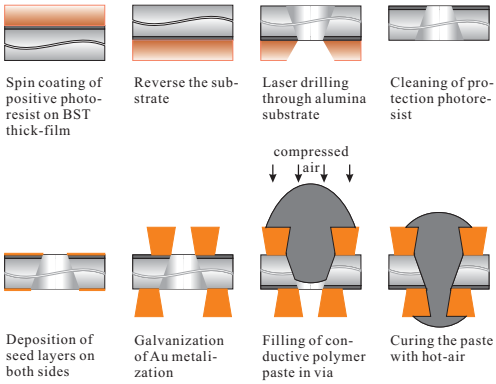


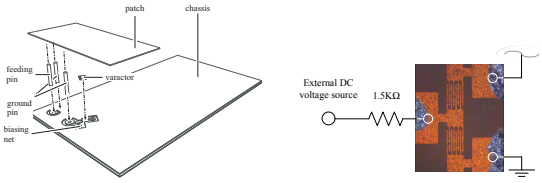
Figure 7. Process flow chart of metalized via through Al_2O_3 substrate and BST thick-film.

III. Tunable Ferroelectric Devices

By utilizing the processing technologies, functional components like ferroelectric varactors are implemented [6]. Built with the components, the tunable devices like the multiband tunable antenna, tunable matching network and tunable substrate integrated waveguide filters can enable the reconfigurability of frontends. The novel concepts not only introduce new functionalities, but also improve considerably the integration density while reducing manufacturing complexity.

The challenging trend towards compactness with wider spectrum coverage of antennas is coped with several tunable resonant modes, which on one hand provide narrower stationary bandwidth than the static counterparts, on the other hand, they can be

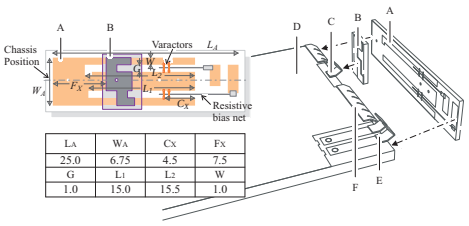
tuned to the desired frequency to equivalently increase the spectrum coverage and allow multiband operations. In a capacitively loaded tunable antennas, the varactors exhibit a voltage-dependent capacitance under external DC voltages. The intrinsic resonator of the antenna shifts its resonant frequency with the tuning of varactor. Therefore it covers neighboring frequency under the convenient electric control [7]. However, the RF voltage alters the operation point of the varactor as well. As a result, with high power input the varactor generates harmonic currents, which cause interferential harmonic radiations [8]. Compared to diodes, the ferroelectric varactors built on BST thick-film exhibit symmetrical capacitance-voltage (C-V) dependence without forward conduction, low hysteresis and high break-down electric field strength. When implemented in tunable antennas as in Fig. 8, the varactors show advantages in improving the antennas' linearity [9]. When the prototype is fed with $-10\,\mathrm{dBm}$ input power, a $35.7\,\mathrm{dB}$ relative suppression of total radiated power (TRP) at the first harmonic is achieved by the BST varactor in comparison to the diode loaded antenna.



(a) Assembly perspective. (b) Ferroelectric varactor pair.

Figure 8. Experimental tunable planar inverted-F antenna with BST varactors.

In order to promote the integration density and copy with multiple band operation requirements, a fully integrated ceramic tunable antenna was proposed in [10]. The configuration of the proposed antenna is depicted in Fig. 9. It consists of a ceramic antenna, microstrip feed and chassis. The tunable antenna is built on a piece of ferroelectric ceramic substrate. The microstrip feed is built on a single sided $0.8\,\mathrm{mm}$-thick FR4 substrate. The antenna is mounted at the chassis' edge. The feed port, ground and bias are connected through spring connectors to the chassis. In the antenna, across each slot there is an IDC pair close to the open end. The varactor pairs namely C_1 and C_2 load at the bottom and the upper slot, respectively. Since they are built on the BST thick-film, the capacitance varies by applying external electrostatic field across the gaps between digits, thus tuning the slot antennas. BST thick-film can be selectively printed only in the varactor areas. The IDC pair is biased at the middle through a highly resistive line. The integrated topology decouples RF signal and external electrostatic bias, without compromising the overall tunability and Q-factor [6]. The two varactor pairs are independently tunable through external DC bias voltages. Therefore, by tuning the capacitances of C_1 and C_2 synchronously, the center frequency F_C at the middle of the two channels is tuned. And by varying the ratio between C_1 and C_2, the channel separation B_{SP} is altered.



L_A	W_A	C_X	F_X
25.0	6.75	4.5	7.5
G	L_1	L_2	W
1.0	15.0	15.5	1.0

Figure 9. Perspective view of A: planar ceramic antenna, B: microstrip feed, C: feed connector, D: chassis, E: DC bias connector, F: grounding pins. All Geometries are in mm unit.

As depicted in Fig. 10, the antenna is fabricated on a $650\,\mu\mathrm{m}$-thick Al_2O_3 substrate with $3.5\,\mu\mathrm{m}$ BST thick-film screen printed on top. The BST-layer exhibits a relative permittivity of 440 at $2\,\mathrm{GHz}$ and room-temperature, with a loss tangent of 0.011. A thin chromium and gold seed layer is evaporated above. Then the IDCs are realized with $3.8\,\mu\mathrm{m}$-thick plated gold electrodes. Additional $50\,\mu\mathrm{m}$-thick gold is plated on strip lines. $40\,\mu\mathrm{m}$-wide and approximately $30\,\mathrm{nm}$-thick bias lines are etched on the chromium seed layer, which show $4\,\mathrm{k\Omega/mm}$ resistivity per line length. The antenna and the feed are edge mounted using a holder made from thin Plexiglas. To ease the manufacturing, spring loaded connectors are utilized instead of springs. The untuned capacitance of each varactor pair is $1.54\,\mathrm{pF}$. With $100\,\mathrm{V}$ bias voltage across the $6\,\mu\mathrm{m}$ gap, $46\,\%$ tunability and Q-factor above 65 are achieved in the frequency range. In measurement, the antenna exhibits the F_C is tunable from $1.47\,\mathrm{GHz}$ to $1.76\,\mathrm{GHz}$, i.e. $16.4\,\%$ tunability. The maximal distance between the low uplink channel and the high downlink channel, which is defined at $-6\,\mathrm{dB}$ matching level, is variable from $38\,\mathrm{MHz}$ to $181\,\mathrm{MHz}$. The controlling of the two parameters are well decoupled.

The environmental impact and frequency dependency of antennas can be then compensated by the tunable matching network. Through an efficient control, it can not only stabilize the antenna impedance, maintain the transducer gain, but also increase the frequency coverage. A typical tunable

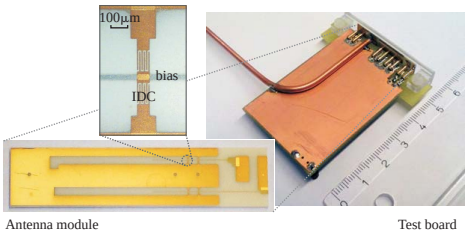
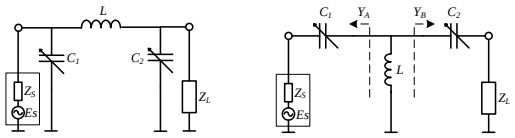


Figure 10. The realized prototype and the varactor pair with bias network.

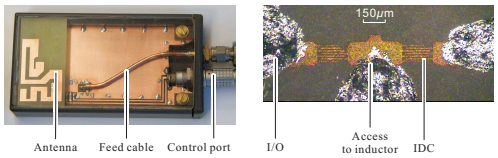
matching network (TMN) is designed to enlarge the impedance matching range through tuning its varactors. Two simple and functional types of single-band TMN are in Π- and T-topologies as shown in Fig. 11(a) and 11(b), respectively [11]. They bridge the source and the load with two varactors, namely C_1, C_2, and one inductor L. The varactors are biased by external DC voltage supplier through DC-RF decoupling peripherals. The DC biasing circuitry is not shown here.



(a) Π-topology (b) T-topology

Figure 11. Representative topologies of single-band lossless tunable matching networks.

Such TMN can be used to match a poorly performing monopole antenna. As in Fig. 12, the kernel TMN encompasses a piece of ceramic module with two IDC varactors and an external discrete inductor. The ceramic module has input and output contact pads as well as a central contact pad to access the middle of the varactor pair. All pads are connected through silver conductive epoxy glue. It is mounted on the ground of an unmatched monopole antenna, with its pads facing upward. Discrete decoupling capacitors and resistors are soldered at the ports of the TMN as bias-tees. Therefore, the whole circuit has six discrete components including the module, inductor and decoupling components. An $50\,\Omega$ coaxial cable stimulates the antenna through the TMN. The pair of bias voltage is generated by an external source and delivered through an additional port as illustrated. The module including peripherals has a footprint of $8.1\,\mathrm{mm} \times 8.5\,\mathrm{mm}$. The antenna is measured to be $35\,\mathrm{mm} \times 20\,\mathrm{mm}$ and $8\,\mathrm{mm}$ extruding above a ground plane of $40\,\mathrm{mm} \times 75\,\mathrm{mm}$.



(a) Demonstrator with a planar inverted-F antenna. (b) Ceramic module with a tunable interdigital capacitor.

Figure 12. Demonstrator of antenna bandwidth enhancement with a tunable matching network on BST thick-film.

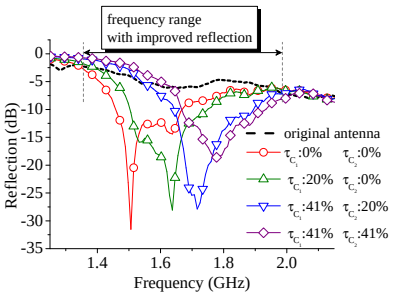


Figure 13. Measurement of bandwidth enhancement of the demonstrator in Fig. 12.

The original antenna exhibits a reflection no less than $-7.5\,\mathrm{dB}$ in the frequency range from $1.5\,\mathrm{GHz}$ to $1.8\,\mathrm{GHz}$. As shown in Fig. 13, with $41\,\%$ varactor tunability, a general improvement of reflection is achieved from $1.35\,\mathrm{GHz}$ to $1.98\,\mathrm{GHz}$, especially the reflection is below $-15\,\mathrm{dB}$ over the range from $1.48\,\mathrm{GHz}$ to $1.81\,\mathrm{GHz}$. The instantaneous bandwidth at $-15\,\mathrm{dB}$ is from $57\,\mathrm{MHz}$ to $140\,\mathrm{MHz}$.

An integrated module within a single package as a part of system-in-package (SIP) is proposed. By using internal fine wires, the module can be realized in a high density. In contrast to the assemblies with bonding wires or conductive epoxy glue, the parasitics in the module can be considerably mitigated through the combination of solder bumps and flip chip technology. However, a discrete off-chip inductor is implemented instead of integrated one. Firstly, high Q factor is indispensable for the TMN, which is not yet available in on-chip inductors. Secondly, by isolating the varactor module and inductor, one gains a flexibility in prototype and fine tuning, the knowledge of which can be later transfered to SIP concepts. Lastly, the concept of the packaged module is compatible with low temperature cofired ceramics (LTCC) carriers, which can be extended to embed high Q factor inductor in the carrier [12]. In the following, several technical challenges towards a packaged module are identified and coped with. The

efforts lead to a demonstrative prototype in Fig. 14. The module consists of the integrated varactor module and an inductor. Both are flip-chip mounted on a multilayer carrier.

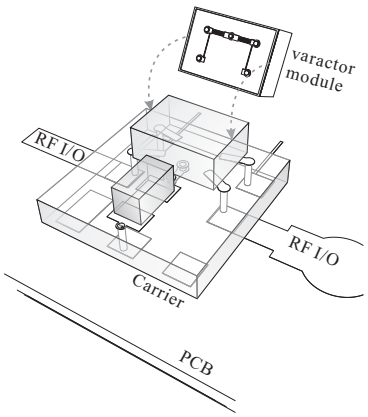


Figure 14. Integrated tunable matching network with BST varactor module and lumped inductor. It is assembled in a multilayer package.

Its functionality is finally proven through verification. Two independent channels of DC bias voltage from $0\,\mathrm{V}$ to $100\,\mathrm{V}$ are applied to the varactors. The two port scatter matrix of the packaged module is measured with $50\,\Omega$ reference on Anritsu 37397C vector network analyzer (VNA). The input reflection and transmission coefficients are measured during the tuning. When both varactors are biased with $0\,\mathrm{V}$ and $100\,\mathrm{V}$, the TMN exhibits a tunable pass band across the target frequency range from $1.8\,\mathrm{GHz}$ to $2.1\,\mathrm{GHz}$ as shown in Fig. 15. With a Q factor of 60 of the varactors and 64 of the inductor, the insertion loss with $50\,\Omega$ source and load is found between $0.86\,\mathrm{dB}$ and $0.98\,\mathrm{dB}$.

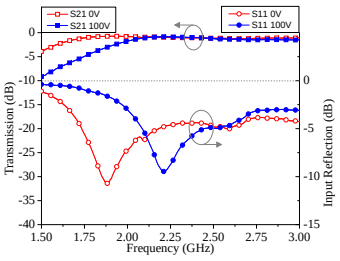


Figure 15. Measured scattering coefficients with $0\,\mathrm{V}$ and $100\,\mathrm{V}$ bias voltage on both varactors.

Ferroelectric varactors have been reported for the implementation in tunable bandpass filters, mainly microstrip or dielectric resonators [13]–[15]. An evanescent mode substrate integrated wave cavity is loaded with a pair of complementary split ring resonators [16]. The ring resonators are tuned through embedded varactors. The input mismatch due to impedance drift during tuning is then compensated by integrated tunable matching with varactors. The configuration of the proposed filter is depicted in Fig. 16. It consists of a tunable evanescent-mode SIW cavity, and two tunable impedance matching networks. The evanescent-mode SIW cavity is loaded with a pair of tunable mushroom-type complementary split-ring resonator (CSRR)s. Each matching network is formed by a serial varactor and a shunted microstrip inductor. The whole module is based on an aluminum oxide ceramic substrate with a Cu-doped BST thick-film screen printed on top.

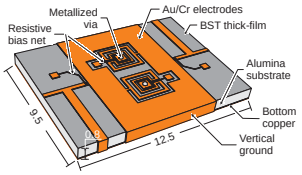


Figure 16. Overview of the proposed tunable filter. Circuitries are implemented on the top of a ceramic substrate. The substrate integrated waveguide cavity and microstrip inductors are grounded at board edges.

In each CSRR there are four IDC pairs at vertexes of the patch. The IDCs are built on the BST thick-film, by applying external electrostatic field across the gaps between digits, the capacitance varies, tuning the CSRRs. The IDC pair is biased at the middle through a highly resistive line. The integrated topology decouples RF signal and external electrostatic bias, without compromising the overall tunability and Q factor as measured and depicted in Fig. 17. In order to deliver DC bias from contact pads to IDCs, the CSRR is split by a $0.25\,\mathrm{mm}$-wide gap at the outer ring to accommodate the resistive line, which has negligible disturbance to the symmetric current distribution along the gap.

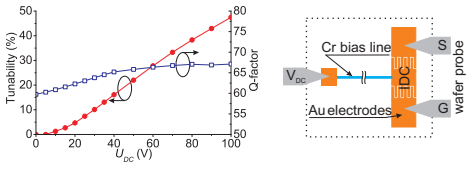


Figure 17. Measured tunability and quality factor of the varactor pair at $3\,\mathrm{GHz}$. The varactor pair is biased at the middle through a resistive line and measured by a signal-ground probe at the gold electrodes.

With the above mentioned parameters, a prototype is realized on a $650\,\mu\mathrm{m}$-thick Al_2O_3 substrate with $2.8\,\mu\mathrm{m}$ BST thick-film screen printed on top. The BST-layer exhibits a relative permittivity of 416 at $3\,\mathrm{GHz}$ and room-temperature,

with a loss tangent of 0.014. 0.3 mm-diameter vias are drilled through substrate using laser. They are afterwards metalized using conductive polymer ProConduct® from LPKF. The vias introduce about 0.02 Ω resistance. A thin chromium and gold seed layer is evaporated above. Then the IDCs are realized with 3.1 µm-thick plated gold electrodes. Additional 4.4 µm-thick gold is plated on patches and rings, which in total is more than 5 times the skin depth at 3 GHz to reduce metallic loss. 20 µm-wide and approximately 30 nm-thick bias lines are etched on the chromium seed layer, which show 6 kΩ/mm resistivity per line length. The realized CSRR is depicted in Fig. 18. A piece of copper sheet is attached to the substrate's bottom. The vertical groundings are finally realized using the conductive polymer.

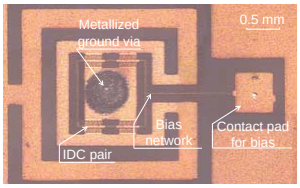


Figure 18. The realized planar tunable complementary split-ring resonator with a ground via at center and four varactor pairs at vertexes. Bias network is resembled by resistive chromium strips in dark color.

The transmission and reflection coefficients are measured during tuning as shown in Fig. 19. The center frequency of passband is tunable from 2.95 GHz to 3.57 GHz, i.e. 21 % tunability. The 3 dB fractional bandwidth is below 5.4 %. The reflection is lower than −10.9 dB at the passband center, while the insertion loss is between 3.3 dB and 2.6 dB. Besides the metallic loss of the microstrip structures, the insertion loss is raised considerably by the loss in BST varactors and the inductive rings. The varactors' equivalent serial resistance is below 1.1 Ω, and it is 0.21 Ω of the rings. According to post-simulations, they are expected to introduce 1.4 dB and 0.5 dB loss, respectively, at the low frequency end.

IV. Conclusion

In this paper, the technology evolvement of multilayer ceramic components has lead to several innovative tunable ferroelectric components for reconfigurable wireless frontends applications. The multiband tunable devices with improved performance and novel functionalities have revealed the potential of ferroelectric thick-film technology,

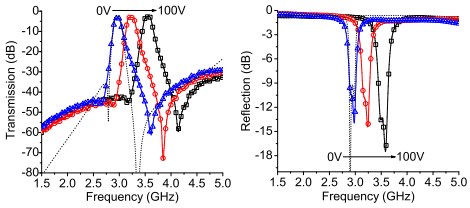


Figure 19. S-parameters of the prototype. Measured: solid lines, simulated at 0 V bias: dot lines.

which provides sufficient tunability to cope with services' variation and environmental impact. Meanwhile, the affordable dielectric loss guarantees the devices' efficiency which can be further compensated with optimized designs.

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