Design of Compact Transmission Line Transformers in LTCC Technology

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Abstract

Concepts for ceramic integrated transmission line transformers (TLT) to conduct powers up to some kW and currents up to 10 A with an impedance ratio of 4:1 are presented. In this power range, a TLT usually consists of coaxial cables. To optimize size, improve integrability and enhance electric performance, our work pursues the integration into a planar multilayer board with electroplated conductors using Low Temperature Cofired Ceramics Technology (LTCC). The methodical design approach is presented, using complementary simulation tools for circuit, multilayer and FEM analysis to reach the aforementioned application-specific performance. Size is reduced further using specific ferrites and optimizing their position. The correlation between measured characteristics of various transmission line transformers produced and underlying design considerations are given in detail. Minimum sizes of 10 to 15 mm squared have been realized using single sided metallisation, which is also well suited for electroplating.

Key words: transmission line transformer, LTCC, enhanced ampacity, optimized scale

Introduction

Transmission-line transformers are used for matching RF and microwave devices. They are compulsory especially for high working frequencies where traditional, magnetically coupled coil transformers can not operate properly any longer since the leakage inductance and parasitic capacitances between the two windings and the turns of each winding restrict their high-frequency operation. Absorbing this leakage inductance and parasitic capacitance into the characteristic impedance of a transmission line so that $Z_0 = \sqrt{L/C}$ or using it to form an equivalent transmission line, the frequency of operation of such transformers can be extended to higher frequencies because transmission lines can be used up to very high frequencies [1]. Moreover, this transformer type features very broad bandwidths. In this paper, a concept to design transmission-line transformers (TLT) in Low Temperature Cofired Ceramics technology (LTCC) is presented.

It is desired to create a preferably minimized ceramic integrated TLT able to conduct powers up to several kW and currents up to 10A with an impedance ratio of 4:1. In this power range, a TLT conventionally consists of coaxial cables, twisted around a ferrite toroid and designed as a surface mounted device (SMD). In order to optimize size, to improve integrability with additional circuit elements and to enhance electric performance, this configuration is to be implemented into a planar multilayer board with electroplated conductors using LTCC.

The presented TLTs use the so called 'boot-strap' configuration invented by Ruthroff [2] for obtaining a 4:1 impedance transformation. It works by splitting the input current between two identical uncoupled transmission lines connected to ground and load, respectively. Figure 1 shows the voltages and currents in this configuration, where terminal 4 is connected back to the input terminal 1.

The characteristics of transmission-line transformers can be derived by considering a 1:4 transformer using lossless twin wires as shown in

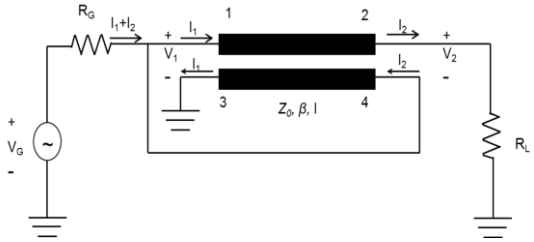

Figure 1: Block diagram of Ruthroff design type 4:1 transmission-line transformer

Fig.1 [1]. The transmission lines are designed to have balanced (odd mode) currents and their lengths have to be less than λ/8. If this boundary condition is violated, the diametrical currents in the transmission lines are no longer matching due to wave reflections within the lines. The bootstrap effect can no longer take place.

According to the physical laws and equations for transmission lines, an expression for the output current I_2 can be found in terms of source voltage V_G, source impedance R_L, characteristic impedance Z_0 of the transmission line, and the electric length $\theta = \beta l = 2\pi l/\lambda$ yielding

$$I_2 = \frac{V_G(1+\cos\theta)}{2R_G(1+\cos\theta)+R_L\cos\theta+j\sin\theta(\frac{R_g R_L}{Z_0}+Z_0)} \quad (1)$$

The source delivers a power of

$$P_{in} = \frac{V_G{}^2}{4R_G} \quad (2)$$

and the power available at the load is

$$P_0 = \frac{|V_G|^2(1+\cos\theta)^2 R_L}{\left[2R_G(1+\cos\theta)+R_L\cos\theta\right]^2+\left[\sin\theta\left(\frac{R_G R_L}{Z_0}+Z_0\right)\right]^2} \cdot (3)$$

When optimizing P_0 with respect to R_L in the limiting case of very small θ, it delivers the desired impedance matching ratio $R_L = 4\,R_G$. The optimum characteristic impedance is found to be $Z_0=2R_G$. Substituting these results in Equ.3, the performance of an ideal transmission line transformer with matching impedance ratio depends on its electrical length, i.e. the ratio between its physical length and the wavelength λ:

$$\frac{P_0}{P_{in}} = \frac{4(1+\cos\theta)^2}{(1+3\cos\theta)^2+4\sin^2\theta} \quad . (4)$$

A second important parameter for transmission lines is the permeability of the adjacent material. [3] A ferrite core with high permeability enlarges the transmission line's inductivity. This can be converted into a shorter transmission line resulting in the same inductance as without ferrite, yet with less characteristic impedance due to the shorter line. The Ruthroff transformer type directly benefits from this behavior. The transmission line transformer's inductance L is also responsible for the low-frequency cut off behavior according to [4]:

$$f_{lo} = \frac{k_1 Z_0}{L} \quad (5)$$

An enhanced inductance results in a lower cut off frequency.

The impact of magnetic materials on planar TLT size will be addressed by FEM simulations in the next chapter.

Design and Simulation

Considering these boundary conditions, our design approach uses complementary tools for circuit, 2.5D multilayer and 3D FEM simulation as well as resistive loss analysis to reach the given specifications.

An impedance ratio of 4:1 is required to match a 50 Ohm to a 12.5 Ohm environment. Furthermore, the device is intended to transmit power and current in the kW and A range between 100 and 200 MHz at an insertion loss below 1 dB.

Taking these specifications to a library-element based schematic simulator, the component's insertion loss is optimized varying the respective parameters like conductor length *l*, strip width *w* and substrate thickness *s*. This kind of simulation is overly idealised and neglects real-world layout possibilities. To progress to a more adequate design by further refinement, the resulting component parameters are transferred to a Method-of-Moments simulator, which solves Maxwell's equations on the actual multilayer layout. In this case the component parameters listed in Tab.1 yielded three different layouts that were taken into further consideration. A characteristic dielectric constant of 8 was assumed for the LTCC ceramic material.

Table 1: Layout parameters derived by Momentum simulation for best insertion loss

Layout parameter	Abbreviation	Value [mm]
Conductor length	*l*	70
Strip width	*w*	1.5
Substrate thickness	*s*	1

Particularly, two different transformer settings were studied. Layout1 and layout2 each consist of a single layer transmission line, whereas layout3 contains a transmission line expanding over two layers. All layouts can be seen in Fig.2. The upper left corner displays layout1. Consisting of a spiral conductor line and a rectangular ground metallization, with an overall footprint of 18.29x15.5mm², it provides the possibility to insert a ferrite core through a center hole. Length, line width and substrate thickness can be taken from Tab.2.

A second structure with a single dielectric substrate layer is depicted in the lower left of Fig.2. It differs from layout1 by having a more square-shaped spiral conductor. Its footprint is about 9.4x9.4mm², the smallest layout so far. Conductor length, line width and substrate thickness can also be seen in Tab.2.

Layout3 (Fig. 2, right) provides a transmission line on two layers, interconnected through conductive vias. With 23.5x16.91mm² it is the largest layout

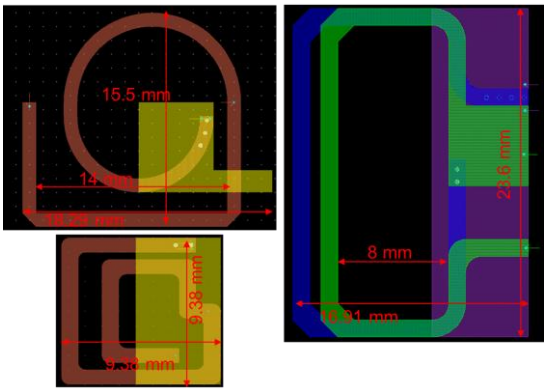

Figure2: TLT layout ideas chosen for further investigation considering their suitability as transmission-line transformers, upper left corner: layout1; lower left corner: layout 2; right side: layout3

under test. Its specifications are given in Tab.2. This layout also provides the option to insert a ferrite core.

Since one of the provided tasks aims at further reducing the required layout space through ferrite application, the layout had to be transferred to a 3D FEM simulation tool to emulate the corresponding electric and magnetic fields in the HF regime. As mentioned above, the application of ferrite material increases the inductance of the transmission line and thereby reduces the low-frequency cut-off. Figure3 displays the simulated insertion loss in dB, comparing a ferrite-less and a ferrite-supported version. The simulation was done assuming a 200µm thick ferrite plate providing a relative permeability of µr=200 attached to top of the substrate. The dielectric properties of the ferrite were neglected for purpose of simplification. The simulated ferrite plate covers the whole substrate surface.

By the ferrite, the insertion loss of layout2 is reduced significantly from -7.12dB at 140MHz to -3.34dB, which is an improvement of nearly 50%.

Table2: Layout parameters: conductor length, width, spacing, and device footprint.

	Layout1	Layout2	Layout3
l [mm]	64	44	100
w[mm]	1	1	1
s[mm]	0.5	0.5	1.2
A[mm²]	18.29x15.5	9.34x9.34	23.4x16.91

Layout1 shows an improvement of 20% from -6dB at 140MHz to -4.87dB in the working frequency range. The behavior of both layouts can be explained by conductor lengths being too short to match the required electrical length and thus generating mismatch losses and a low-frequency penalty. In fact, both layouts emerged from the optimization process with line lengths shorter than the expected 70 mm (see Tab.2). All three layouts indicate how the ferrite raises the permeability of the surrounding, reduces the electromagnetic wavelength (being inversely proportional to the square root of permittivity and permeability) and thus stretches the effective conductor length. In the case of layout3, the conductors are slightly too long and, due to the inherent periodic behavior, the characteristic passes a minimum (maximum insertion loss).In fact, the conductor line of layout3 is 30mm longer than the calculated optimum of 70mm.

A tradeoff exists in ferrites between bandwidth and permeability. At 100 MHz or more it is therefore mandatory to exploit the given permeability as efficient as possible. Therefore, additional simulations were conducted for layout1 and layout3, including a ferrite core material into the layout together with the ferrite plate, increasing the inductance. This way, a relative permeability of

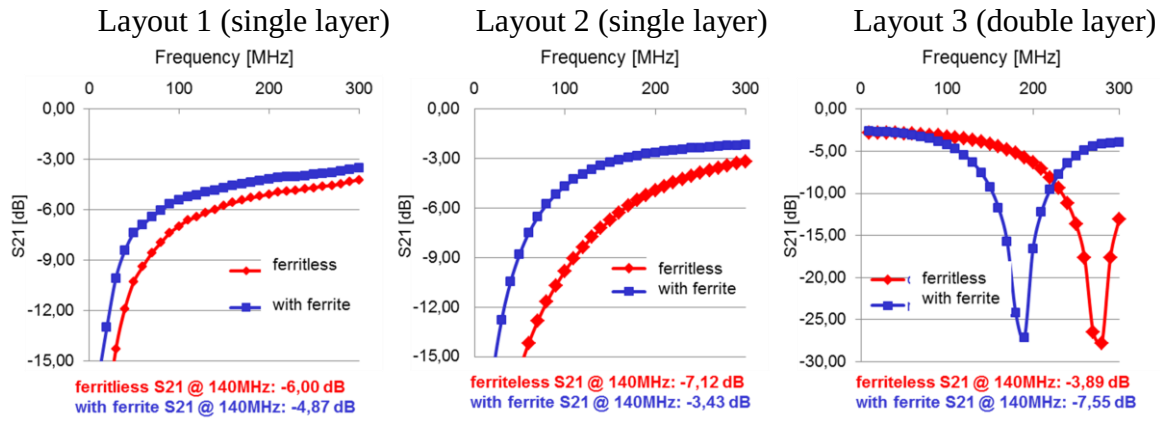

Table 3: FEM simulation results comparing ferrite-less and ferrite-supported versions of the considered layouts, demonstrating the effect of wavelength contraction and electrical length expansion by the ferrite.

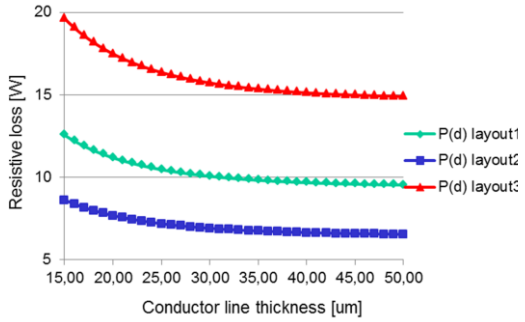

Figure 4: Resistive loss considering skin depth of 5.4um at 140MHz vs. conductor thickness in um, each line is 1mm in width, respective conductor lengths are given in Tab.2.

about 20 has a comparable influence as a higher permeability cover plate alone. For example, commercial NiZn ferrites with permeability above 10 are available.

To improve the current capacity, further processing will include electroplating of the conductor lines. To assess the resistive loss in the component, the resistive loss dependent on the conductor thickness in case of full load, 10A, was determined.

The resistive loss is calculated using the specific material and component parameters, characteristic material resistance ρ, conductor length *l*, width *w* and thickness *d* to derive the component's resistance *R*:

$$R = \rho \frac{l}{w d} \qquad (6)$$

In the RF regime, the skin depth δ

$$\delta = \sqrt{\rho / (\pi f \mu_0 \mu_r)} \qquad (7)$$

has to be taken into consideration. Accordingly, the current density decay exponentially inside the conductor and not the whole geometric conductor cross section is effective. Integrating this decaying current density over the height d of the conductor

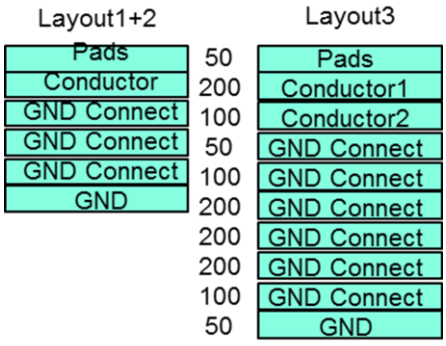

Figure 5: Layer structure and layer thicknesses in µm of the three layouts. The transmission lines are on conductor layers. Vertical interconnects to ground pass through "GND Connect" layers.

from both sides yields the frequency-corrected resistance and consequently the resistive loss

$$P(d) = \frac{1}{2} R(d) I_0^{\,2} = \frac{l I_0^2}{4 \sigma \delta w (1 - e^{-d/2\delta})} \qquad (8)$$

The result for the three layouts is given in Fig.4. For simplification, a fixed frequency of 140 MHz and corresponding skin depth of 5.4 µm (copper metallization) were assumed.

Since layout2 is the shortest, its losses are the smallest ranging from 9W for 15um conductor thickness to 7 W for 50um conductor thickness. Layout3 is on the opposite end of the scale, since its conductor line is the longest. By electroplating, its losses can be reduced by 25% from 20W to 15W. At this appreciable frequency of 140 MHz screen printed conductors have a thickness of three skin depths. Therefore, electroplating can give an improvement of a few W only. However, due to the double benefit in system efficiency and thermal management, future components with 50µm thick electroplated conductors are under way.

Manufacturing

Demonstrators were realized in LTCC technology to test the designs. The demonstrators consists of standard material tapes with a relative dielectric constant of 7.8 (Commercial LTCC tape number 951, DuPont, Wilmington, DE), filled and printed with standard silver conductor paste (Commercial Ag paste number, DuPont, Wilmington, DE) with an electric conductivity of 6.3×10^7 S/m.

After mechanically punching holes into the individual ceramic green tapes, these are filled with Ag paste (DuPont6141) for vertical interconnects (vias) between the layers. The layer sequence and substrate thickness of green tapes is given in Fig. 5. The top layer is required to provide soldering pads, the bottom layer holds the ground metallisation. The layers in between serve as dielectric between conductor line and ground to achieve a well-defined line impedance. Layout1 and layout2 have similar tape structures, layout3 requires more substrate thickness. Conductor paths are formed by screen printing a 15µm thick layer of Ag paste with suitable viscosity (DuPont6145) onto the tape surface. In the next process step, the tapes are stacked in the given sequence (Tab.3), laminated with and sintered at 900°C. The outcome is a hermetically sealed ceramic multilayer circuit board as shown in Fig.6. Embedded conductor structures are visible through the 50um thin cover layer. Further discussion and interpretation of characterization results will be given in the following section.

Characterisation

Small signal measurements were done using a Rohde & Schwarz ZVB8 vector network analyzer. Since the TLT layouts were customized for an impedance ratio of 50:12.5 Ohm, two identical transformers were connected face to face to match the analyzers 50 Ohm impedance on both sides. The measured insertion loss was subsequently divided by two, one half for each transformer. The comparison with FEM simulation is given in Figure 7.

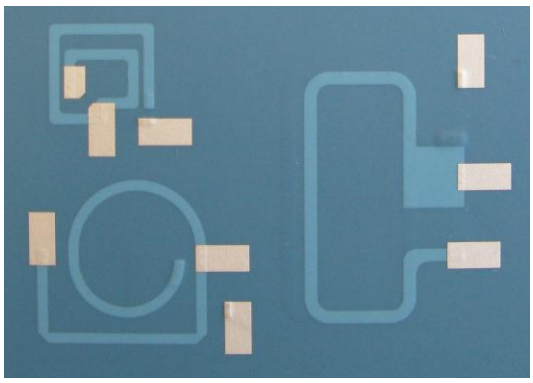

Figure 6: Layout demonstrators after sintering process, clockwise from lower left corner layout1, layout2, and layout3

The first and second layout show generally high insertion losses of about -8dB at 140MHz for layout1 and about -10dB at 140MHz for layout2, roughly 30% higher than expected from the simulation. High insertion loss stems – as described before – from not yet optimized conductor lengths Deviations between measured and simulated performance are attributed to a different ground potential distribution during measurement. Since a full-plane ground metal shielding was intentionally let away, the devices exhibit some sensitivity in this respect; such effects are known for example also from antennas. It demonstrates the necessity to take into account in further simulations the surrounding components and the exact mounting.

With respect to the optimum insertion loss of layout3, the simulated level of 3 dB is well reproduced by the measurement. However, the trend vs. frequency is severely disturbed by the surrounding materials during the measurement, e.g. a supporting plate or clamping mechanism. A design with conductor lines on both substrate sides appears particularly sensitive and less suited for practical use.

Conclusion

A process for converting transmission line transformers into a planar shape suitable for ceramic multilayer board technology was demonstrated. Both, simulatory and experimental results taken from components realized in LTCC technology, pave the way to further development in two directions: Well-defined mounting of the present "minimized" components can be handled when the surrounding electric potential distribution is known and included into the overall component design; alternatively, ground plane shielding from surrounding may be integrated into the component at the expense of size and layer count. This latter approach would resemble the traditional coaxial cable approach to this transformer type that served as the starting point for the present study.

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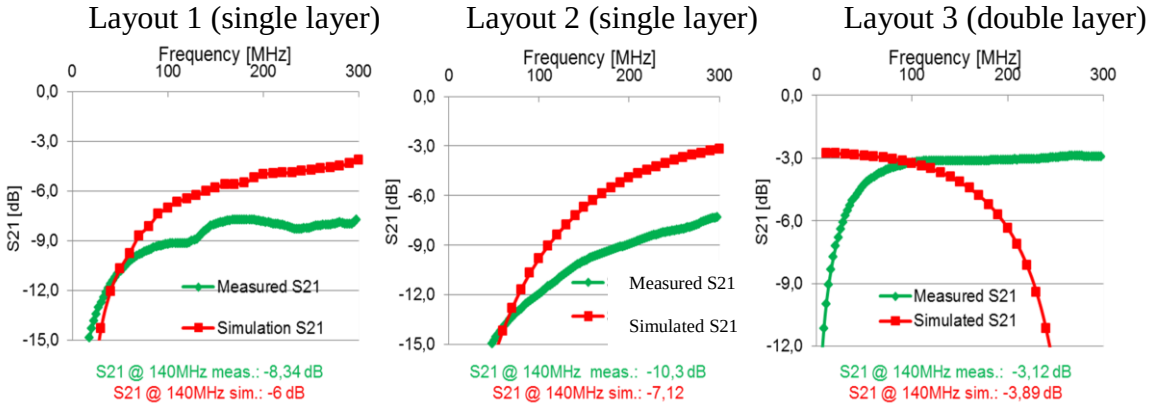

Figure 7: Comparison of measured insertion loss and simulated insertion losses for each layout