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A High Temp standalone 4MByte Flash memory with SPI Interface for 210C applications

This paper covers the internal architecture, testability & performance characterization of Texas Instruments ™ High-Temp 210C 4MByte standalone Flash storage device. It will be available in a 14-pin ceramic dual Flat pack package as well as a Known Good Die (KGD) option. The device is manufactured in TI's 180nm 1.8V flash process with 3.3V IOs. The design implements 8 banks of flash organized into 2M x 16 bits surrounded by a SPI controller. The SPI controller interfaces asynchronously with an internal flash controller. The flash controller is clocked by FCLK, and controls the flash charge pump to access & operate the flash to program, read, erase, validate etc. The SPI controller is responsible for translating and executing the high level SPI protocol commands to the internal flash controller & its registers. A simple and flexible protocol was developed to access the flash array via the SPI supporting various commands and configuration capabilities. Testability of critical parameters for reliable 210C flash operation is ensured with the implementation of an internal test port accessible through a parallel interface (for TI Internal use only). The test port, and a SPI initiated BIST controller are used to provide full & comprehensive characterization of the flash bit cell array, as well as the flash-pump across temperature & frequencies. The form factor, size, and pin out of this flash device is primarily focused on data logging for narrow & space limited extreme harsh environments such as the down-hole drilling industry.

Features: The SM28VLT32-HT is a 4Mbyte flash memory device with Serial Peripheral Interface (SPI). Features include use of a simple SPI based instruction set for read, write, erase and validation. Device utilizes 3.3v supplies and temperature operating range of -55c to 210c with up to 1000 hours of operational life.   Device is packaged in a 14pin ceramic surface mount package with narrow aspect ratio (20mm x 8mm) supporting space constraints for down-hole drilling. See Figure 1.

Figure 1 14-pin ceramic package

Design: The SM28LVT32-HT was designed using Texas Instrument's 180nm flash CMOS process. This same process and flash intellectual property has been used in the development of two other production released extreme high temperature devices. The SM470R1B1M (Arm7 microcontroller), and the SM320F2812 (C2000 DSP)

The block diagram can be seen in Figure 2, and is comprised of the following blocks: SPI controller, flash controller, flash pump, and 8 flash banks. Each flash bank is consists of 8 sectors.
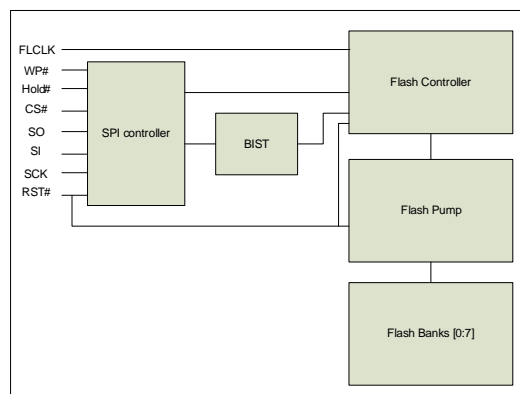

Figure 2 SM28LVT32 block diagram

Figure 3 shows the device physical floorplan and orientation.   Efforts were taken to allow testability access pins on the long axis of device,

while still maintaining aspect ratio suitable for down hole drilling constraints.
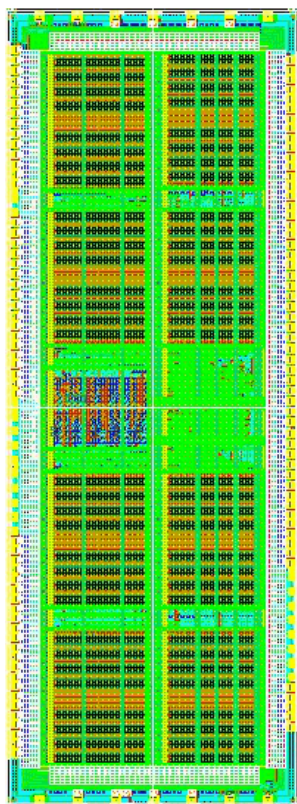

Figure 3 SM28LVT32 Floorplan

A flash memory is comprised of multiple levels of hierarchy. The lowest level is the bit-cell. For this technology, it is a transistor with an isolated floating gate See Figure 4. The bit-cells are organized into 64bit words. The words are organized into a sector, and sectors are organized into banks.

A single bank contains 8 sectors. A sector is the physical representation of the minimum block of memory that can be erased at one time. The sectors are created in balanced pairs by physical location with equal-distance to the sense amplifiers. Sectors 0 & 7, 1 & 6, 2 & 5, and 3 & 4 are balanced together. This is significant to user only in the event that the user desires to manage device erasure on sector by sector basis. For example, if a single sector is to be erased, then its matched balanced sector should be either erased or validated if data in that sector is to be maintained. This will insure that the differential sense amp methodology remains valid between the balanced pairs. If both sectors are erased,

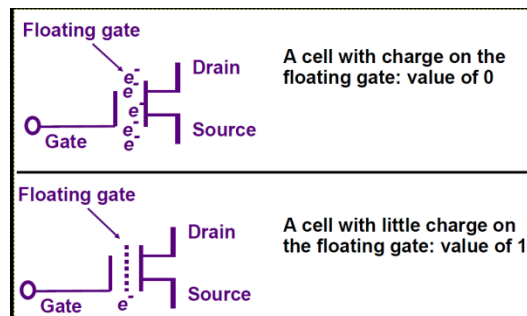then no user activity is required to maintain the balance.

Figure 4 Flash Bit-cell

The SM28LVT32 implements standard SPI modes for communication. It supports CS active low, with CPOL modes 0 and 3. Modes 0 and 3 represent SI sampled on rising edge of SCK, and SO launched from falling edge of SCK. Multiple SPI commands are implemented to facilitate writing (programming) and reading the array. Commands are a single byte, followed by several additional bytes that vary in meaning and length depending on the particular command. See Table 1 for command descriptions and SPI and framing information. See Figure 4 for SPI timing diagram.

A read command consists of the command byte 15h followed by three bytes of address, followed by one byte of dummy input, completing with 2 bytes of data on SO with result. During the SI dummy byte shift-in, the read address is transferred to the internal flash controller and the data at the specified address is read and transferred back to the SPI controller to shift out during the SO bytes. The parenthetical number on the dummy bytes on SI column in Table 1 represents the total dummy data on SI, including the overlap with data on SO being output. The next command 16h is also a read command. This is identical to prior read command with the exception that the address is auto incremented from last address, thus the command is three bytes shorter only requiring four bytes in the frame. The write word command is very similar, and begins with the command byte 17h, followed by three bytes of address, two data bytes and a single dummy byte. It is important to note that successive back to back writes is not necessarily possible. A write takes time to complete, and a new write must not be sent until prior write is

Table 1 SPI commands

COMMAND NAME	COMMAND BYTE ON SI	ADDRESS BYTES ON SI	DATA BYTES ON SI	DUMMY BYTES ON SI	DATA BYTES ON SO	TOTAL BYTES IN FRAME	DESCRIPTION
Read Word	15h	3	0	1 (3)	2	7	Read word at given address
Read Word with auto addressing	16h	0	0	1 (3)	2	4	Burst read from previous address
Write Word	17h	3	2	1 (1)	0	7	Write word at given address
Write Word with auto addressing	18h	0	2	1 (1)	0	4	Burst write from previous address
Erase segment	19h	3	0	1 (1)	0	5	Erase addressed segment
Validate segment	1Ah	3	0	1 (1)	0	5	Validate (compact) segment
Read Status Register	22h	0	0	0 (2)	2	3	Read SPI status register
Write Command	1Fh	0	2	1(1)	0	4	Flash controller command interface for special functions. See Application section
Quick Status	FFh	0	0	0	0	1	Obtain Quick Status bits
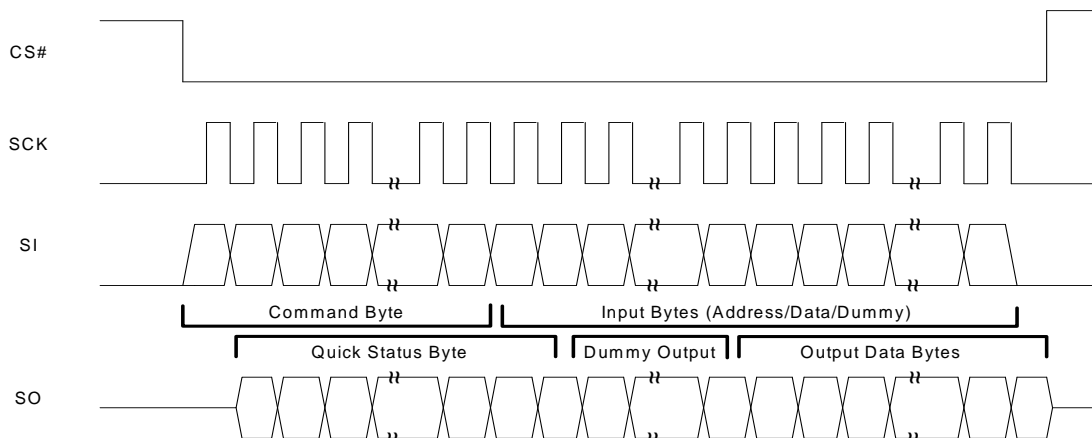
Figure 5 SPI Timing Diagram

complete. This is further discussed with respect to application requirements later in this article.

The erase command (19h) requires 5 bytes in the frame to execute. The erase will take a finite amount of time to complete. The erase command is actually comprised of 3 sequential internally controlled operations. First the flash controller will completely program the sector to all 0s. Then it will erase the entire array to 1's. After erasure, a compaction (validation) will occur. The validation is essentially a soft programming to prevent over erasure (depletion). The erase command is similar to the write command, as such a new command to the

memory should not be executed until the prior command has completed. The mechanism the host must use to determine if a command is still executing or been completed successfully is in the assessment of the quick status bits. These are the first 8 bits that are output on any SPI transaction.

See table 2 for quick status representation

Table 2 Quick status results mapping.

BIT	DESCRIPTION
7	Unused
6	SPI frame error: indicates frame ended with less than required bytes to complete
5	Write busy: indicates that a program operation is in progress
4	Erase busy: indicates that a sector is being erased
3	Device busy: logical of all possible busy sources (Read, Erase, Program, and test functions)
2	Invalid data: indicates that an attempt was made to set a bit to 1 that has already been programmed to 0
1	Read error: indicates that read was attempted on address when data was not available
0	Command error: indicates that prior command failed. Must be cleared.

Bit 6 indicates that upon de-assertion of CS, the command was recognized as a valid command, but the correct number of bytes was not provided. Thus an error was generated. If the correct number of bytes is not sent, the command may not have completed correctly. In case of a read command then the data returned was not complete. Bit 5 represents that a write is in progress. The host must use this bit to determine if it can continue with the present command being sent. There are several ways to handle this. This is discussed later in the document with respect to application usage. Bit 4 represents that an erase is currently in progress. Bit 3, is a combination of all potential busy flags internal to the device. Including Write, erase, read (not normally seen), and some testability flags. Bit 2 is an error that will indicate that the host has attempted to write a word into a location that has data already programmed, and it cannot physically write this data. For example, a bit is already programmed to a 0, but the new word being written has this bit at the erased state of 1. This is physically impossible, and thus an error is generated. Bit 1 represents a result indicating that the last read failed due to data not being ready when attempted to be read. This is not a normal error that would be seen, and is related to some advanced functions that will be validated and documented in the near future. This error bit is self clearing. The final bit indicates that the last command failed for some reason. There are several reasons for a failure. If this failure is due to an erase, then this indicates that the erasure failed due to a read verify. This indicates that some of the bits did not read 1 at completion of algorithm. If this error is generated after programming, then it indicates that the word was not able to be written after the algorithm completed. Both the Invalid data and the command error bit are sticky. They will not self clear. This special case requires the host to clear the bits by executing a special command. This command is 1F 00 40 xx xx. Where xx xx are

000069
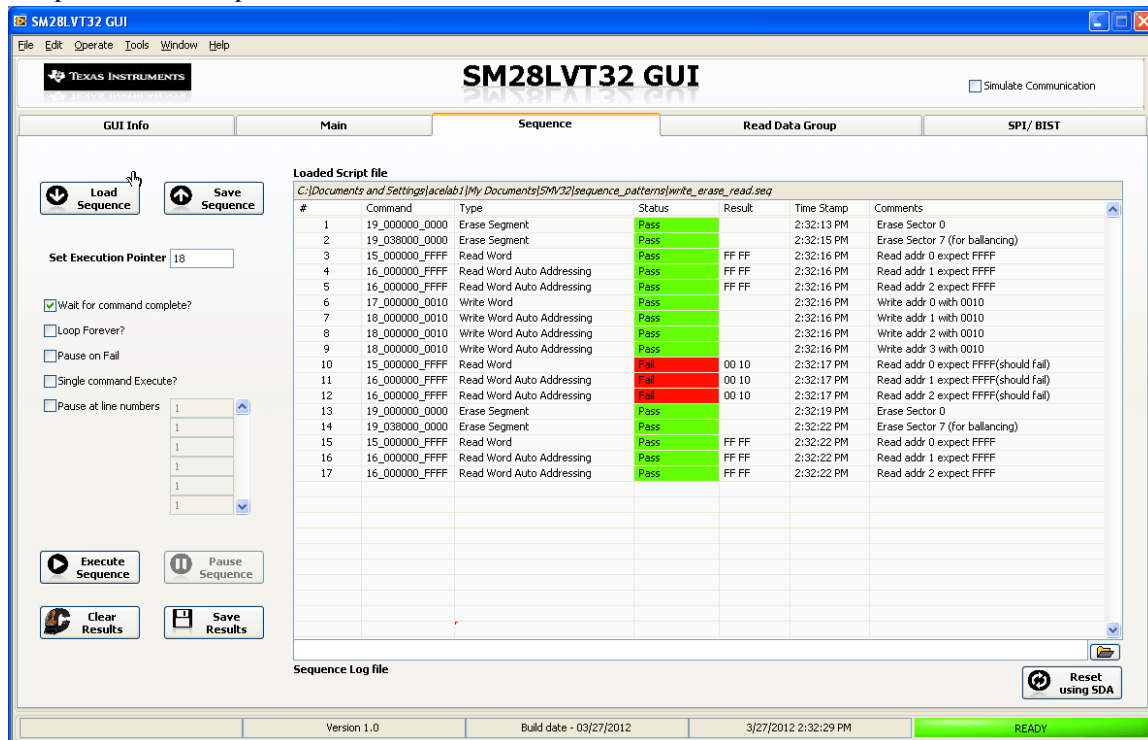
Figure 6 SM26LVT32 GUI

two don't care bytes. The 1F command is a special command that allows the host to send instructions to the internal Flash controller. The h40 instruction clears an internal status register storing the errors.

The internal flash controller is a complex state machine that is managing all aspects of internal reading, programming, and erasing of the flash array. The erase and programming algorithms contain time critical loops. These loops are pre-configured for operation with at 12Mhz FCLK. The design has the ability to modify the flash controllers register settings to allow for alternate slower frequencies. Modification and description of these registers is outside the scope of this article. Application notes will be made available for applications requiring lower than the datasheet specified12Mhz clock frequency.

Application:

There are several methods that a host can use to manage successful and efficient communications with the SM28LVT32. It is envisioned that the host will poll for the completion of a command for any command that is queued. In this case, the host can either start to send the next command, and evaluate the quick status bits. If the memory is still busy, it can abort the transaction, and resubmit until device is no longer busy. This will have the side effect of frame errors being generated due to the aborted command. A simpler method, but not as efficient would be to use the FFh quick status command. If prior command is no longer busy, then resume with next command This will not generate the frame errors as in prior example. The only commands that are not queued are the read command and status register read command. They do not require polling, as the result is immediately furnished. An exception to this will likely be introduced in the future with the read error. The read error is intended to notify host for cases when device is not ready and the error will be generated. This error will not occur, unless some advanced memory configurations are employed. These advanced configurations/features will be documented in near future.

EVM/GUI:

To facilitate device checkout and temperature testing, an EVM and software GUI have been developed. The version of the EVM that will be available upon device release will be 210c capable.

The software GUI allows complete operation of the flash. The GUI can perform sequence (scripted) actions with or without polling. The scripting language allows for easy command generation without needing to know specific formats for each command. Additionally the capability to flag read errors by utilizing an expected value in the sequence file. The GUI can also dump the full array to file for examination. See Figure 6. The GUI and hardware utilizes 3rd party hardware for SPI transactions between the flash memory and the PC. The hardware utilized is the Cheetah SPI Host adapter from TotalPhase.com.

Design for Test:

The flash controller was extracted from an embedded flash architecture designed to interface with a host microcontroller through a bus. The architecture employs a state machine designed into a wrapper that performs all overhead associated with program, erase & comprehensive testing of the flash array and the flash pump module. See Figure 7. Access to the test port, parallel port and direct access PMT (Parallel Multiplex Test) mode pins are not available in the final production package. These pins are accessible for TI internal use through special test modes during wafer level testing and within a special package designed for internal characterization across temperature.
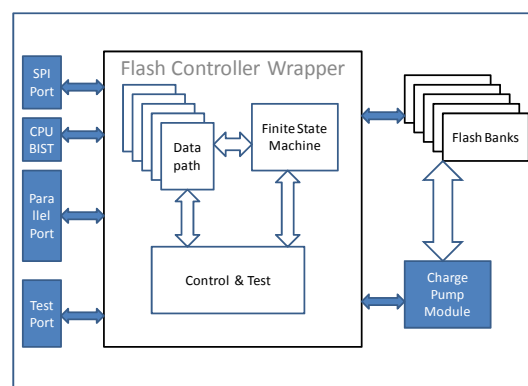

Figure 7 Flash Controller

The flash controller has internal control and test registers. The controller provides access to several data-paths that can be interfaced with a CPU (not available on this design), SPI, parallel port or test ports.

In addition to the test & parallel port, a BIST controller state machine is embedded for TI

internal use for further characterization. The BIST state machine can be controlled and provided the start & end address, read out the done, fail or diagnostic modes with accessibility though SPI.

Also a scan test mode is inserted to invoke scan stuck-at tests to the wrapper logic & controllers, multiplexers and state machines.

Equipped with scan, bist, parallel port, test port and direct access to a few key flash pump voltage and timing measurements, this device can be extensively characterized at different temperatures and frequencies, and production screens implemented to yield the optimum material specific to the High Temp application profile needs.

Tests developed include full-array program, erase, validate in different algorithms such as checkerboard, inverse-checkerboard, walking 1s etc. The flows developed for data-retention at wafer & package level pre & post-bake; endurance tests, scans, core & pump dynamic/static power dissipation measurements, pin leakage etc.

Flash Test flow:

The flash array is extensively tested & characterized at various temperatures up to 210C & frequencies up to 20 MHz on material from different fabrication lots, to ensure robustness of design, as well as, production quality throughput.
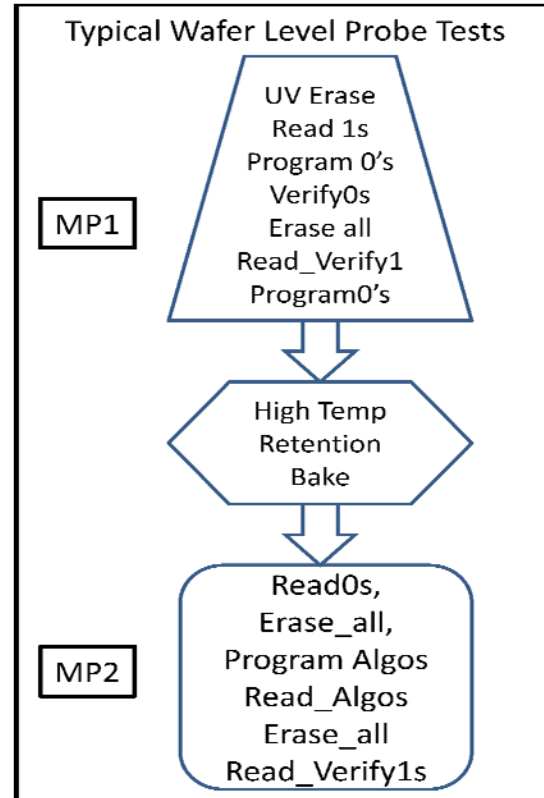

Figure 8 Wafer Probe Flow

After the wafers are received from the fab, it is back-grinded to optimum thickness, and tested for basic functionality followed by full array tests. The wafers are baked at high temperature for custom duration for outlier screens at MP2. See Figure 8. Additional comprehensive tests are performed at MP1 and MP2 including scan, performance, parallel port, BIST, pin leakage etc to ensure operation at temperature derived from characterization & qualification tests. Package level testing utilizes some of the same extensive tests as wafer probe in addition to other tests.