Solid State Equipment LLC

Silicon Wafer Thinning to Reveal Cu TSV

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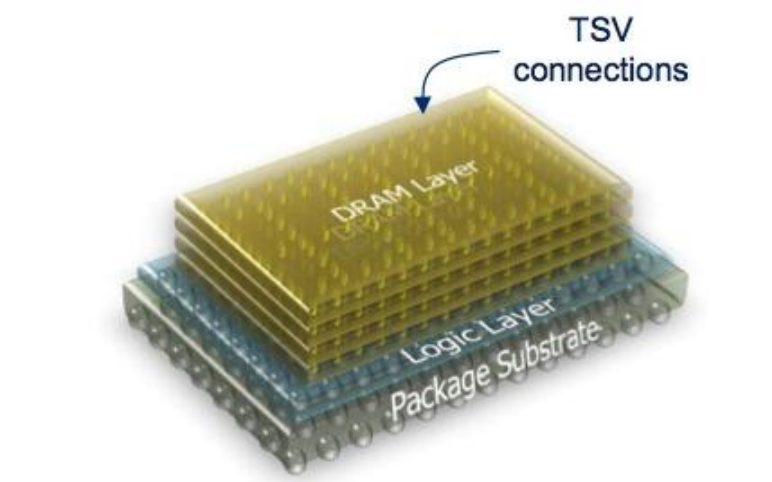
IMAPS Device Packaging Conference 2012

Outline

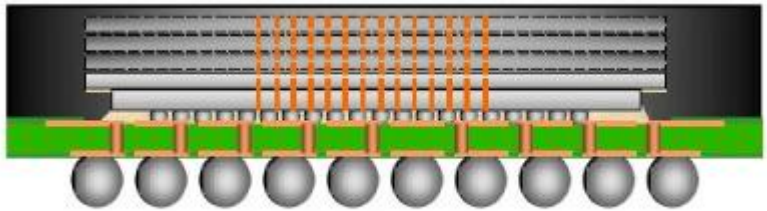
- Background
- Wafer thinning to reveal Cu TSV
- Silicon etch with KOH
- Process results
- Integrated Wafer Thickness Measurement
- Summary

Background

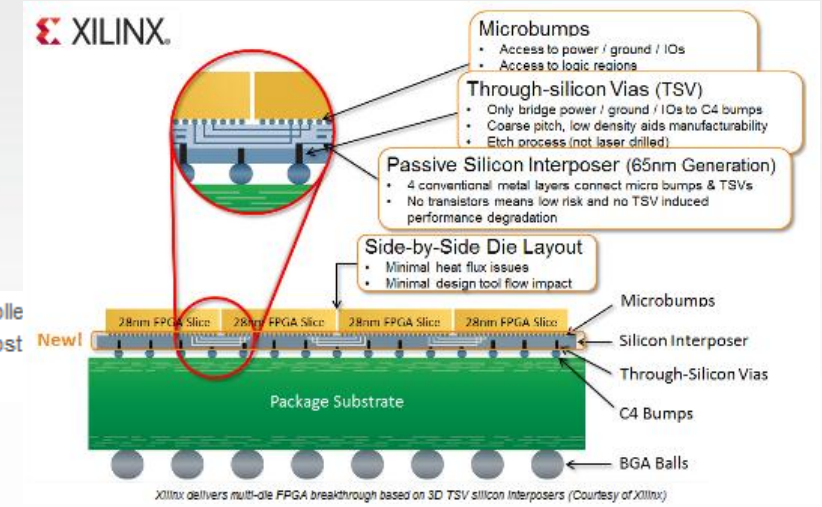
Examples of TSV to increase performance



Micron uses through-silicon via (TSV) technology to stack memory on top of a controlle chip ('logic layer'). The on-chip controller is the key to delivering the performance boost (Credit: Micron Technology)

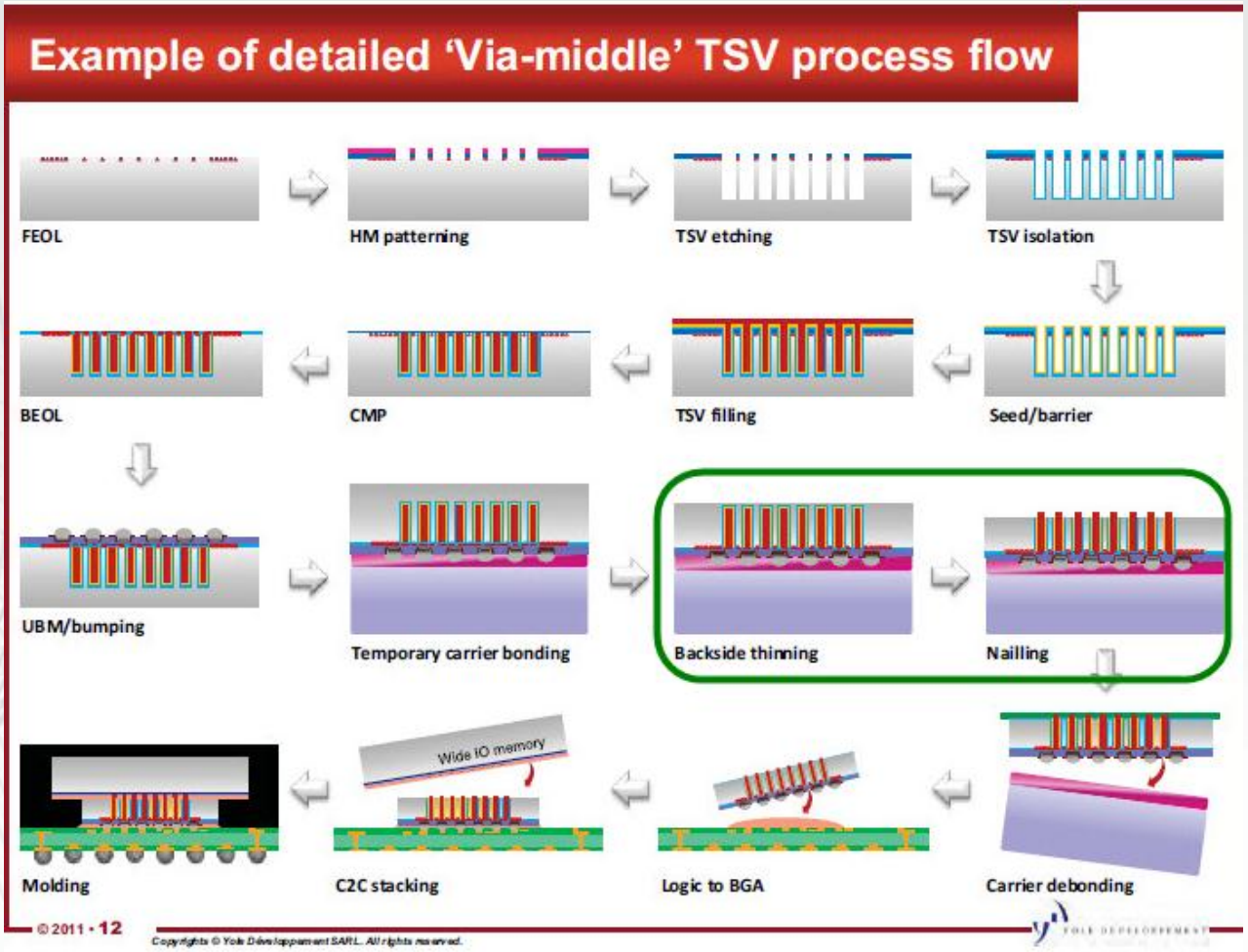


Nokia's wide I/O memory interface to Mobile CPU is expected to hit market by 2013

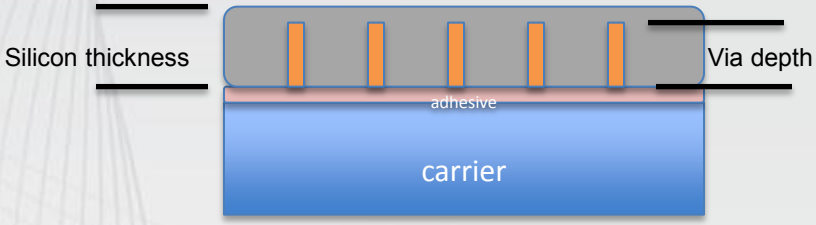


Xilinx delivers multi-die FPGA breakthrough based on 3D TSV silicon interposers (Courtesy of Xilinx)

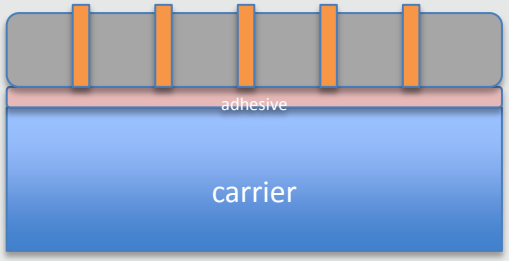
Wafer Thinning to Reveal TSV



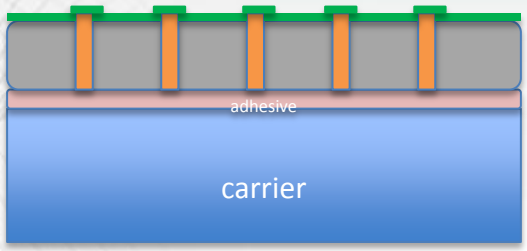
TSV Reveal, Protect and Planarize



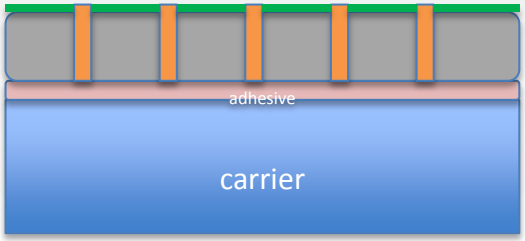
Post Grind



After Si Etch – TSV Revealed



Oxide/Nitride deposition to protect Si surface from Cu



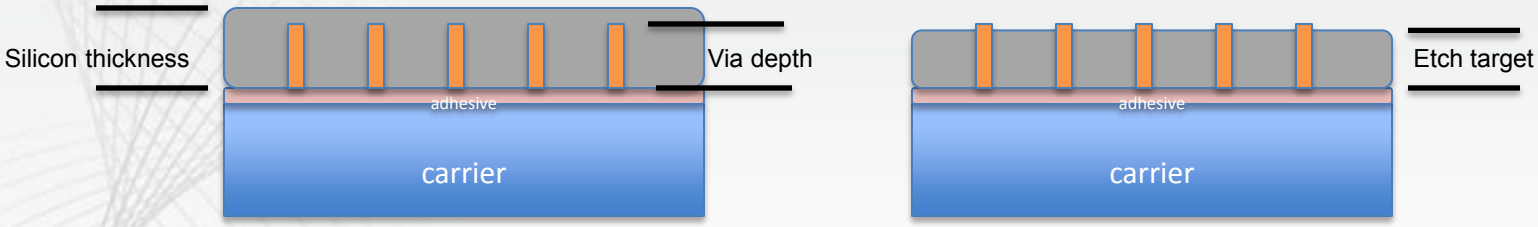
Surface planarized and Cu vias exposed

TSV Reveal: Process Options post Grind

CMP	Silicon Recess Etch	Wet Etch
CMP to smooth surface, remove defect zone and expose Cu	Partial CMP to smooth surface, remove defect zone	KOH etch to expose via without etching oxide liner
Chemical clean to remove Cu contamination from Si surface	Silicon recess plasma etch to expose via without etching oxide liner	Seal with low temperature oxide/nitride
Seal with low temperature oxide/nitride deposition	Seal with low temperature oxide/nitride	CMP to planarize and expose Cu vias
Litho step to expose Cu vias	CMP to planarize and expose Cu vias	

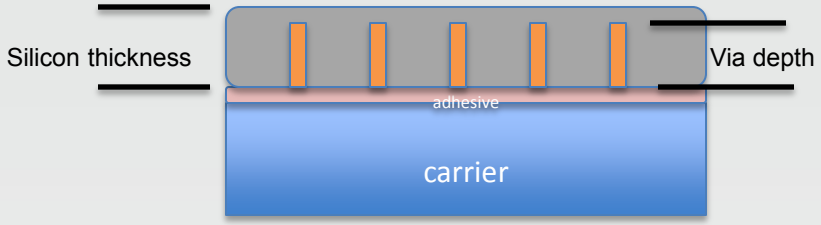
Wafer Thinning to Reveal Cu TSV

- Device wafer on carrier
- Grinding process used to get within 10-20µm of Cu TSV
- Wet etch process to reveal Cu TSV
  - Use of KOH to etch Silicon without attack of Cu via or Oxide liner



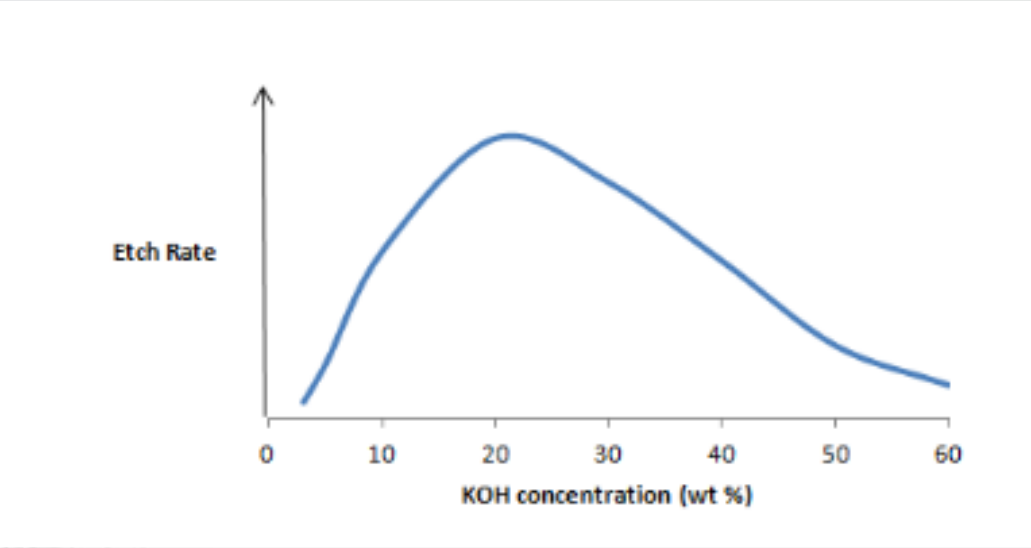
Integrated Thickness Measurement

- Need to know
  - Silicon thickness post grind
  - Uniformity of Silicon
  - Via depth
- Use of integrated measurement provides
  - Silicon thickness and radial thickness variation
  - Etch rate feedback from previous wafer
- Determine amount of Silicon to etch
  - Average silicon thickness to be removed
  - Radial profile of etch



Example	Thickness Post Grind	Via depth	Etch depth to reveal
nominal case	65	55	12
thicker silicon	70	55	17
thinner silicon	60	55	7
shorter via			
nominal case	65	50	17
thicker silicon	70	50	22
thinner silicon	60	50	12
longer via			
nominal case	65	60	7
thicker silicon	70	60	12
thinner silicon	60	60	2

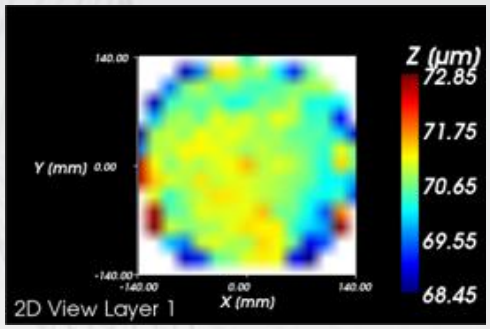
KOH etching of Silicon



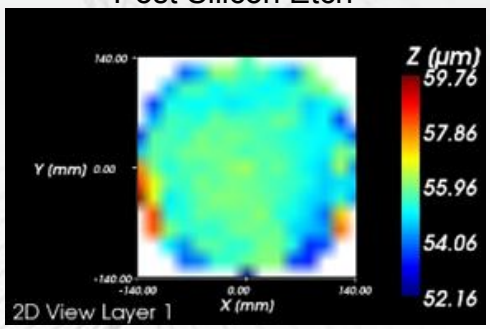
$$Si + 2OH^- + 2H_2O \rightarrow SiO_2(OH)_2^{2-} + 2H_2$$

Single wafer spin etching

Post Grind



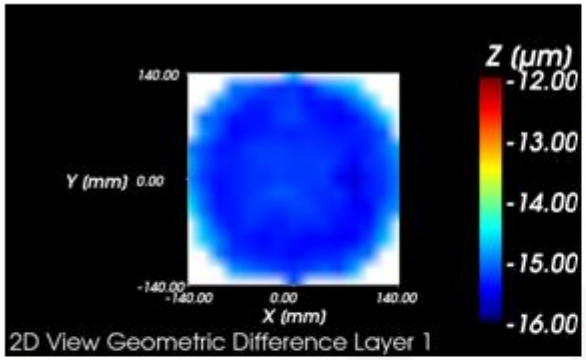
Post Silicon Etch



- Post Grind non-uniformities can have radial dependence
  - Center to edge variations
- Single wafer etch process can compensate for radial non-uniformities
  - More/Less etch in center of wafer
- Resulting Silicon wafer thickness is more uniform

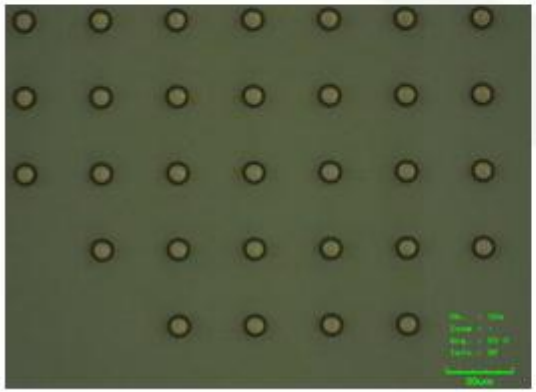
Wafer Thinning to Cu TSV

Uniform etching of the silicon:

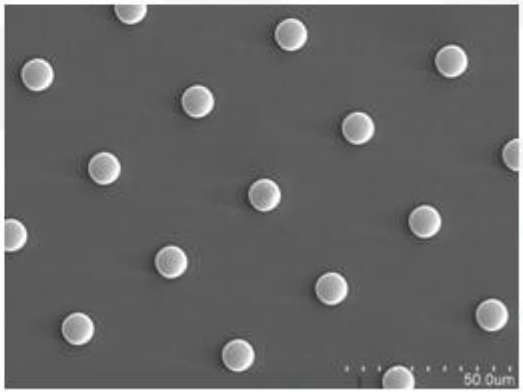


Mean: -15.259 µm
Maximum: -14.50 µm
Minimum: -15.67 µm
TTV: 1.18 µm
StdDev: 0.20 µm

In the example shown above, 15µm of silicon was etched in order to reveal the Cu vias.

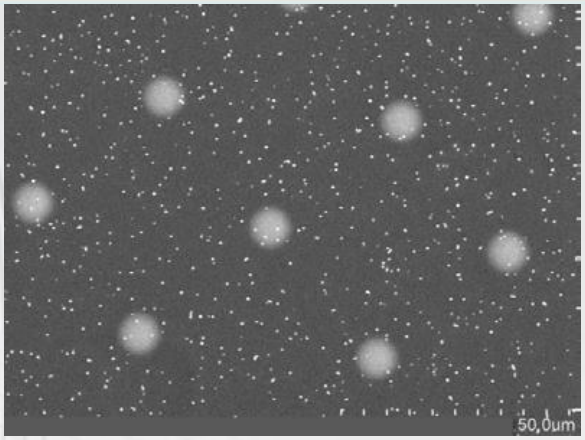


Optical image of revealed Cu vias

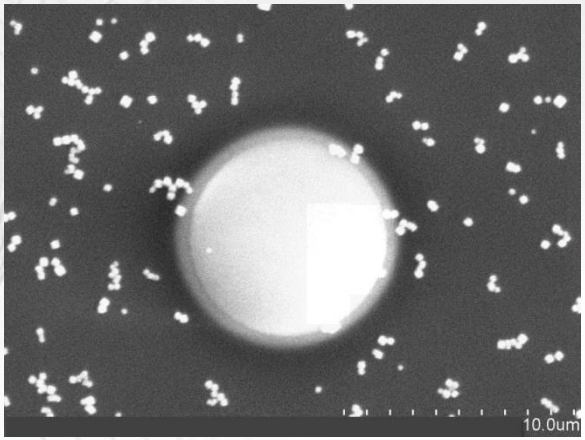


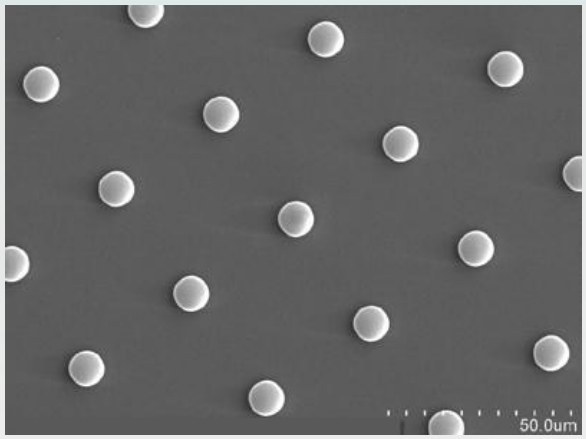
SEM image of revealed Cu vias

KOH etching of Silicon requires Post Clean

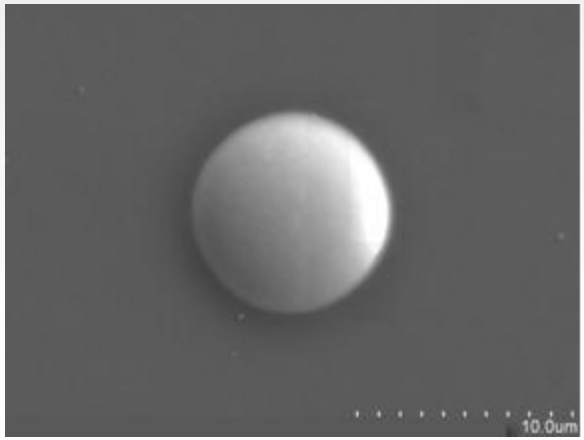


Post Etch





Post Clean

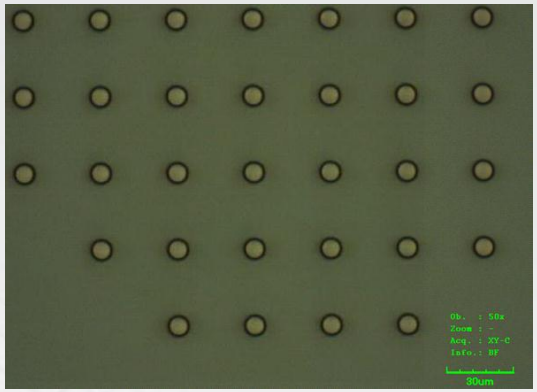


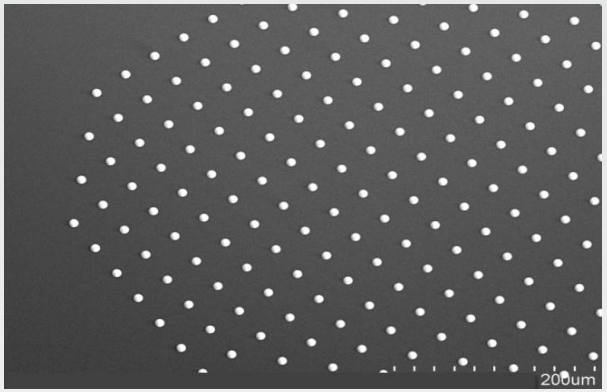
Wafer Thinning to Cu TSV

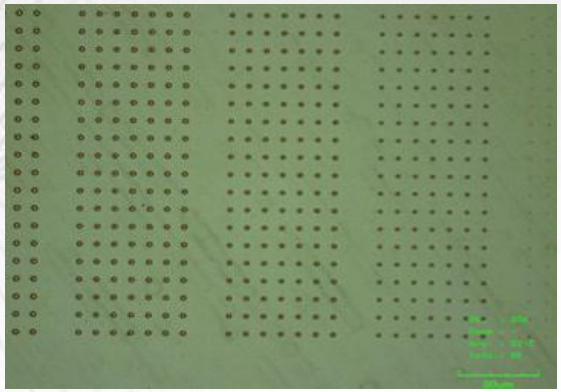
			Surface Concentration (x 10^{10} atoms/cm2)		
		Method Detection Limit	Control	KOH etch	KOH etch + Clean
Potassium	(K)	0.2	61	170	0.47

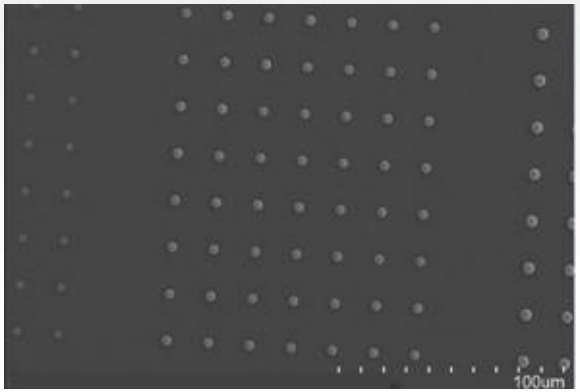
VPD-ICPMS measurements indicate the cleaning process is effective at removing the residual Potassium from the etch process.

TSV revealed post etch and clean

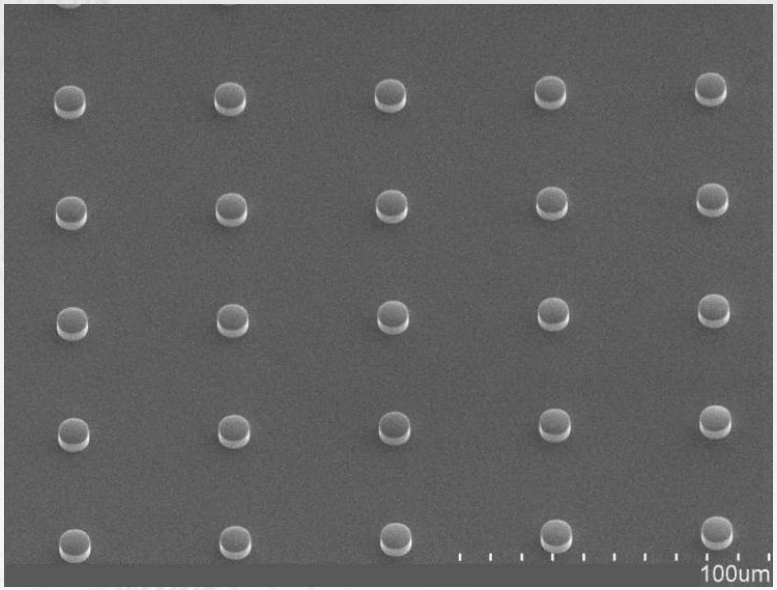


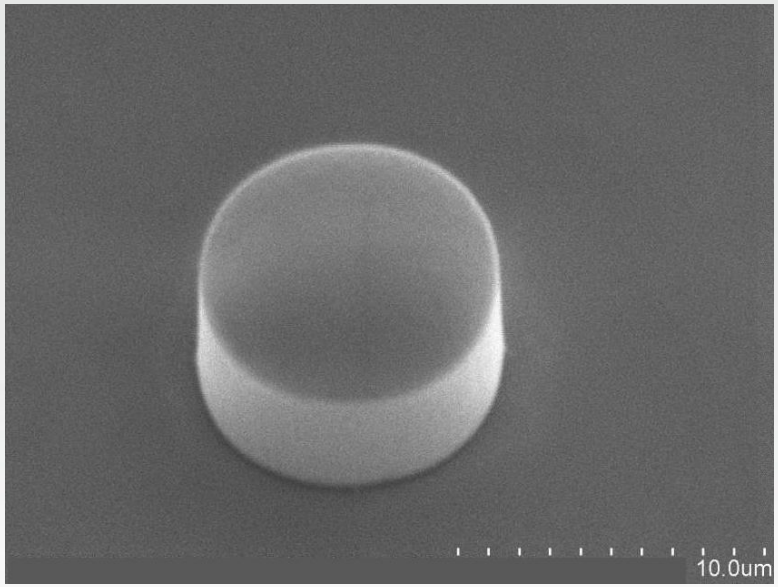






TSV revealed post etch and clean

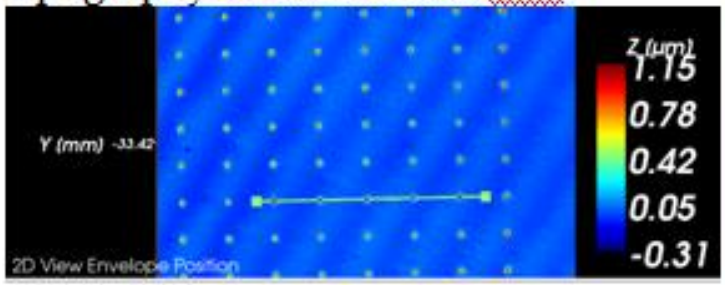


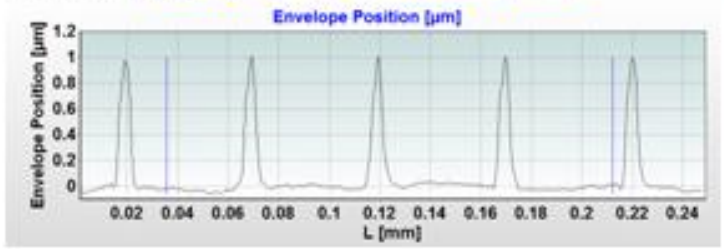


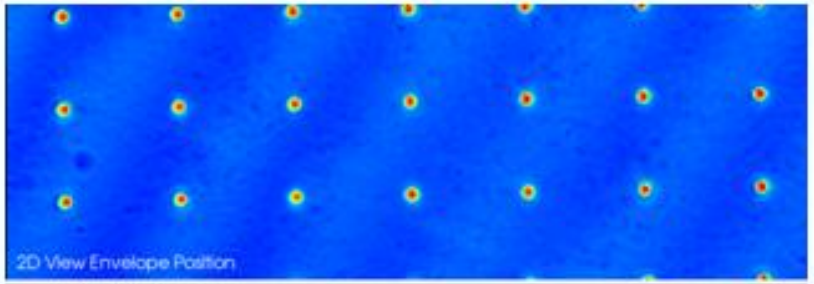
Wafer Thinning to Cu TSV

Topography Measurements

The ISIS Sentronics Wafer Inspection System provides capability to measure the topography of the revealed vias.



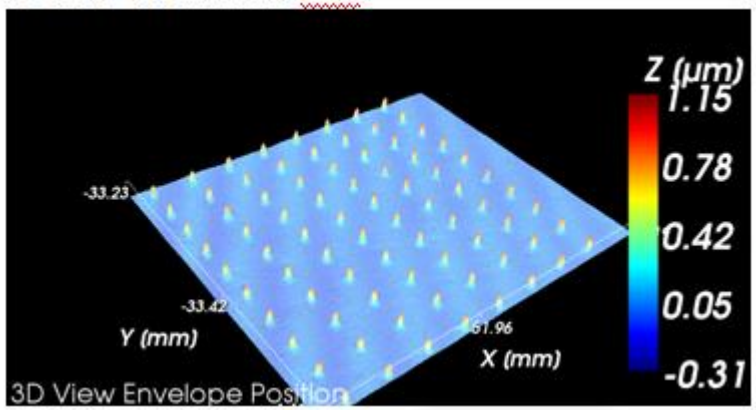




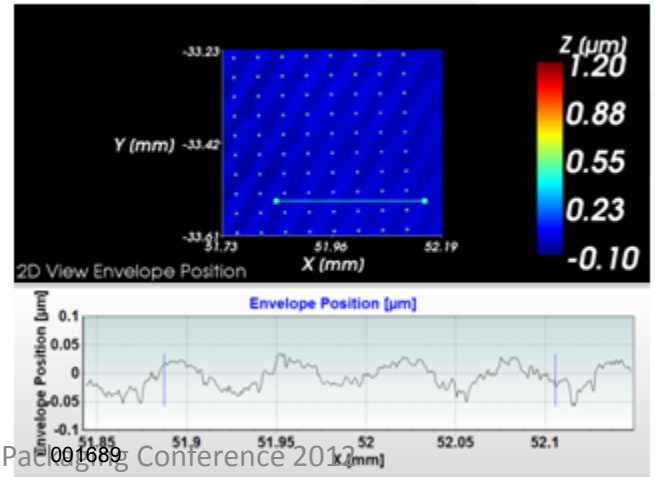
Site	Bump	X [mm]	Y [mm]	r [um]	h [um]
1	1	51.764	-33.603	2.291	-0.169
1	2	51.813	-33.602	2.291	-0.259
1	3	51.863	-33.601	2.291	-0.238
1	4	52.113	-33.595	2.644	-0.192
1	5	51.762	-33.563	2.291	-0.228
1	6	51.757	-33.284	2.291	-0.256
1	7	52.106	-33.276	2.468	-0.294
1	8	51.756	-33.244	2.468	-0.322
1	9	52.105	-33.236	2.468	-0.267

Wafer Thinning to Cu TSV

3D view of revealed vias



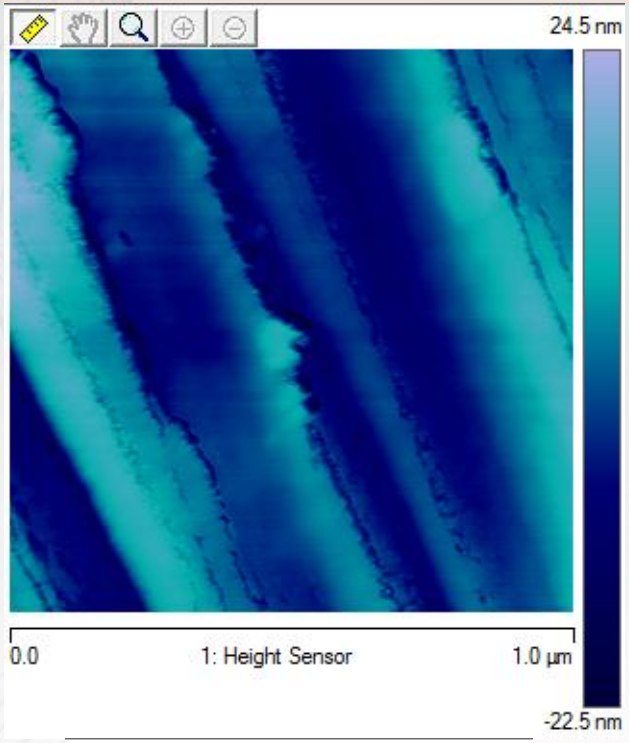
Surface roughness

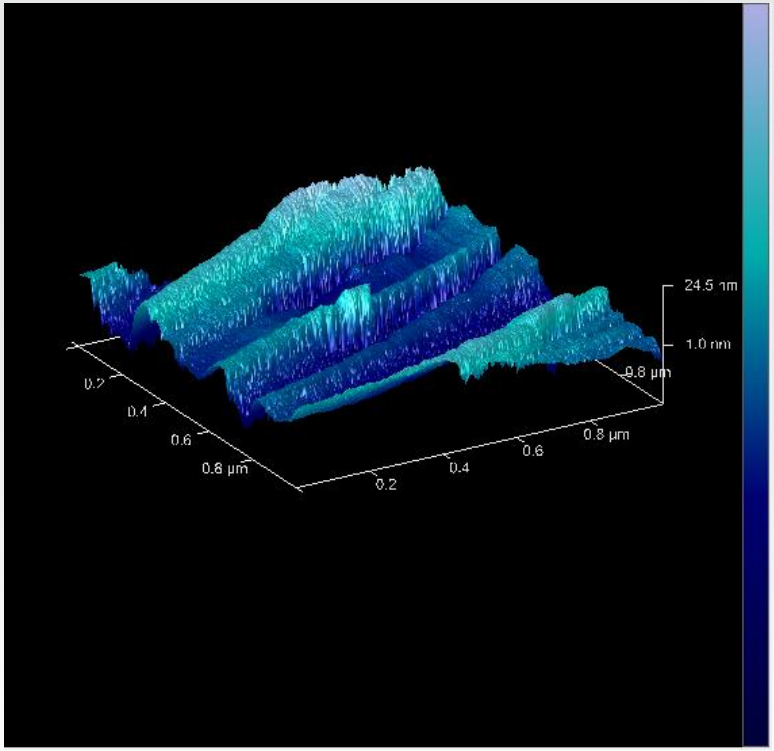


Envelope Position Roughness

Ra2D: 0.02516 µm
Rq2D: 0.07995 µm
Rt2D: 1.12796 µm
Rz max: 0.05912 µm
Rz: 0.04572 µm
Ra: 0.01040 µm
Rq: 0.01260 µm
Rt: 0.06343 µm
Rsk: -0.33500 µm
Rku: 2.49863 µm
Rsm: 36.21939 µm
Rv: 0.02674 µm
Rp: 0.01897 µm
Lc: 80.0 µm
Ls: 2.5 µm

Surface Roughness after Grind

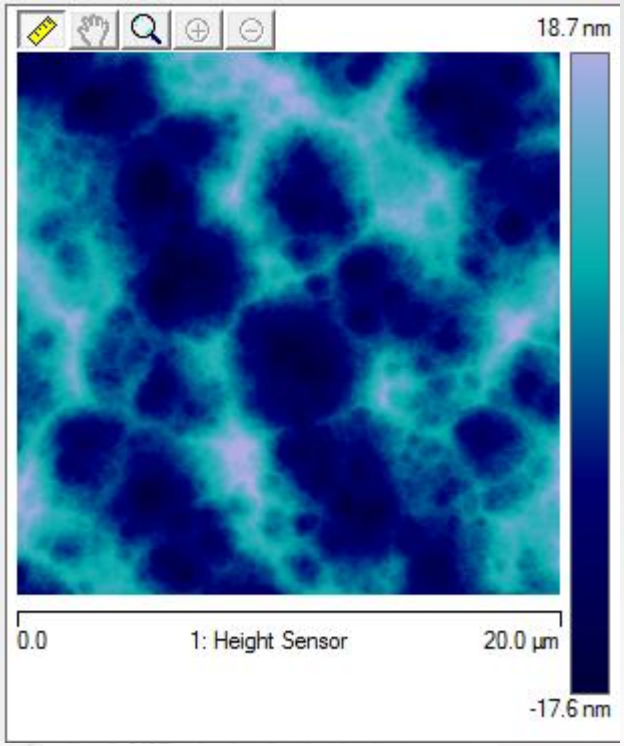


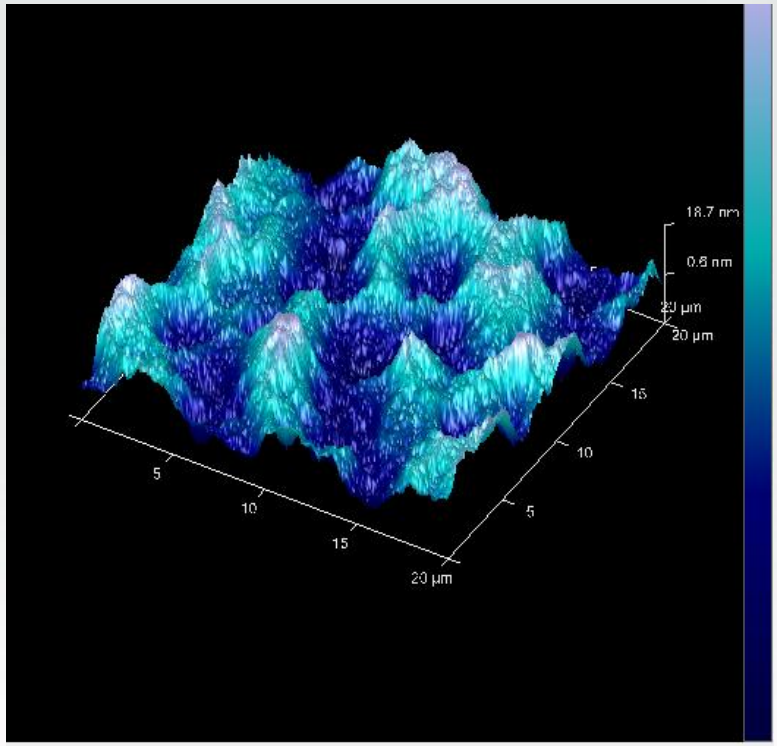


Results

Image Raw Mean	-344 nm
Image Mean	0.000000 nm
Image Z Range	58.5 nm
Image Surface Area	1100264 nm²
Image Projected Surface Area	1000000 nm²
Image Surface Area Difference	10.0 %
Image Rq	7.35 nm
Image Ra	6.00 nm
Image Rmax	58.5 nm

Surface Roughness post KOH etch

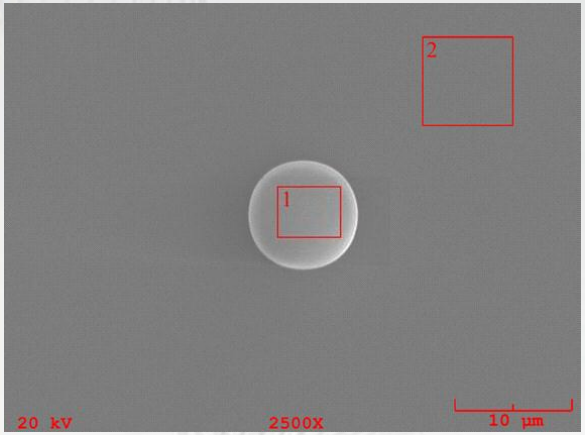


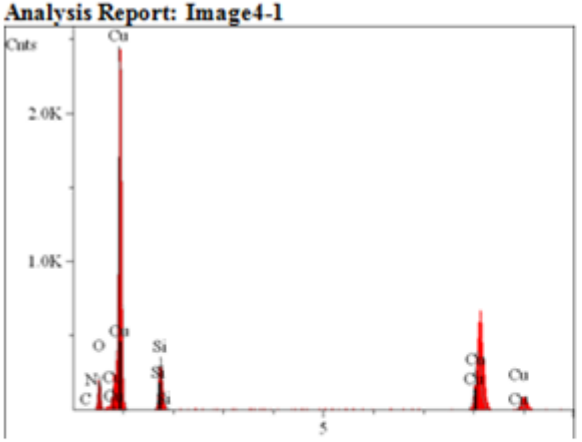


Results

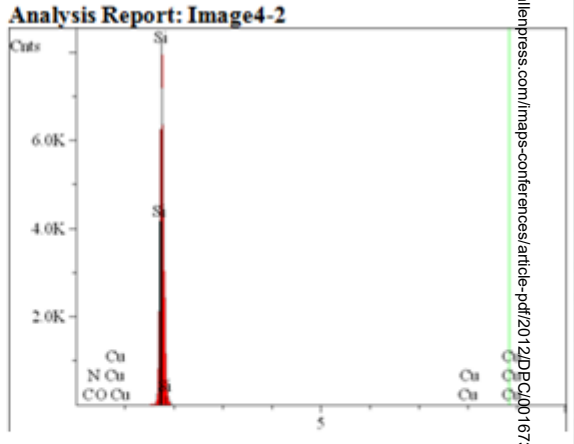
Image Raw Mean	0.000056 nm
Image Mean	0.000056 nm
Image Z Range	42.4 nm
Image Surface Area	400 µm²
Image Projected Surface Area	400 µm²
Image Surface Area Difference	0.0141 %
Image Rq	7.72 nm
Image Ra	6.36 nm
Image Rmax	42.4 nm

Wafer Thinning to Cu TSV





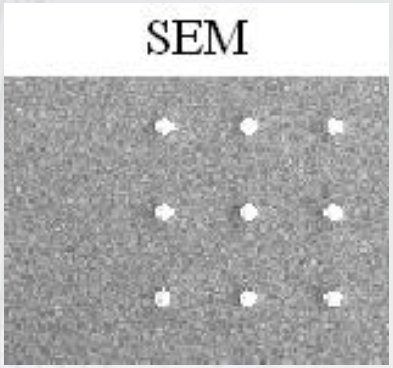
Elt.	Line	Intensity (c/s)	Error 2-sig	Conc	Units	
C	Ka	0.00	0.000	0.000	wt.%	
N	Ka	0.36	0.154	0.586	wt.%	
O	Ka	28.40	1.376	17.925	wt.%	
Si	Ka	55.21	1.918	15.715	wt.%	
Cu	Ka	102.63	2.615	65.774	wt.%	
				100.000	wt.%	Total

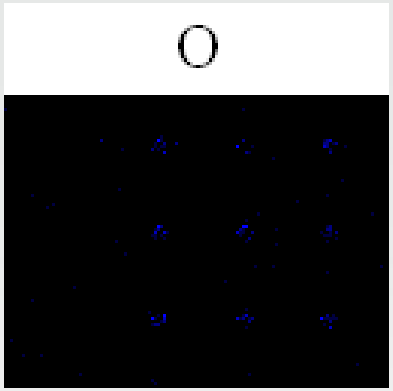


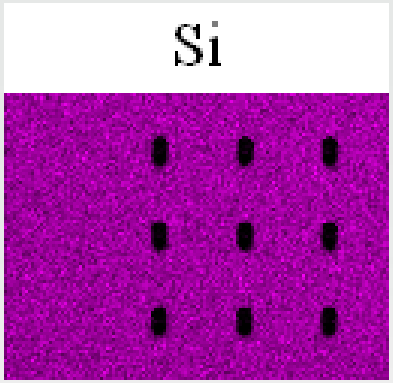
Elt.	Line	Intensity (c/s)	Error 2-sig	Conc	Units	
C	Ka	0.00	0.000	0.000	wt.%	
N	Ka	0.00	0.000	0.000	wt.%	
O	Ka	0.09	0.079	0.070	wt.%	
Si	Ka	1,156.43	8.780	99.512	wt.%	
Cu	Ka	0.98	0.256	0.419	wt.%	
				100.000	wt.%	Total

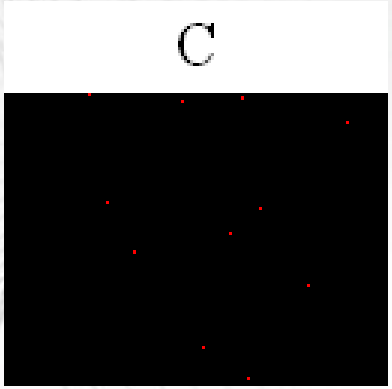
EDX analysis shows the oxide liner and Cu via remain intact

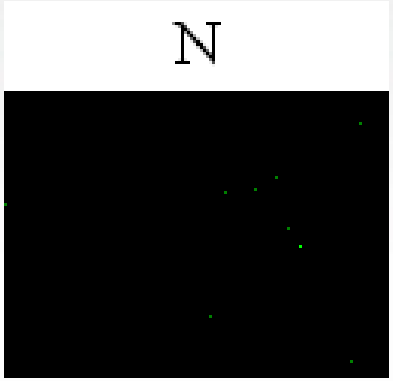
EDX Map

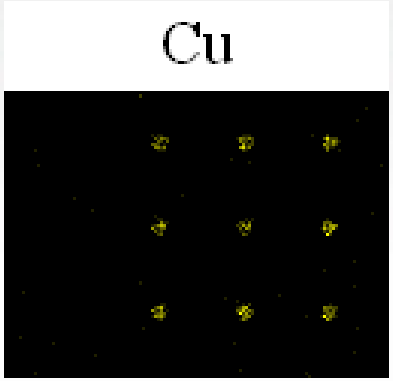






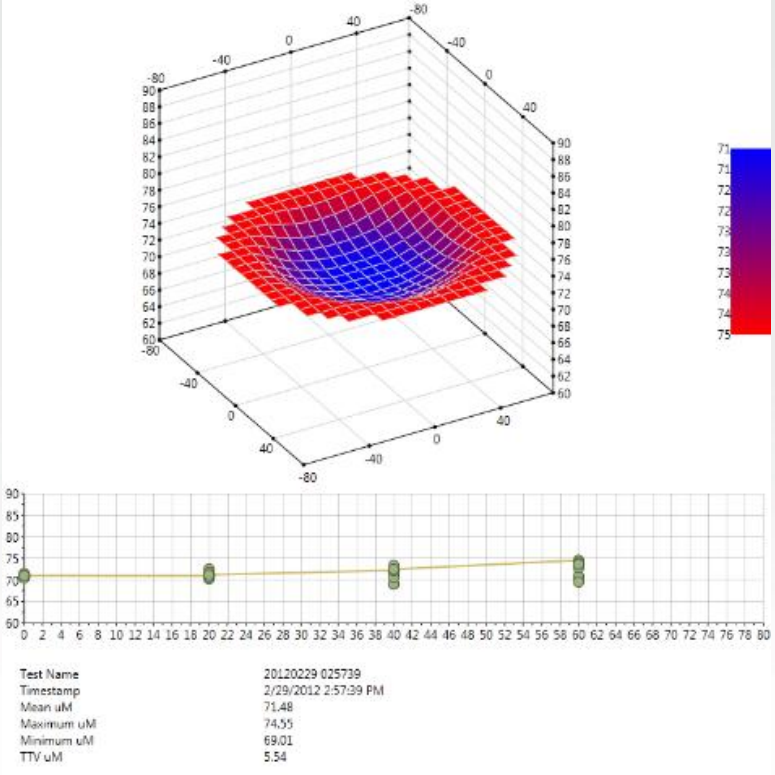




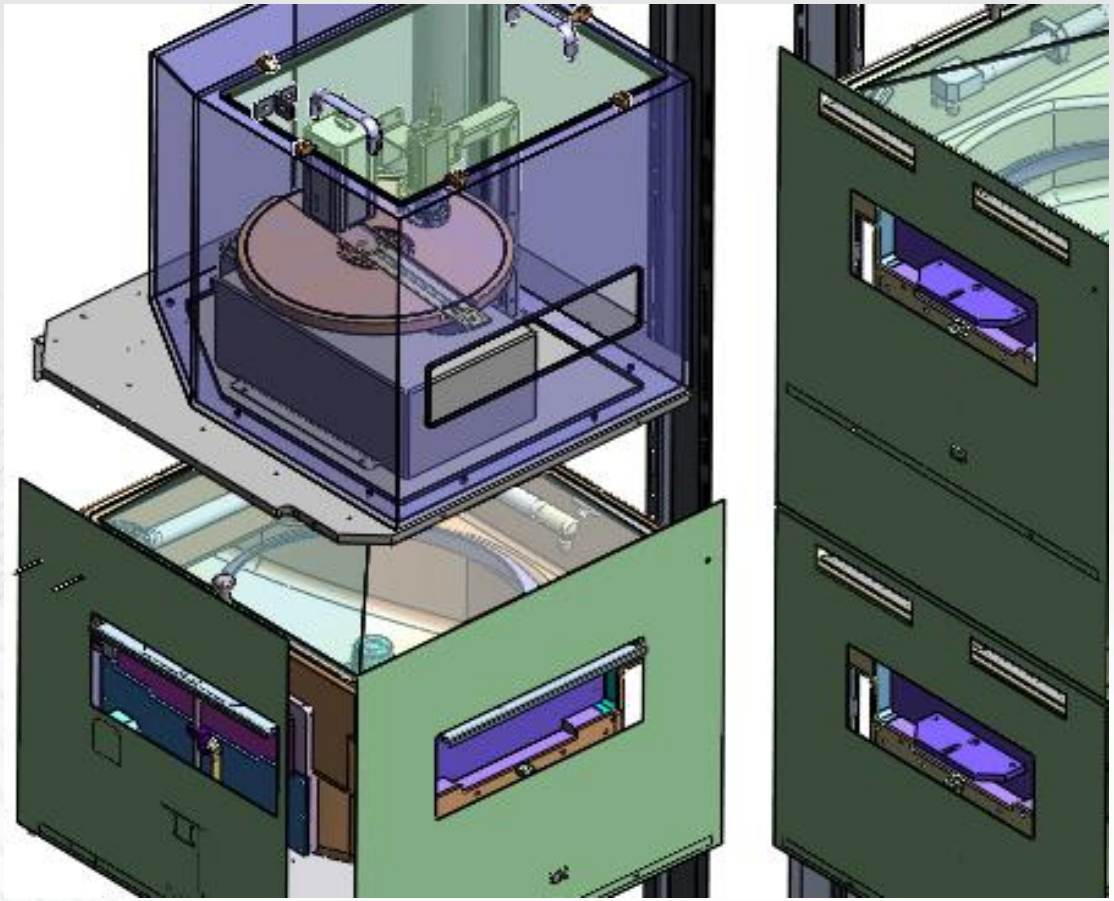


Integrated Wafer Thickness Measurement: Process Control

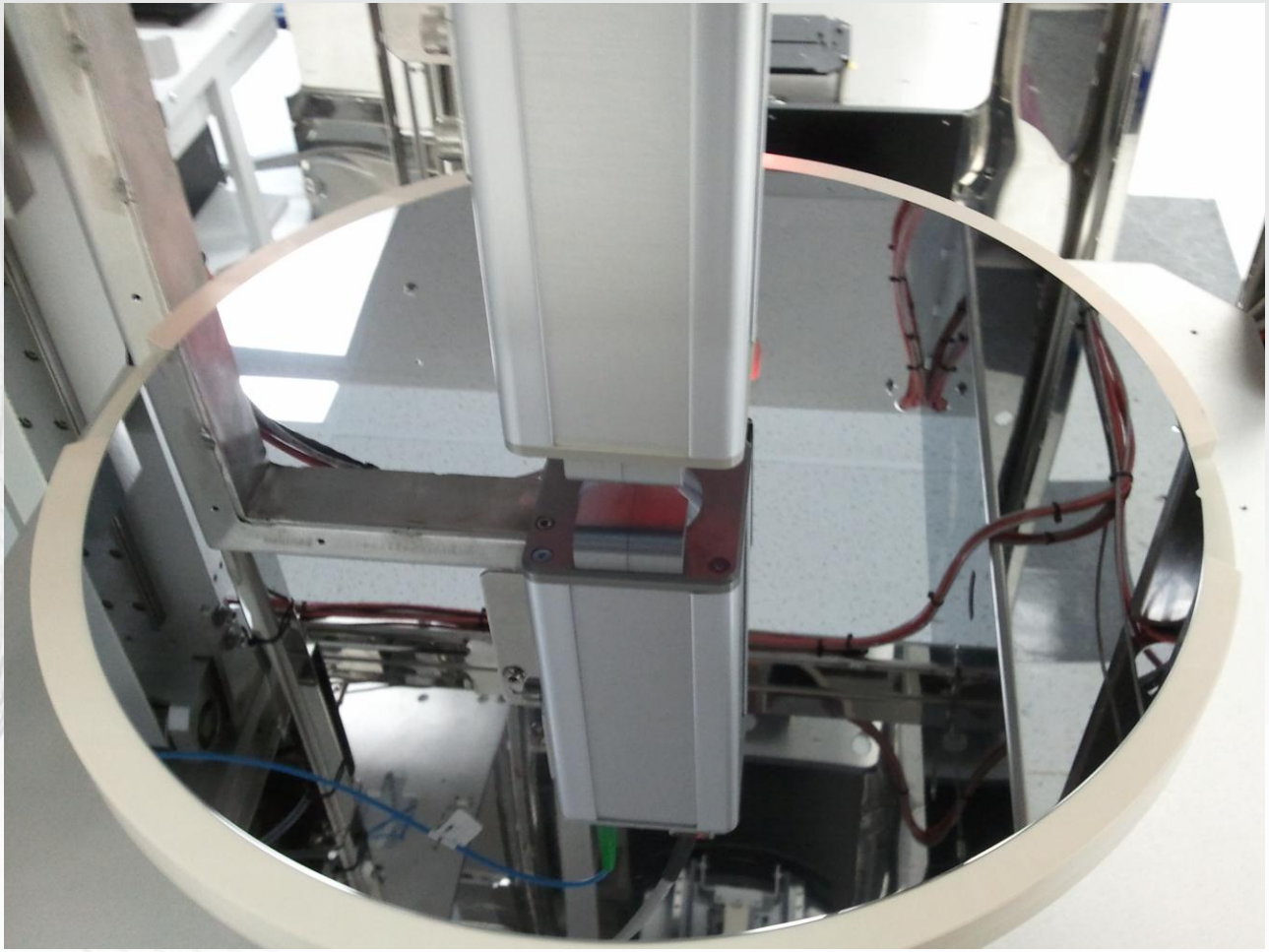
- Create map before etch
- Create map after etch
- Compute etch rate
- Compute etch uniformity
- Spike chemistry
- Determine etch time



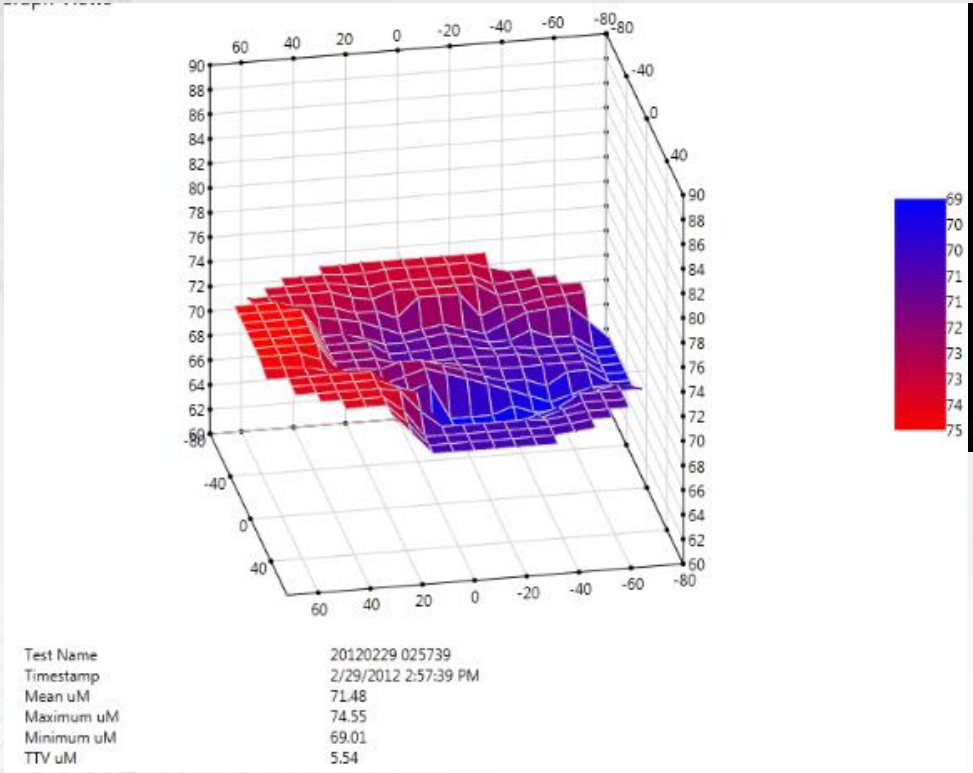
Integrated Wafer Thickness Measurement

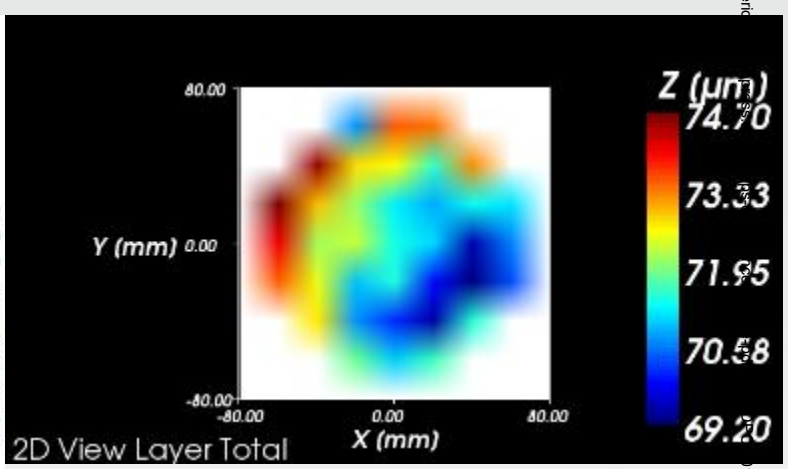


Integrated Wafer Thickness Measurement



Wafer Thickness Measurements





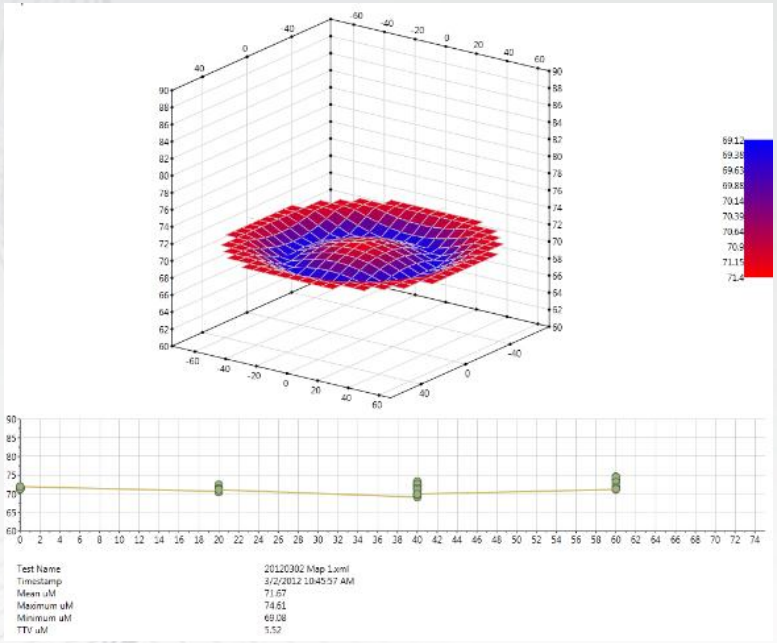
Layer Total Statistics

Mean: 71.744 µm
Maximum: 74.70 µm
Minimum: 69.20 µm
TTV: 5.50 µm
StdDev: 1.39 µm

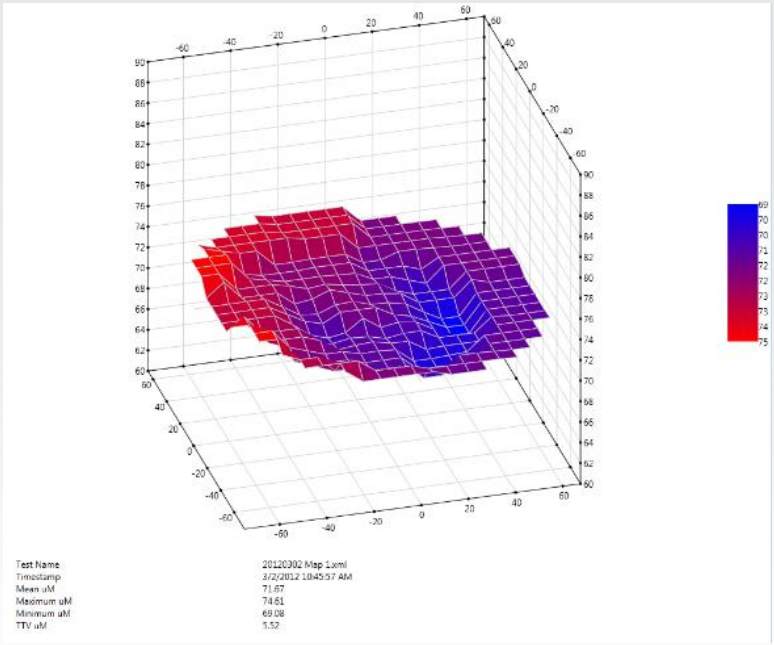
SSEC Integrated Sensor Graphics

ISIS SemDex Graphics

Integrated Wafer Thickness Measurement - mapping options



Ring map



Surface map

Summary

- Process demonstrated to etch silicon and safely reveal Cu TSV
- Clean silicon surface and isolated Cu TSVs
- Integrated Wafer Thickness Measurement for process control

"Success is when Customers are Delighted."

SSEC

Solid State Equipment LLC

Single Wafer Wet Processing