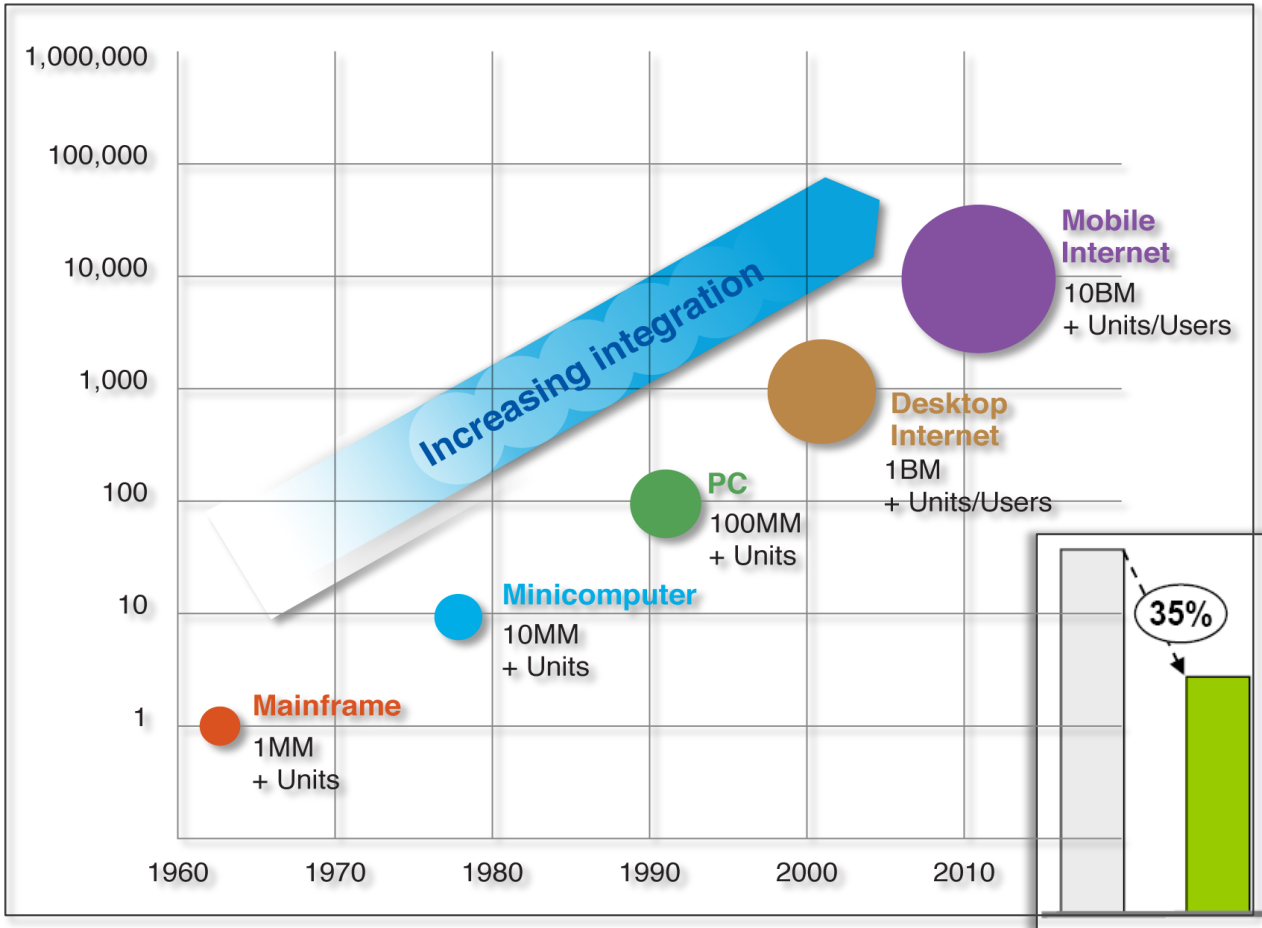
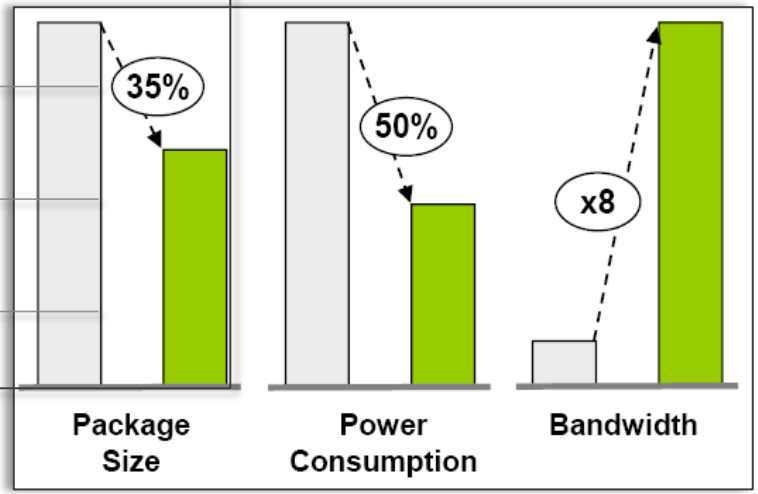
3D Packaging Solution Providing DDR & LPDDR Co-Support for Ultrabook™ and Next Generation Servers

Simon McElrea

The Governing Laws



Dr. Morris Chang: "Mo's Law"



Samsung: "More that Moore's Law"

invensas

In Each Quadrant, Solutions Are Needed

REMOTE

LOCAL

DATACENTER

CLOUD

APPS

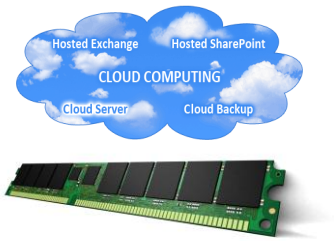
MOBILE TERMINALS

PLUGGED IN

BATTERY

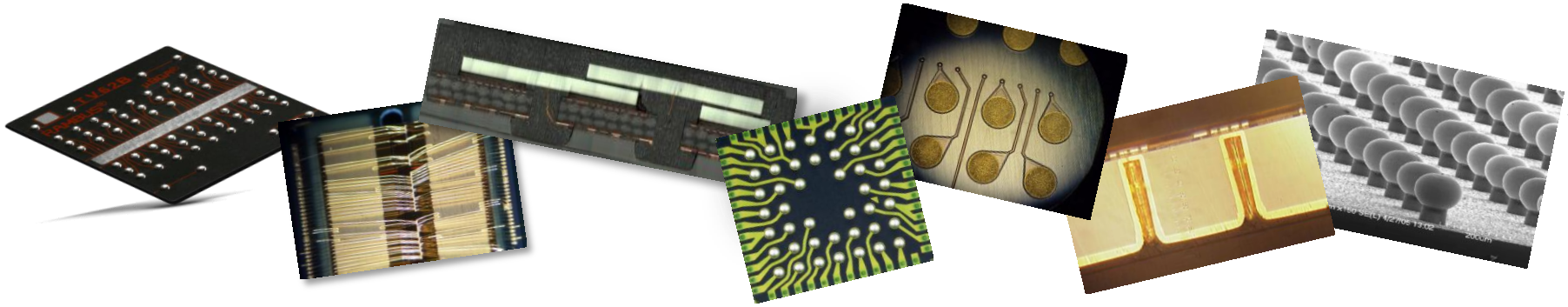
invensas

2D-3D Evolution: Bridge Solutions Needed



CLOUD/STORAGE: CAPACITY + PERFORMANCE
- Enabling Technologies for Memory Integration
- Scalable Performance with Reduced Power & Cost

Advanced Interconnect
IC Circuitry
3D/Interposer
Module/Memory
…



MOBILE/TERMINAL: BANDWIDTH + BATTERY LIFE
- Enabling Technologies for Mobile Integration
- Scalable Performance with Reduced Power & Cost

Advanced Interconnect
IC Circuitry
3D/Interposer
Module/Memory
…

invensas™

Example: The Ultrabook™ Challenge

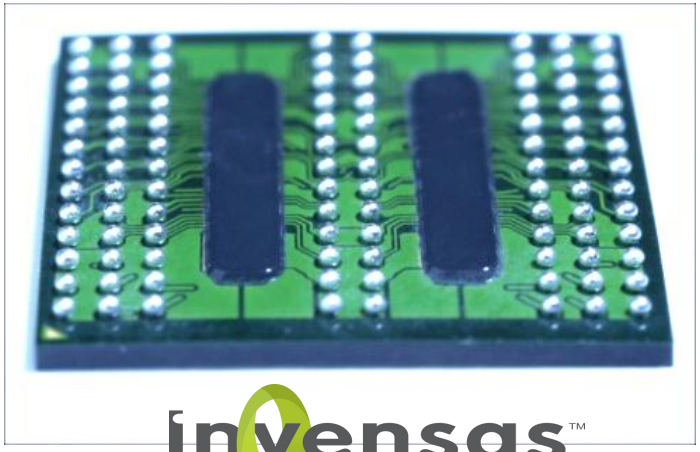
HOW TO TURN THIS …

INTO THIS …

USING THE SAME SILICON

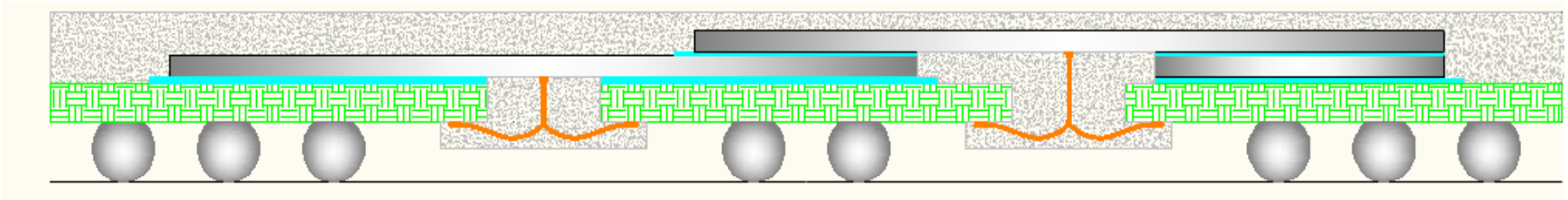
invensas™

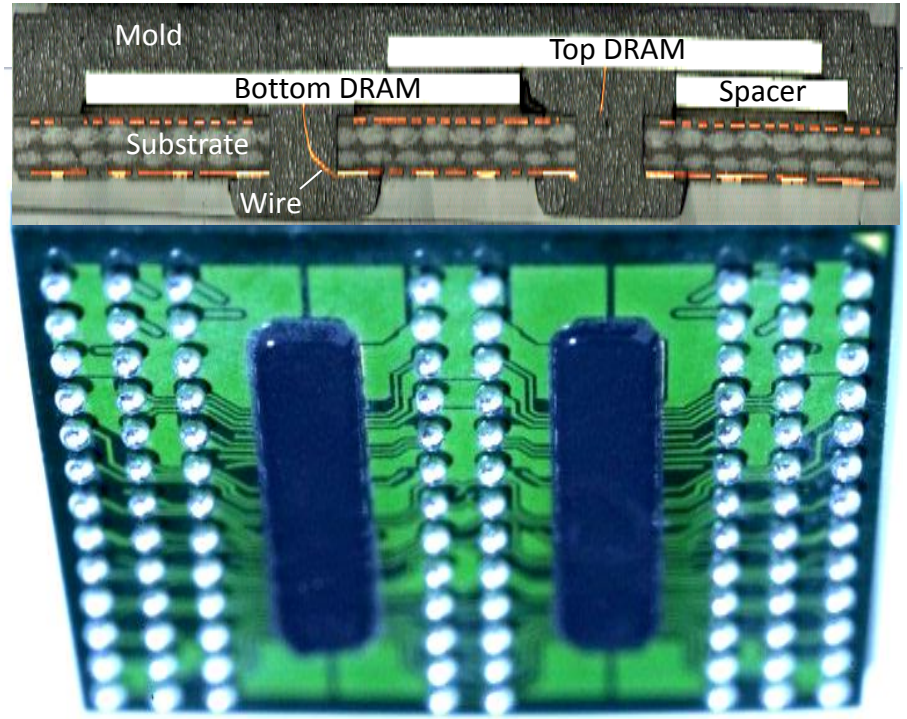
A Brief Introduction to Multi-Die Face-Down (xFD™) Technology

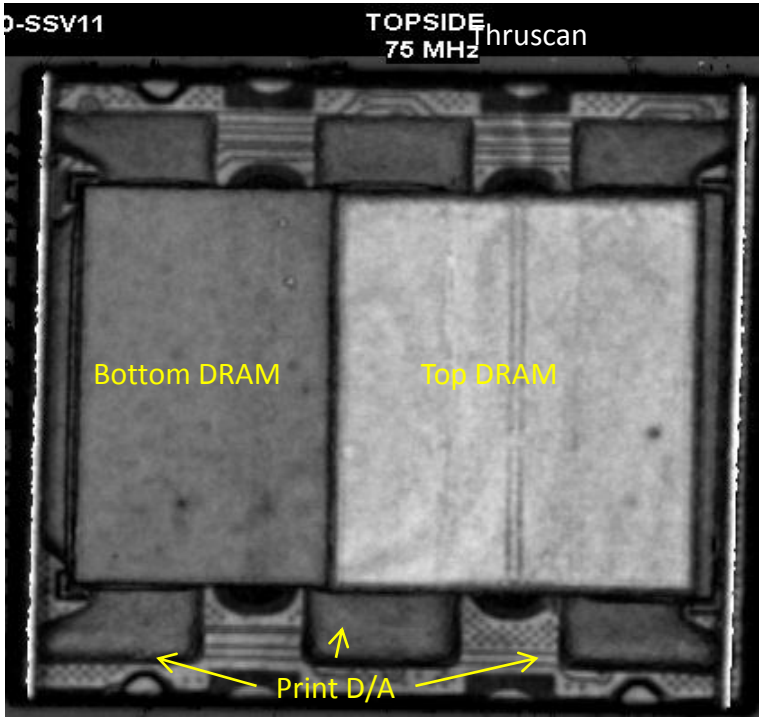


Dual-Face-Down (DFD™) Package

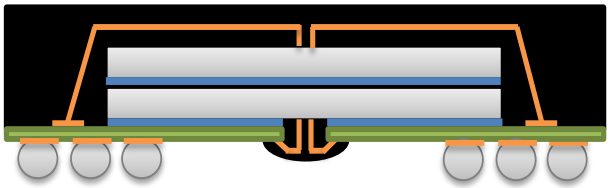
CROSS-SECTION



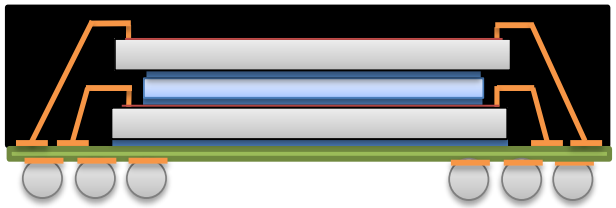




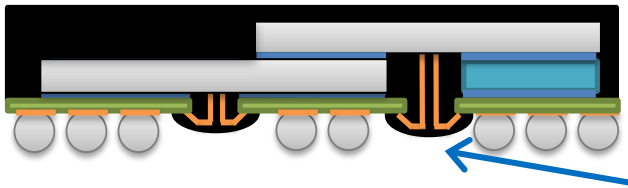
Thinner & Cheaper than Competing DDP



Opposing-Face DDP



Face-Up DDP (RDL)



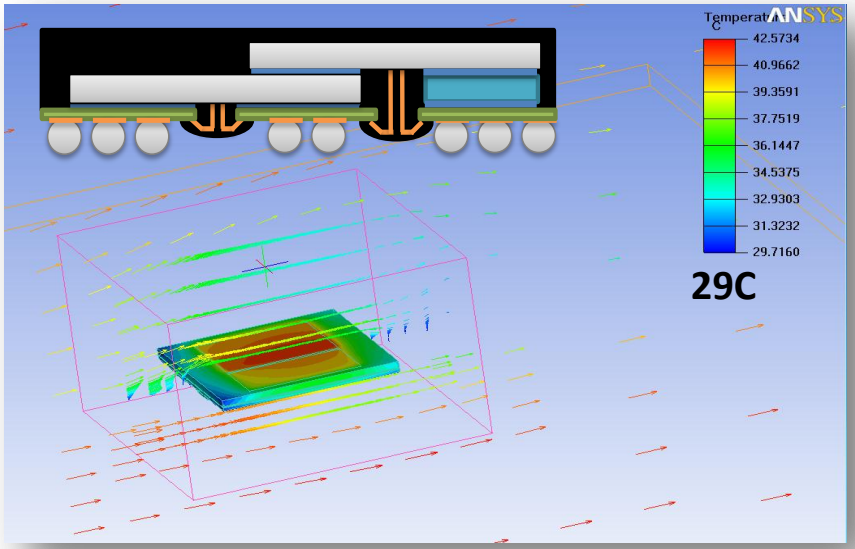
Dual Face Down (DFD)

~10X less Gold

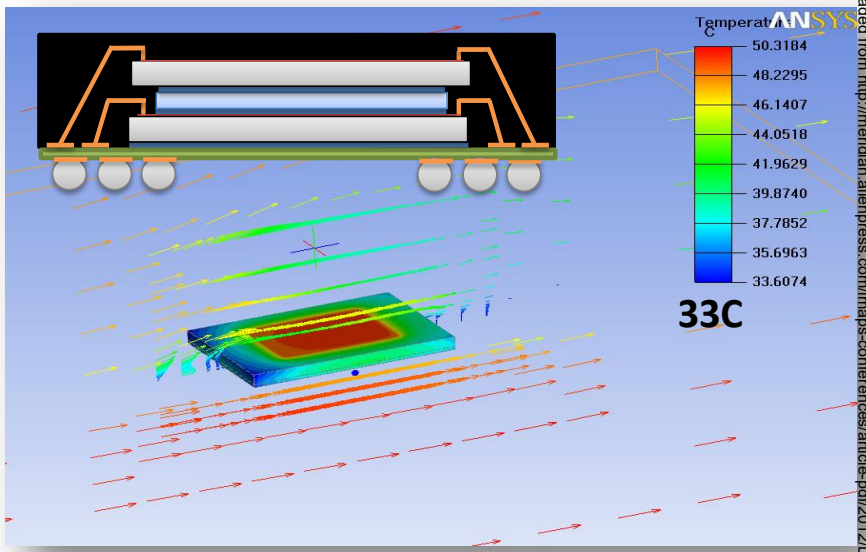
invensas

Thermal Advantage Due to Thinness & Offset Die

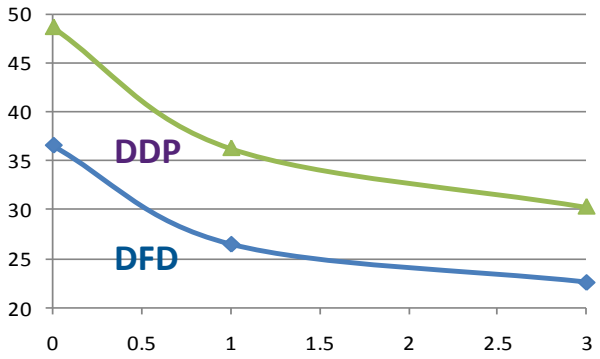
INVENSAS DFD **42C**



CONVENTIONAL DDP **51C**



θ_{ja} vs. Air Flow

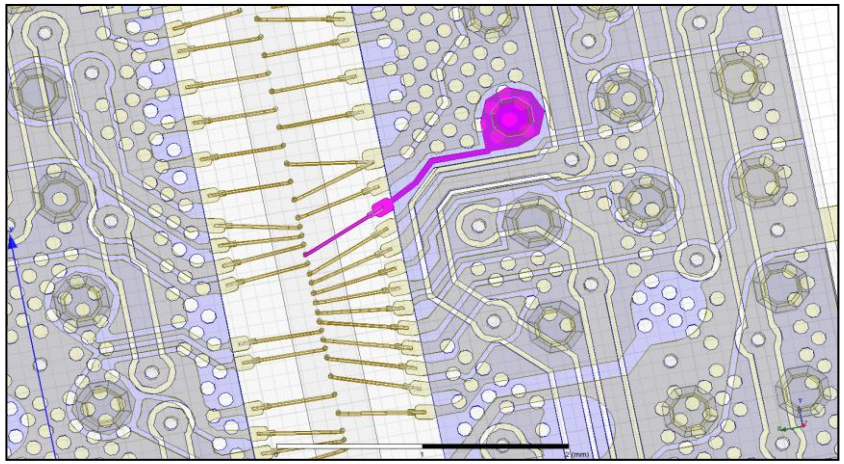


Configuration	DFD (°C/W)	DDP (°C/W)	Delta from DDP
θ_{ja} still air	36.6	48.7	-25%
θ_{ja} @ 1m/s	26.5	36.3	-27%
θ_{ja} @ 3m/s	22.6	30.3	-25%

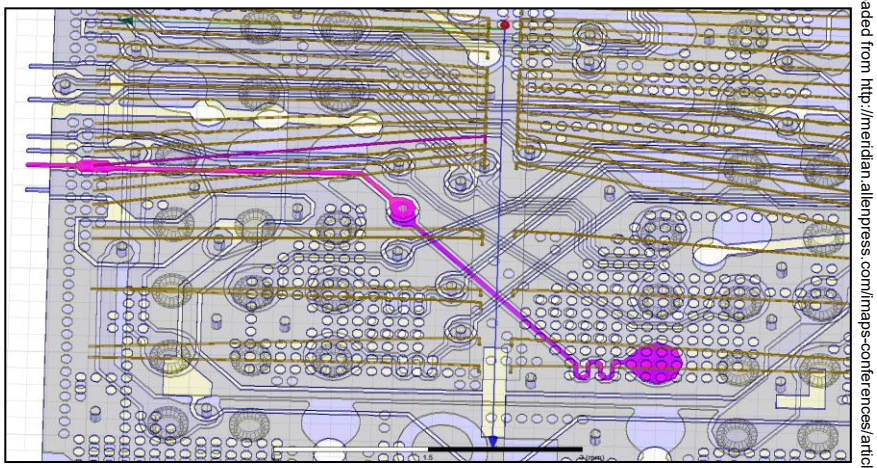
25% LOWER θ_{ja} FOR INVENSAS DFD VS. CONVENTIONAL DDP PACKAGE

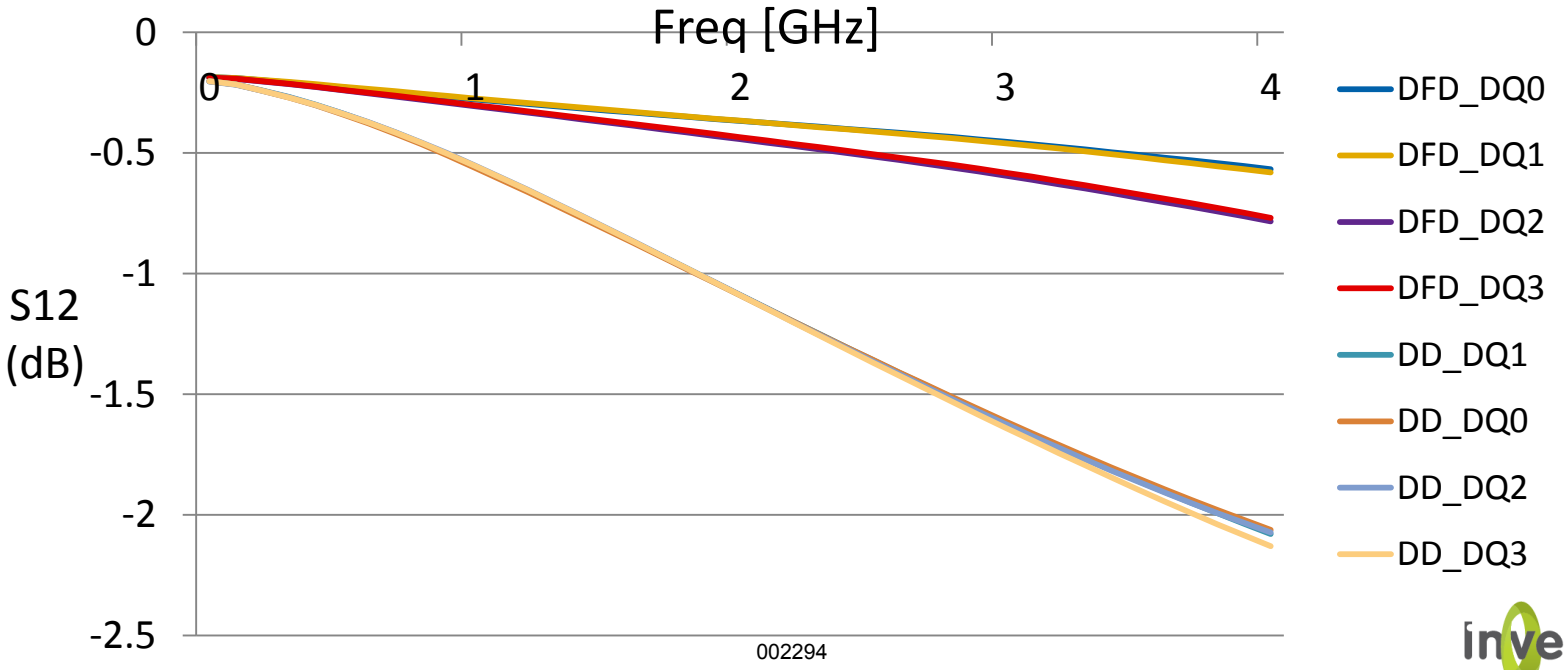
Speed Advantage: DQ Sig. Integrity vs. Opposing Face DDP

DQ: DUAL FACE DOWN



DQ: DDP CONTROL





Data Eye Shmoo Plots at 2133 MT/s & 95°C

Symmetric die performance

Bottom Die

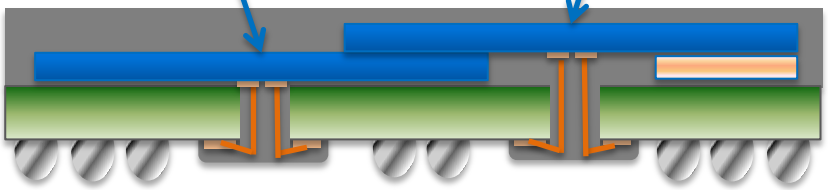
Top Die

DQ

DQS/DQS#

From 15 randomly selected characterization units.

Measured at 95°C on production ATE (Advantest 5501).

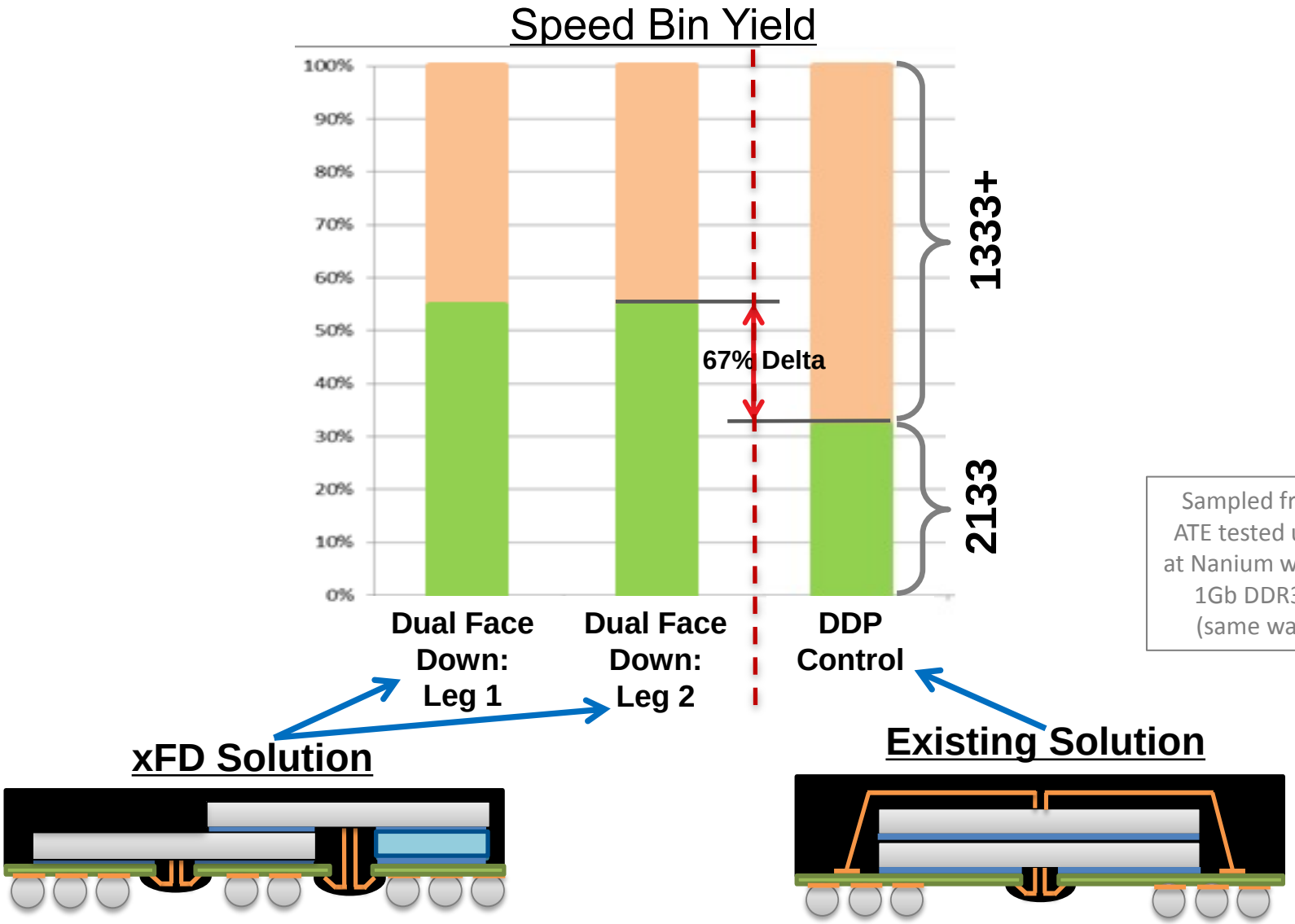


Leg A CS0 – Bottom die 2133MT/s (15 unit sample size)

Leg A CS1 – Top die 2133MT/s (15 unit sample size)

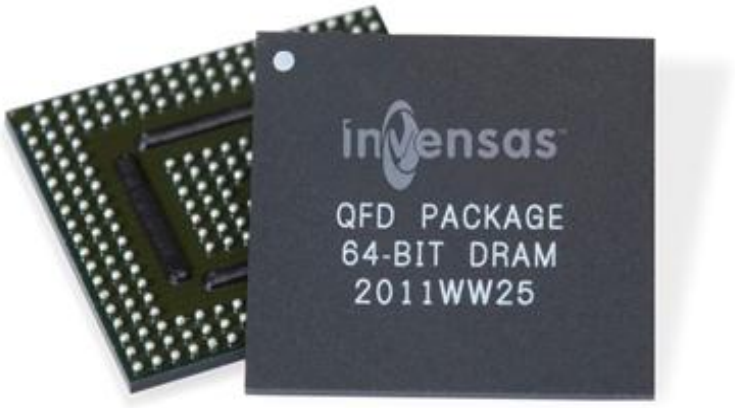
002295

Performance & Cost Advantage: Speed Bin Yield



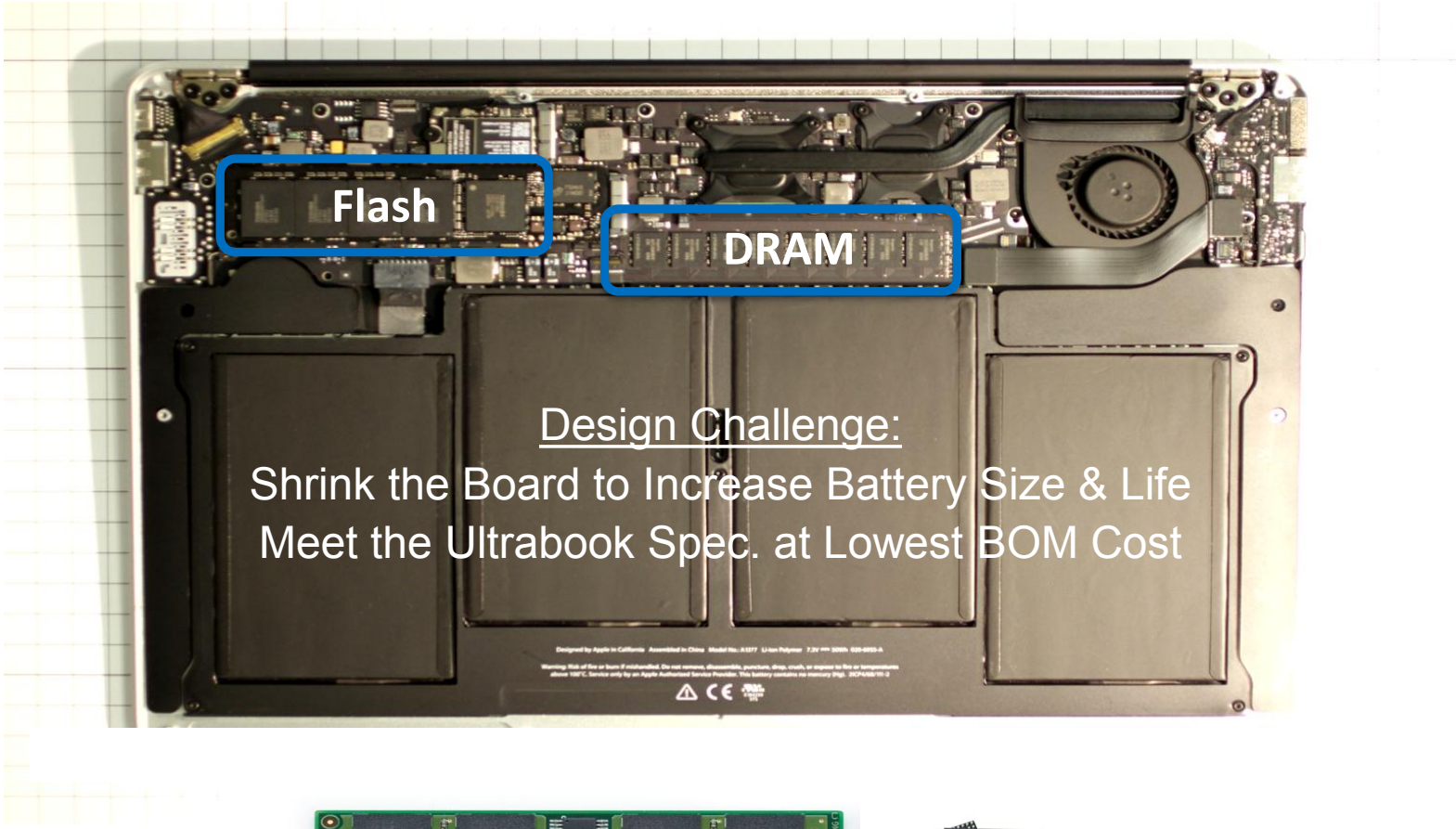
Sampled from 1000 ATE tested units built at Nanium with Micron 1Gb DDR3 Silicon (same wafer lot).

The xFD™ Solution for Ultrabook™



invensas™

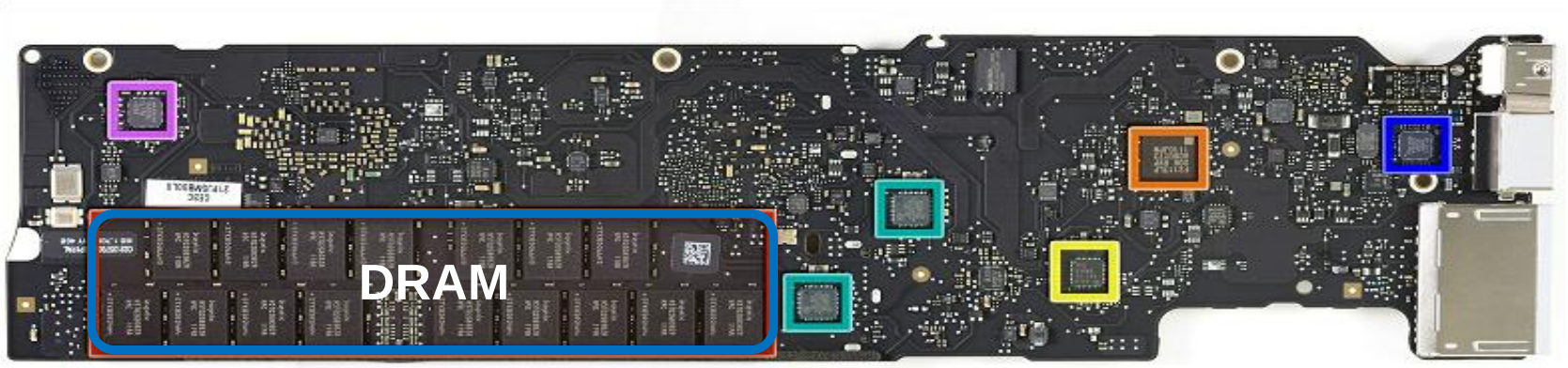
The Ultrabook™ Design Challenge



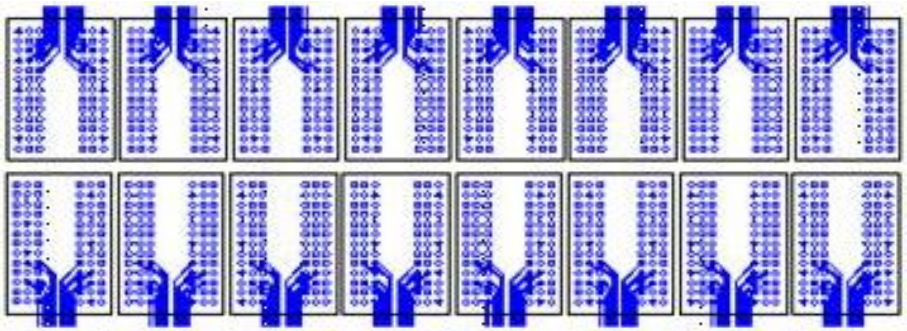
SO-DIMM MODULES DON'T FIT

NEED "DIMM IN A PACKAGE" SOLUTION

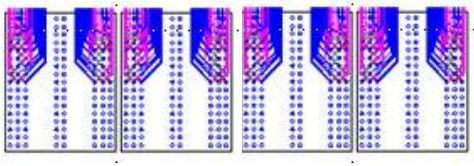
Multi-Die Ultrabook™ Packaging: Real Example



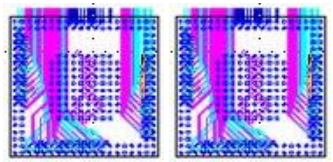
Current PCB Footprint



Dual Face Down (DFD)



Quad Face Down (QFD)

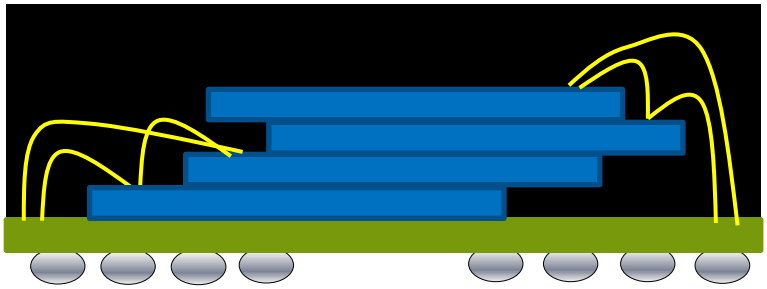


invensas™

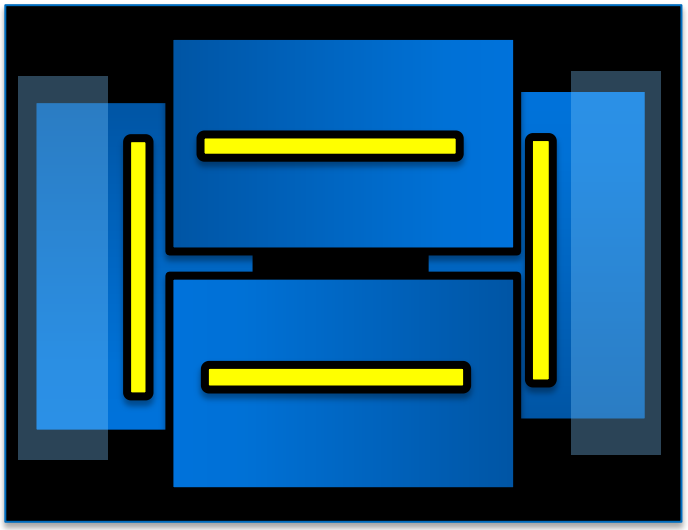
Quad Die Competitive Comparison

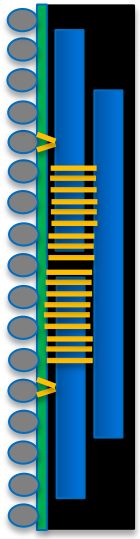
Spacer-RDL QDP

Stairstep-RDL QDP



Invensas QFD

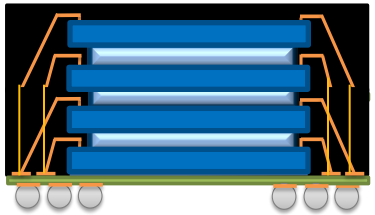




002300

Quad Die Process Comparison

Existing



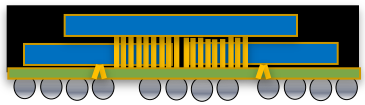
Wafer Level RDL Process

1. Dielectric
2. Mask , Etch
3. Metal Deposition
4. Mask , Etch Metal
5. Dielectric
6. Mask , Etch
7. NiAu plating

1. RDL wafer**
2. Print 1st adhesive
3. Place 1st die
4. Wirebond 1st die
5. Dispense adhesive
6. Place spacer die
7. Dispense adhesive
8. Place 2nd die
9. Wirebond 2nd die
10. Dispense adhesive
11. Place spacer die
12. Dispense adhesive
13. Place 3rd die
14. Wirebond 3rd die
15. Dispense adhesive
16. Place spacer die
17. Dispense adhesive
18. Place 4th die
19. Wirebond 4th die
20. Mold
21. Ball attach
22. Singulate

29 STEPS

QFD

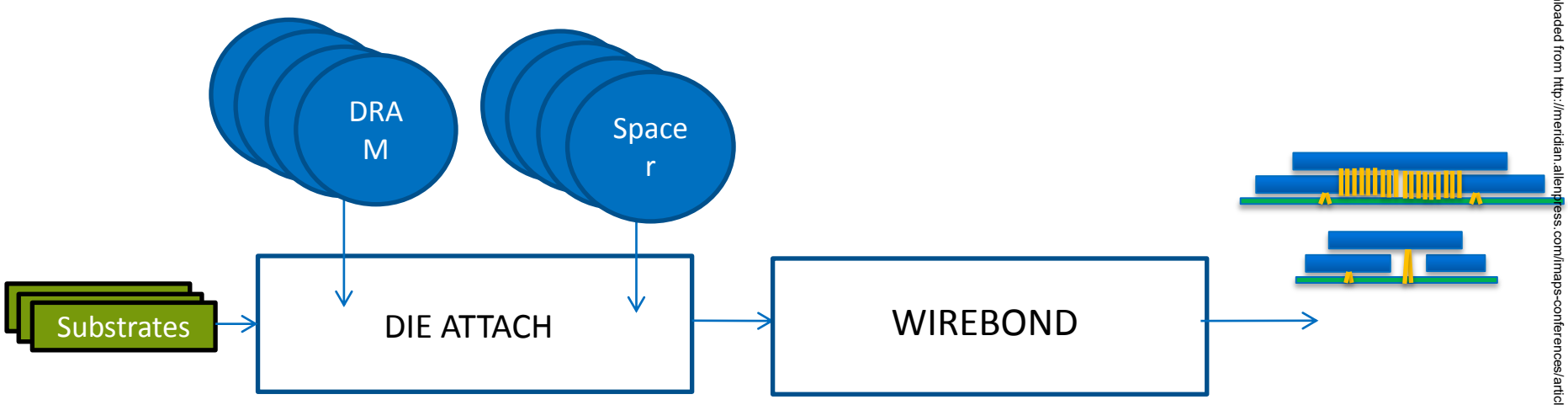


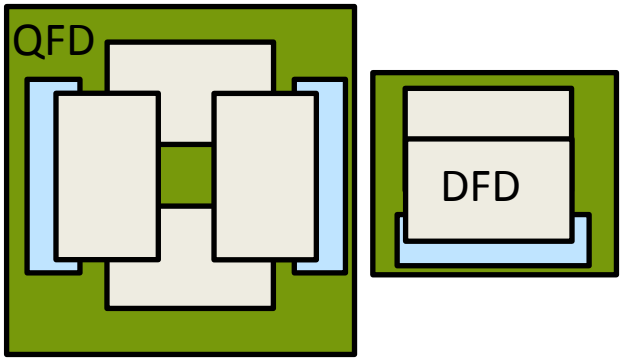
1. Print 1st adhesive
2. Place 1st layer die
3. Dispense adhesive
4. Place 2nd layer die
5. 1-pass wirebond
6. Mold
7. Ball attach
8. Singulate

8 STEPS

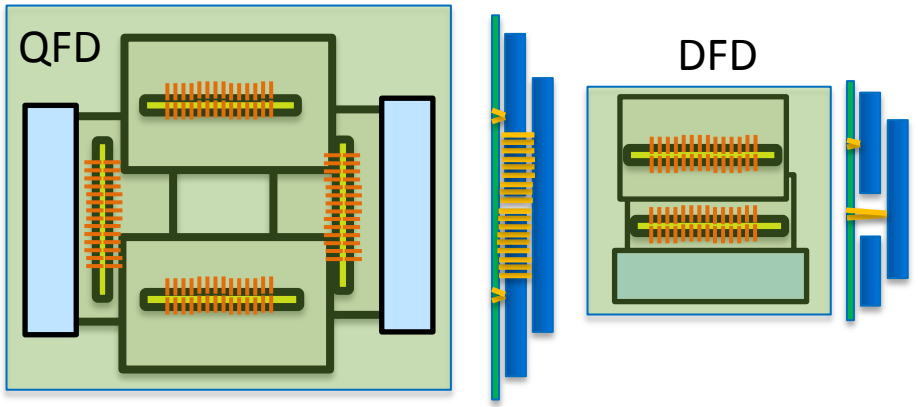
invensas

Assembly Process Flow: QFD or DFD





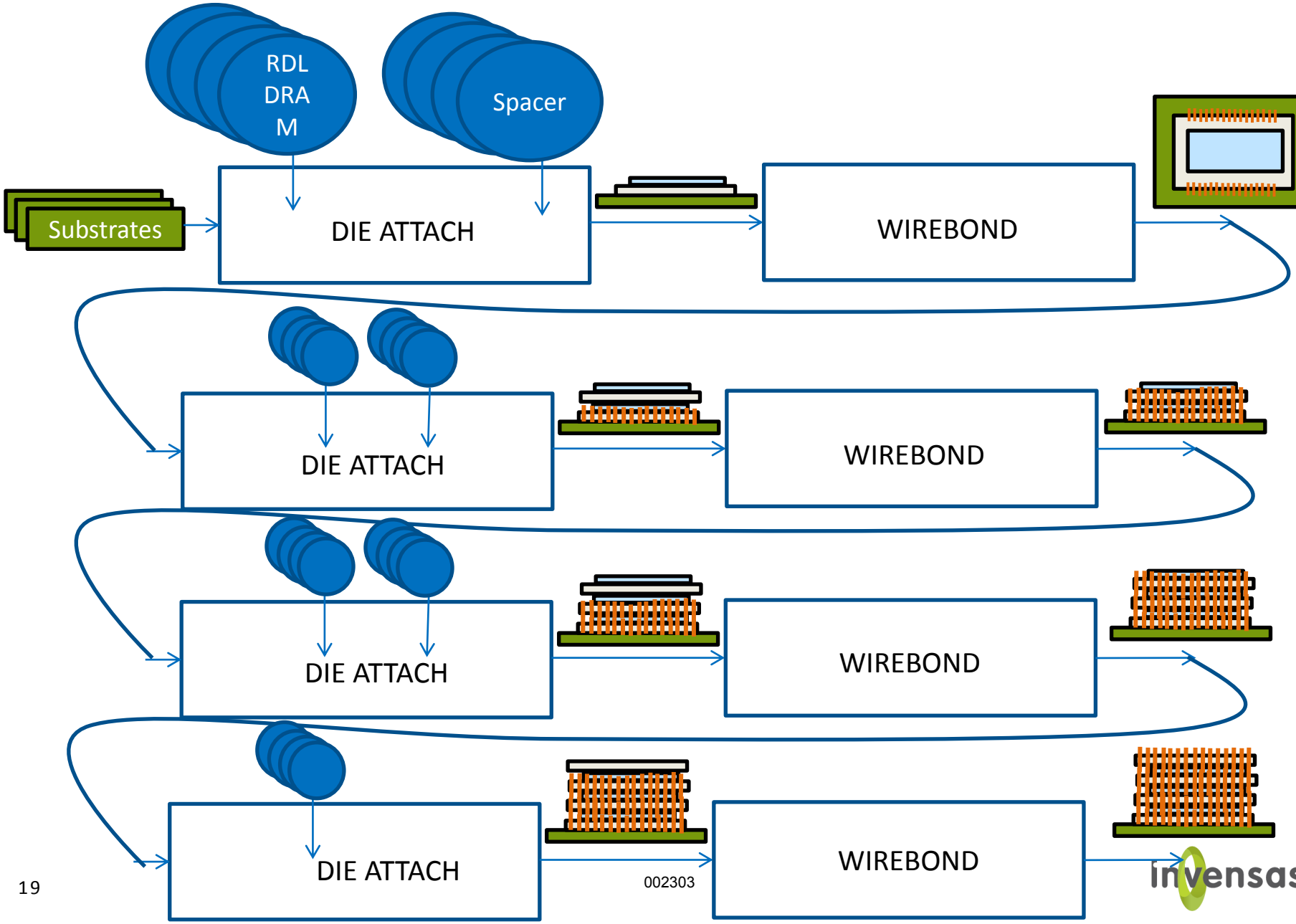
All die + spacers placed
on substrate in one machine pass.



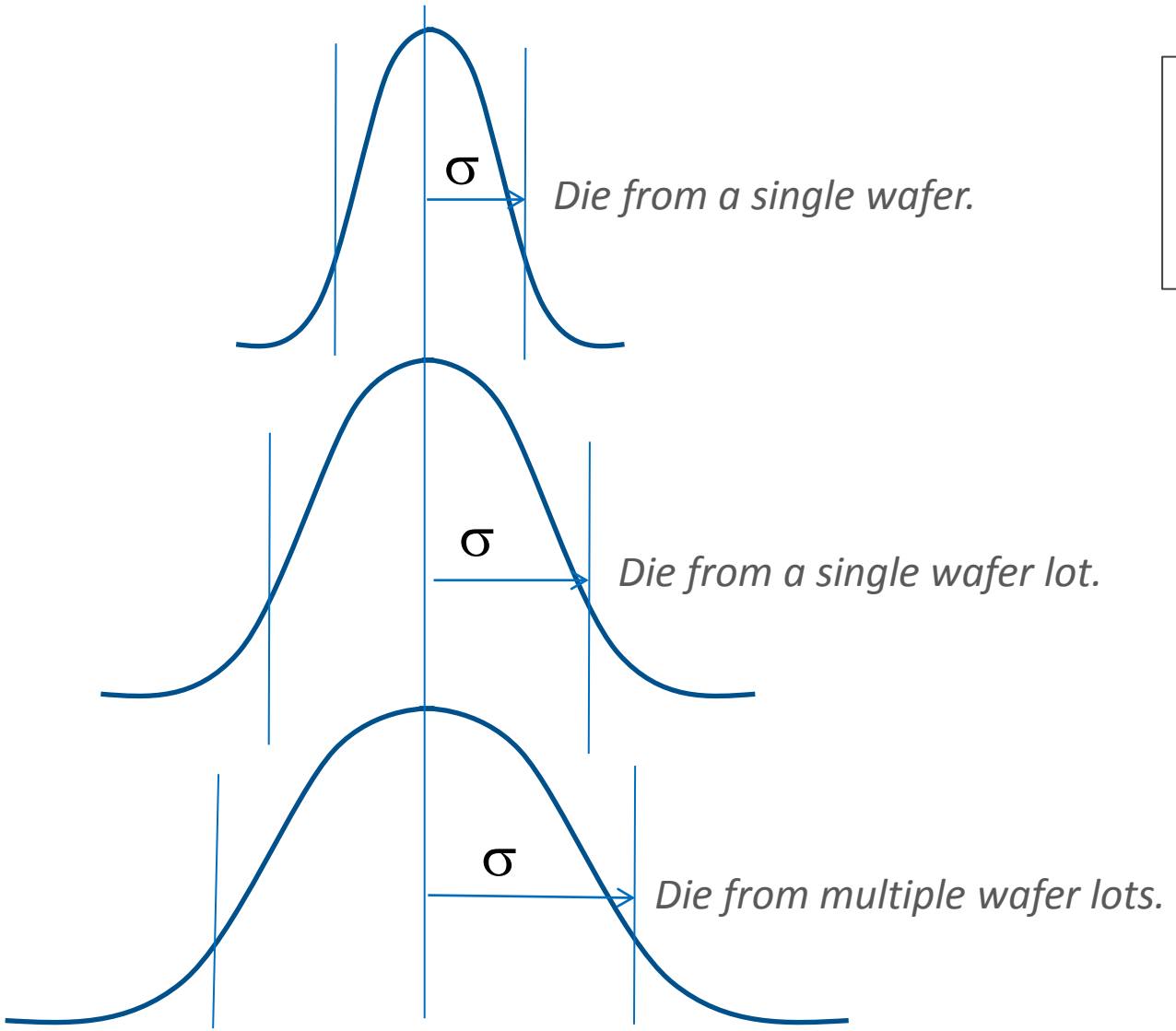
All die wire-bonded in a single pass.

invensas

Assembly Process Flow: Current Stacked Package (QDP)



Wafer/Die Pick vs. Speed Bin Statistics

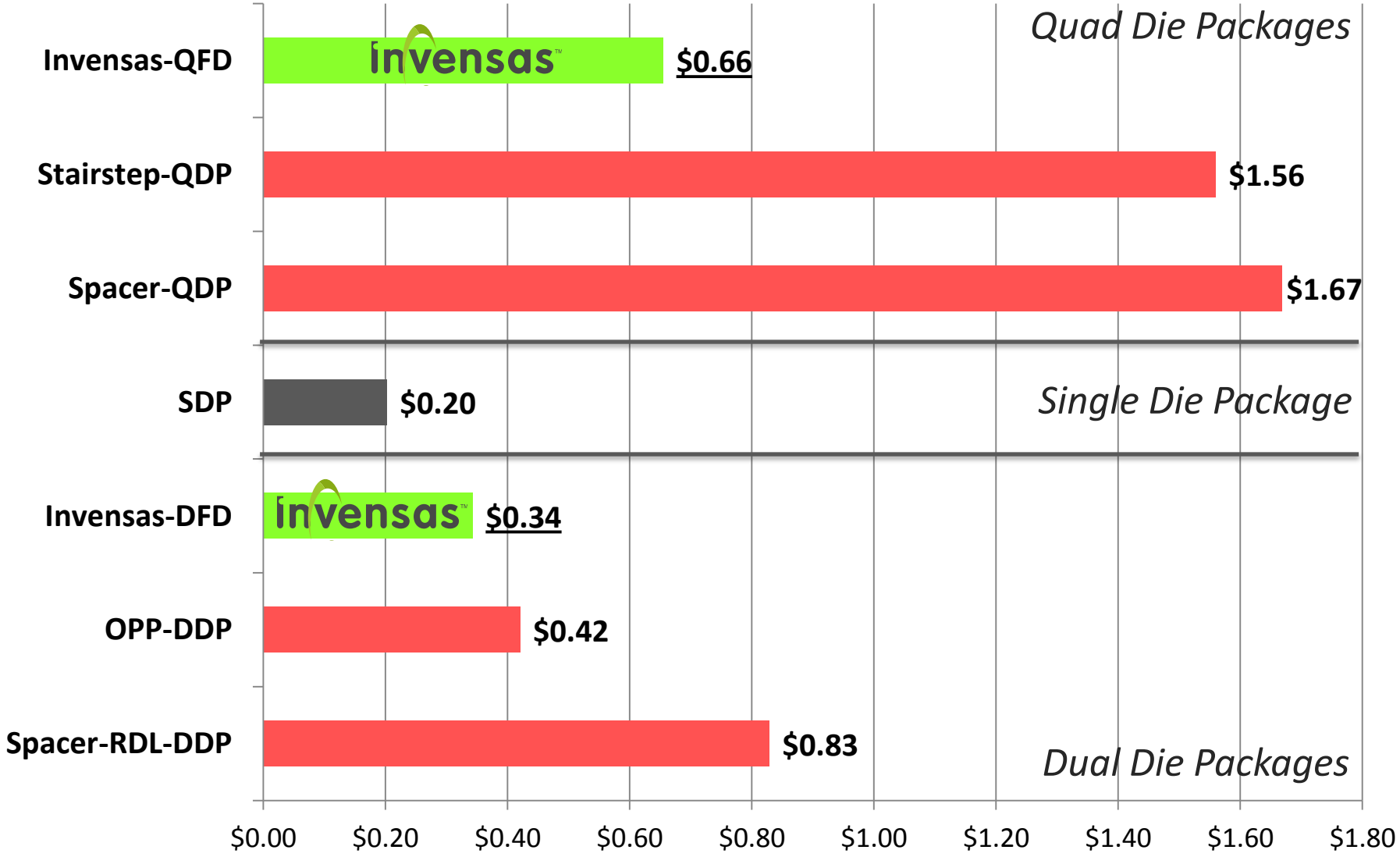


Die from a single wafer show tighter speed distribution vs. multiple wafers/wafer lots.

xFD PICKS ALL DIE SEQUENTIALLY FROM SAME WAFER

invensas

Packaging Cost Comparison



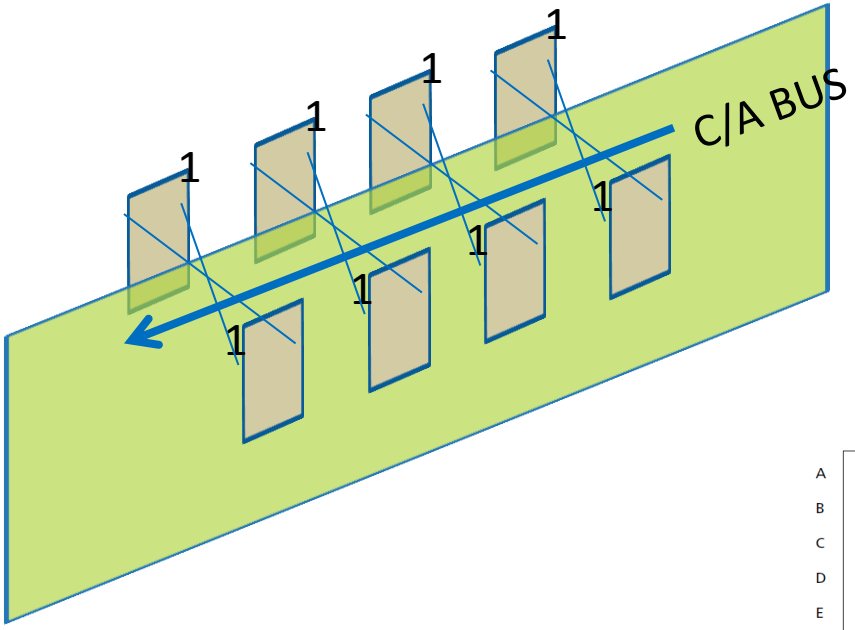
002305

Data based on Invensas and 3rd Party HVM full line cost models.

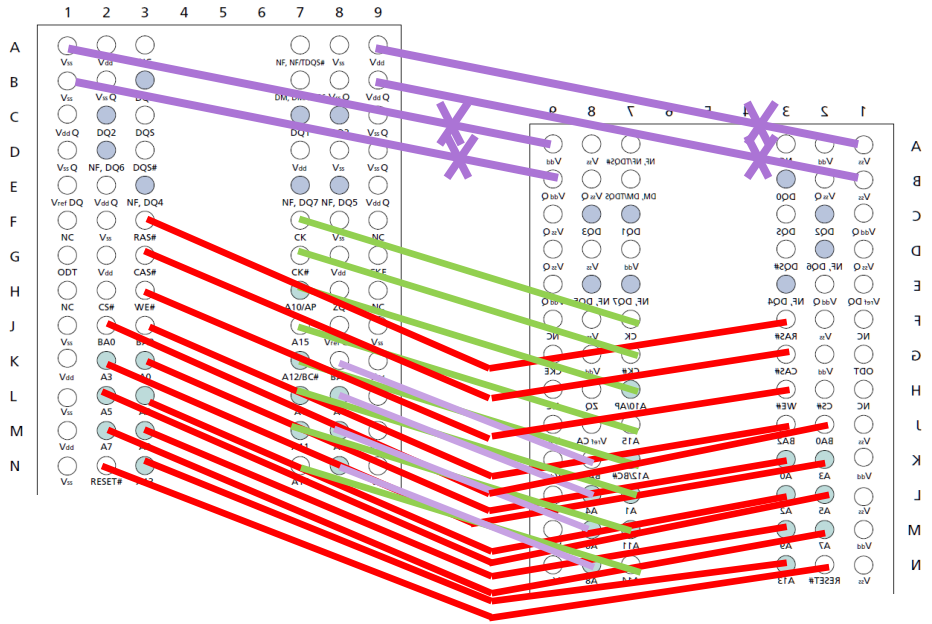
Other Issues with the Current DRAM Ball-Out

- Current 78 Ball DRAM is difficult to use for solder-down memory in Ultrabook:
  - PCB layout is complex and congested
  - Breakout regions cannot share signals top/bottom
  - Lengthy stubs in breakout
- New design goal for ball-out and routing:
  - Axisymmetric ball-out: ideal for clamshell layout
  - Shared signals
  - Short stubs in breakout region
- Additional design goal to avoid HDI PCB technology requirement:
  - Goal: std. PTH vs. HDI build-up board technology

Double Sided Mother Board Assembly Challenges



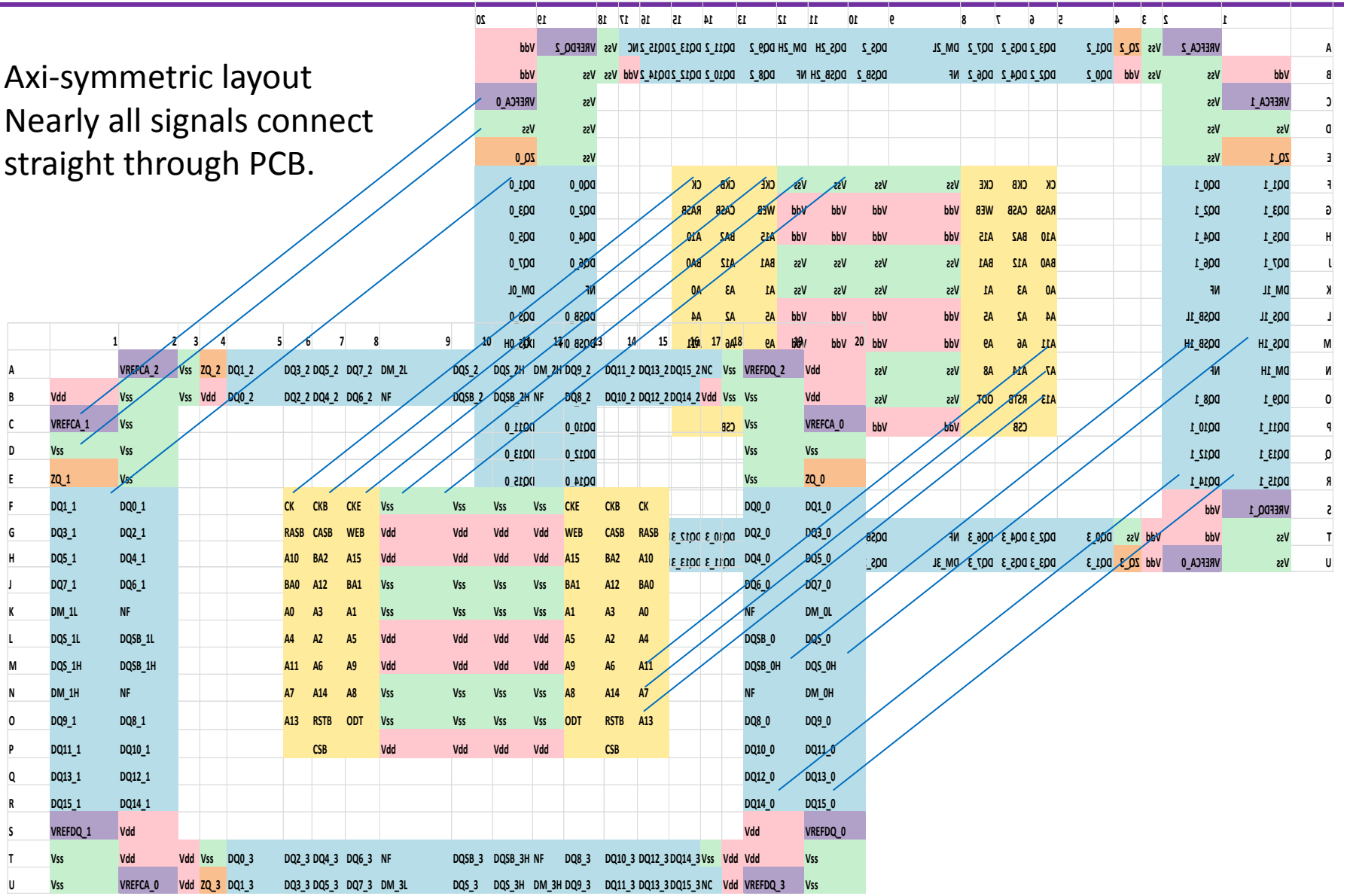
Must interconnect same bussed signals to corresponding leads using “shoelace pattern” (criss-cross routing through the mother board).



Complex unbalanced routing many Vdd/Vss shorts.

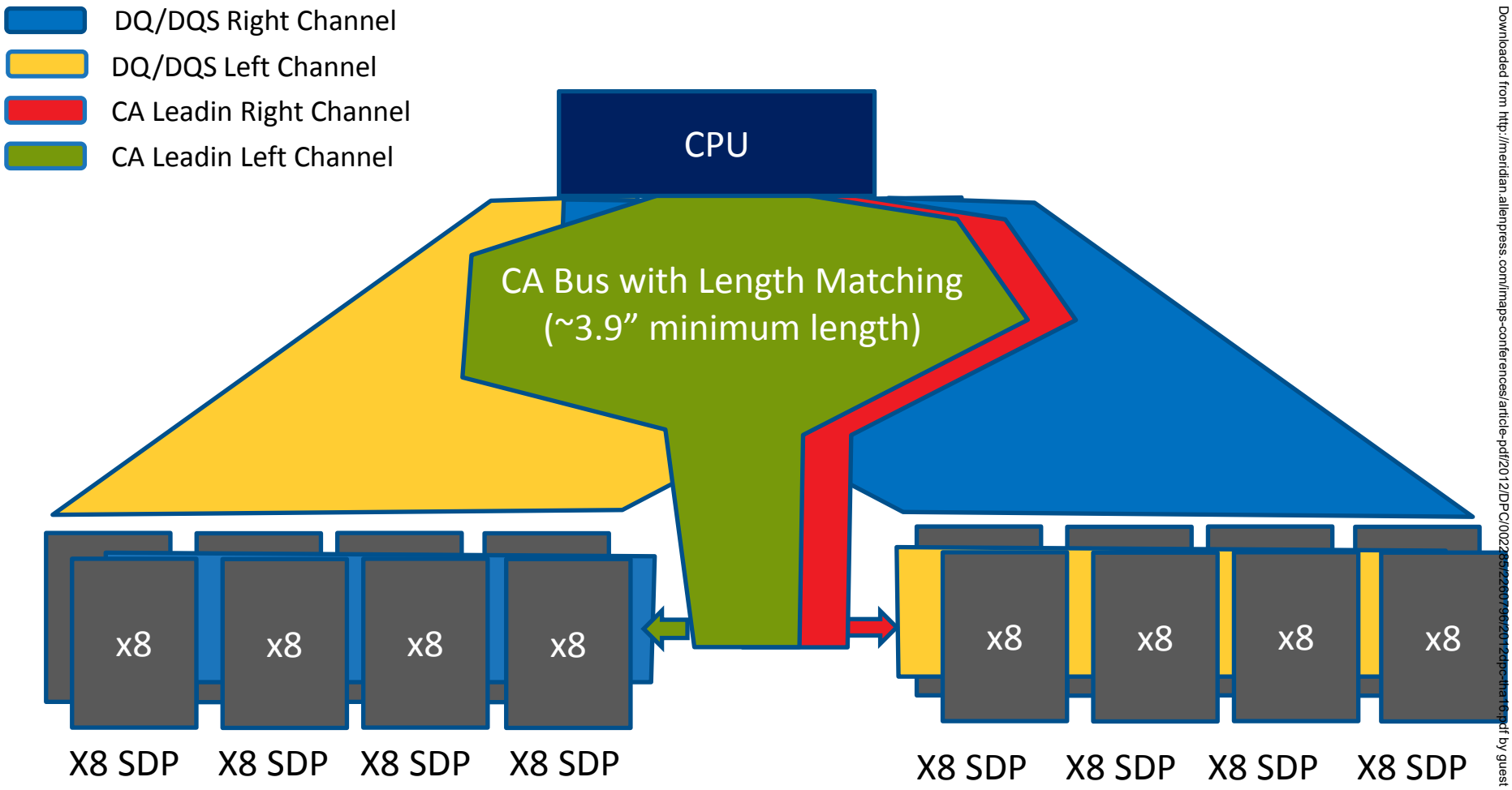
Solution: Axisymmetric Ball-Out with QFD

Axi-symmetric layout
Nearly all signals connect straight through PCB.



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A		VREFCA_2	Vss	ZQ_2	DQ1_2	DQ3_2	DQ5_2	DQ7_2	DM_2L	DQS_2	DQS_2H	DM_2H	DQ9_2	DQ11_2	DQ13_2	DQ15_2	NC	Vss	VREFDQ_2	Vdd
B	Vdd	Vss	Vss	Vdd	DQ0_2	DQ2_2	DQ4_2	DQ6_2	NF	DQSB_2	DQSB_2H	NF	DQ8_2	DQ10_2	DQ12_2	DQ14_2	Vdd	Vss	Vss	Vdd
C	VREFCA_1	Vss															CS#		Vss	VREFCA_0
D	Vss	Vss																	Vss	Vss
E	ZQ_1	Vss																	Vss	ZQ_0
F	DQ1_1	DQ0_1			CK	CKB	CKE	Vss	Vss	Vss	Vss	CKE	CKB	CK					DQ0_0	DQ1_0
G	DQ3_1	DQ2_1			RAS#	CAS#	WE#	Vdd	Vdd	Vdd	Vdd	WE#	CAS#	RAS#					DQ2_0	DQ3_0
H	DQ5_1	DQ4_1			A10	BA2	A15	Vdd	Vdd	Vdd	Vdd	A15	BA2	A10					DQ4_0	DQ5_0
J	DQ7_1	DQ6_1			BA0	A12	BA1	Vss	Vss	Vss	Vss	BA1	A12	BA0					DQ6_0	DQ7_0
K	DM_1L	NF			A0	A3	A1	Vss	Vss	Vss	Vss	A1	A3	A0					NF	DM_0L
L	DQS_1L	DQSB_1L			A4	A2	A5	Vdd	Vdd	Vdd	Vdd	A5	A2	A4					DQSB_0	DQS_0
M	DQS_1H	DQSB_1H			A11	A6	A9	Vdd	Vdd	Vdd	Vdd	A9	A6	A11					DQSB_0H	DQS_0H
N	DM_1H	NF			A7	A14	A8	Vss	Vss	Vss	Vss	A8	A14	A7					NF	DM_0H
O	DQ9_1	DQ8_1			A13	RST#	ODT	Vss	Vss	Vss	Vss	ODT	RST#	A13					DQ8_0	DQ9_0
P	DQ11_1	DQ10_1				CS#		Vdd	Vdd	Vdd	Vdd		CS#						DQ10_0	DQ11_0
Q	DQ13_1	DQ12_1																	DQ12_0	DQ13_0
R	DQ15_1	DQ14_1																	DQ14_0	DQ15_0
S	VREFDQ_1	Vdd																	Vdd	VREFDQ_0
T	Vss	Vdd	Vdd	Vss	DQ0_3	DQ2_3	DQ4_3	DQ6_3	NF	DQSB_3	DQSB_3H	NF	DQ8_3	DQ10_3	DQ12_3	DQ14_3	Vss	Vdd	Vdd	Vss
U	Vss	VREFCA_0	Vdd	ZQ_3	DQ1_3	DQ3_3	DQ5_3	DQ7_3	DM_3L	DQS_3	DQS_3H	DM_3H	DQ9_3	DQ11_3	DQ13_3	DQ15_3	NC	Vdd	VREFDQ_3	Vss

Current Memory Layout Scheme (3-6-3 HDI)



DRAMs are placed directly opposite the PCB from each other (shown offset for clarity).

002309

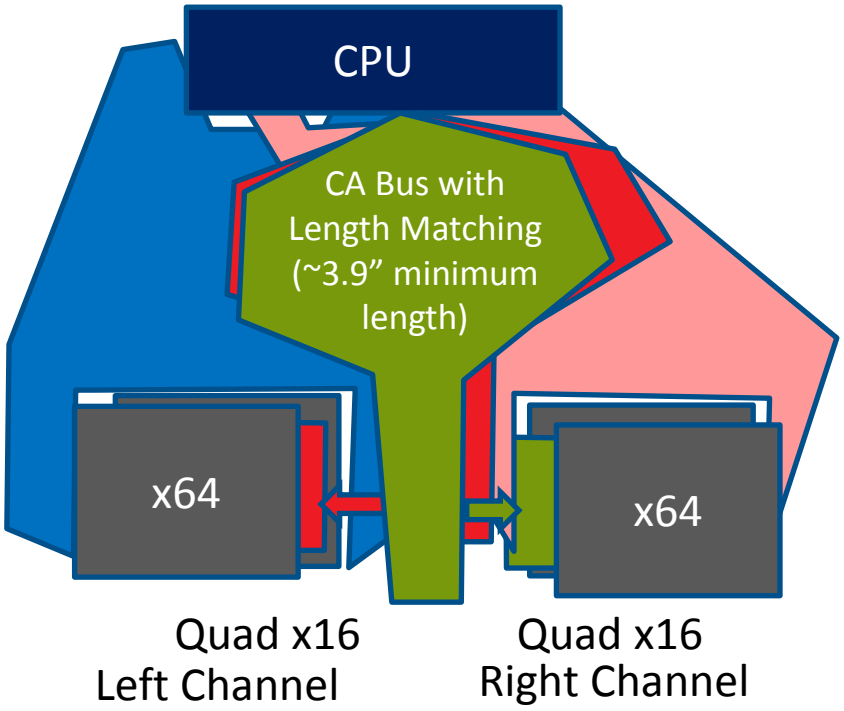
Invensas QFD: Dual Channel Dual Rank (non HDI PCB)

DQ/DQS Channel 0

DQ/DQS Channel 1

CA Channel 0

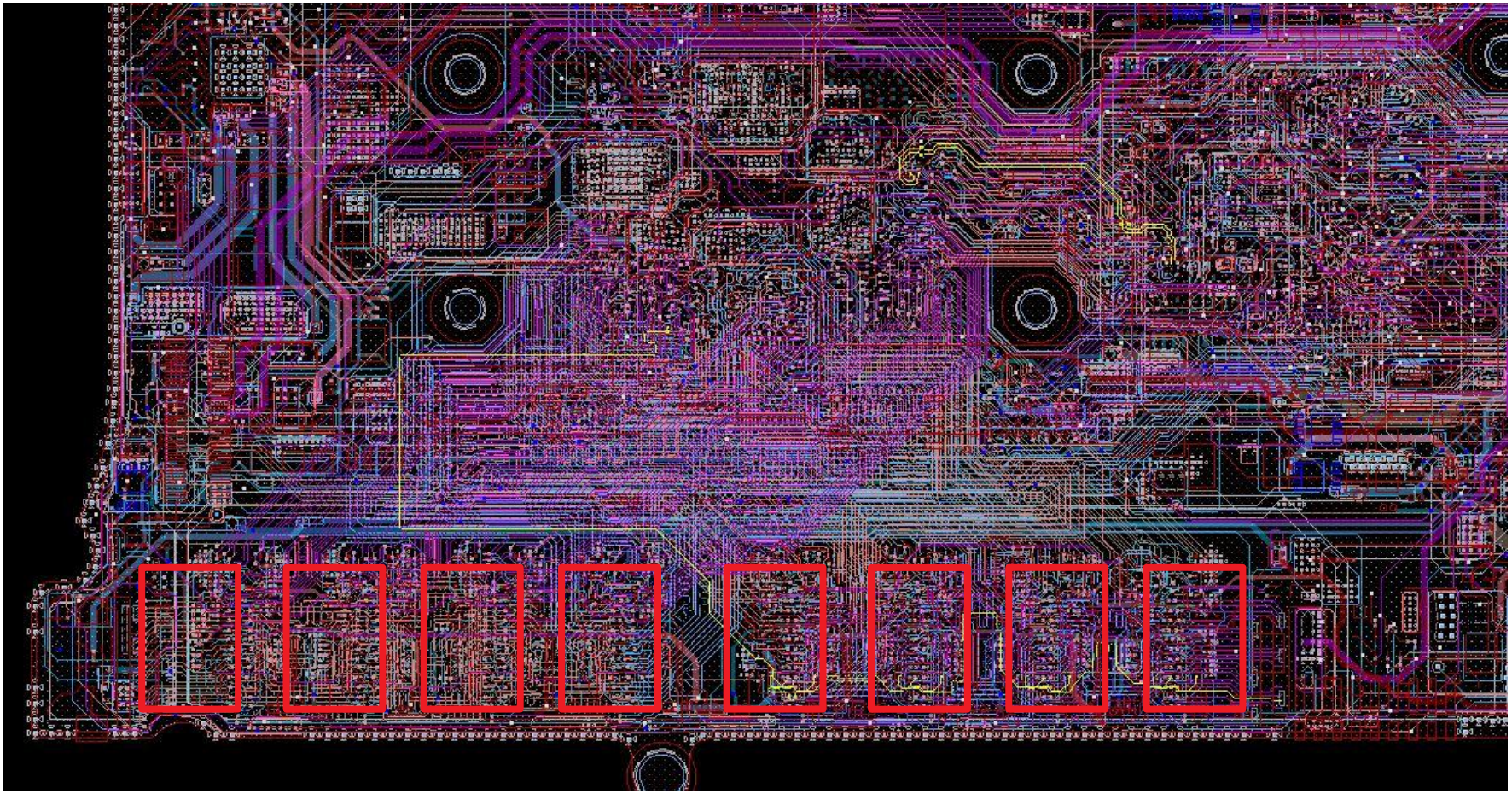
CA Channel 1



DRAMs are placed directly opposite the PCB from each other (shown offset for clarity).

002310

Original Design: SDP DDR3 (3-6-3 HDI Board Required)



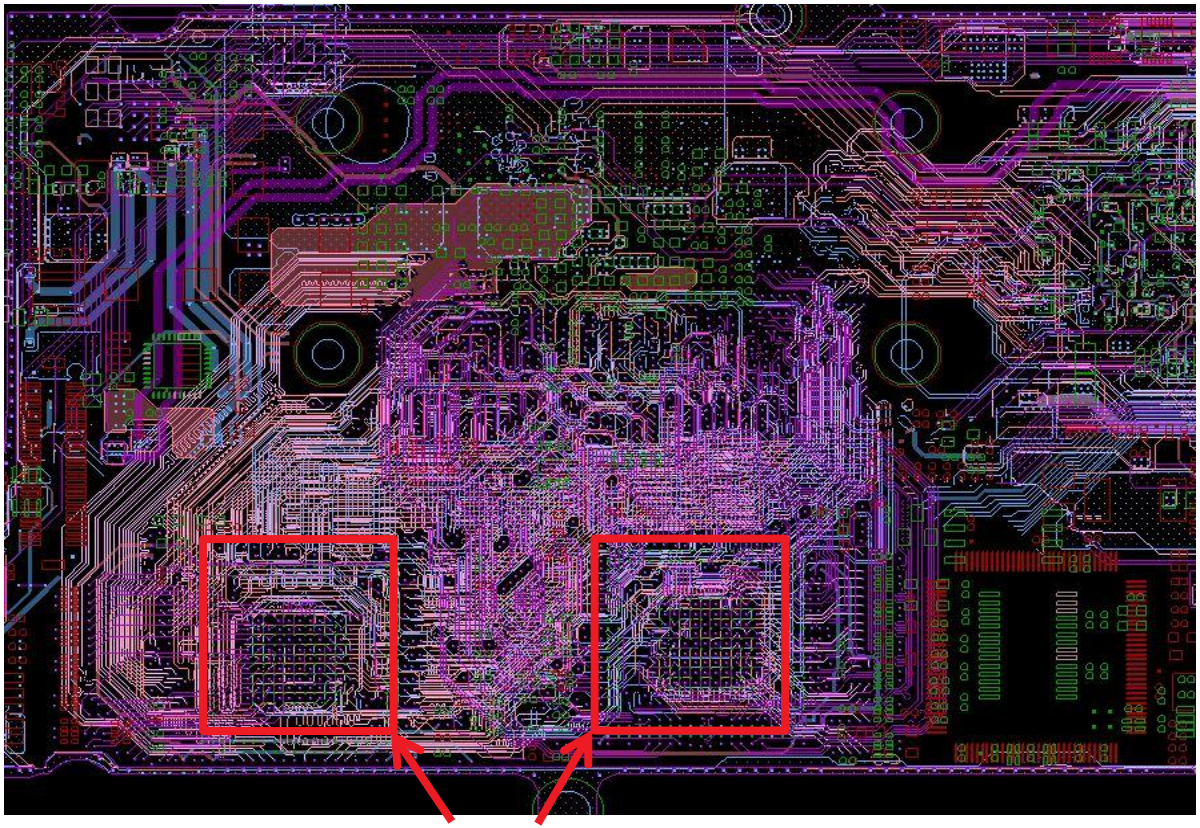
Single Die DRAM Packages: 8 bit organization, Top and Bottom Placement on PCB

Left Channel

Right Channel

002311

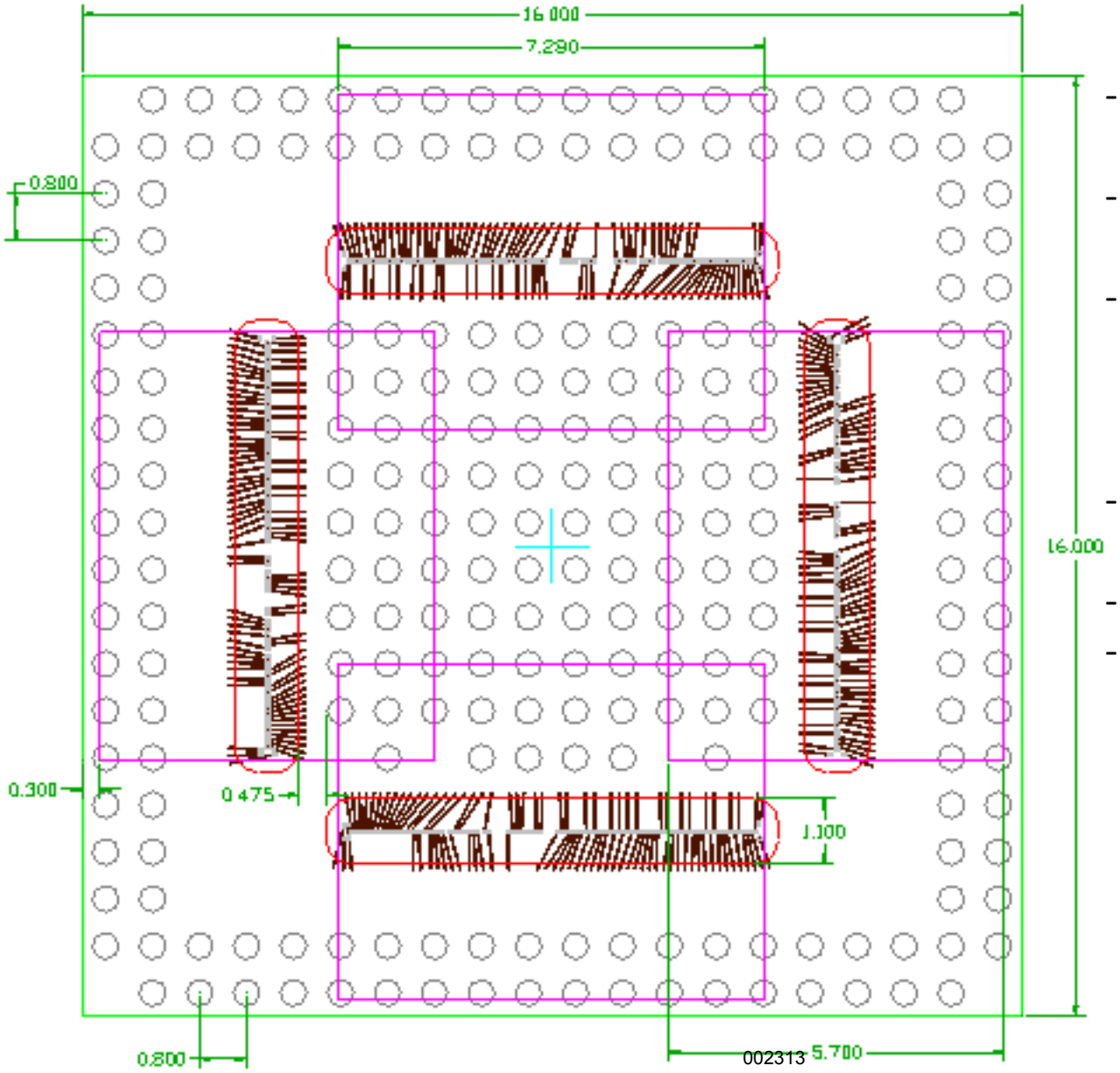
Modified xFD Design: x64 QFD (Std. PCB Required)



17 x 17 QFD MEMORY

Significant Form-Factor Reduction, Plus Conversion from 3-6-3 HDI to Std. PTH saves ~$15 Board Cost.

Ultrabook™ QFD Package Example

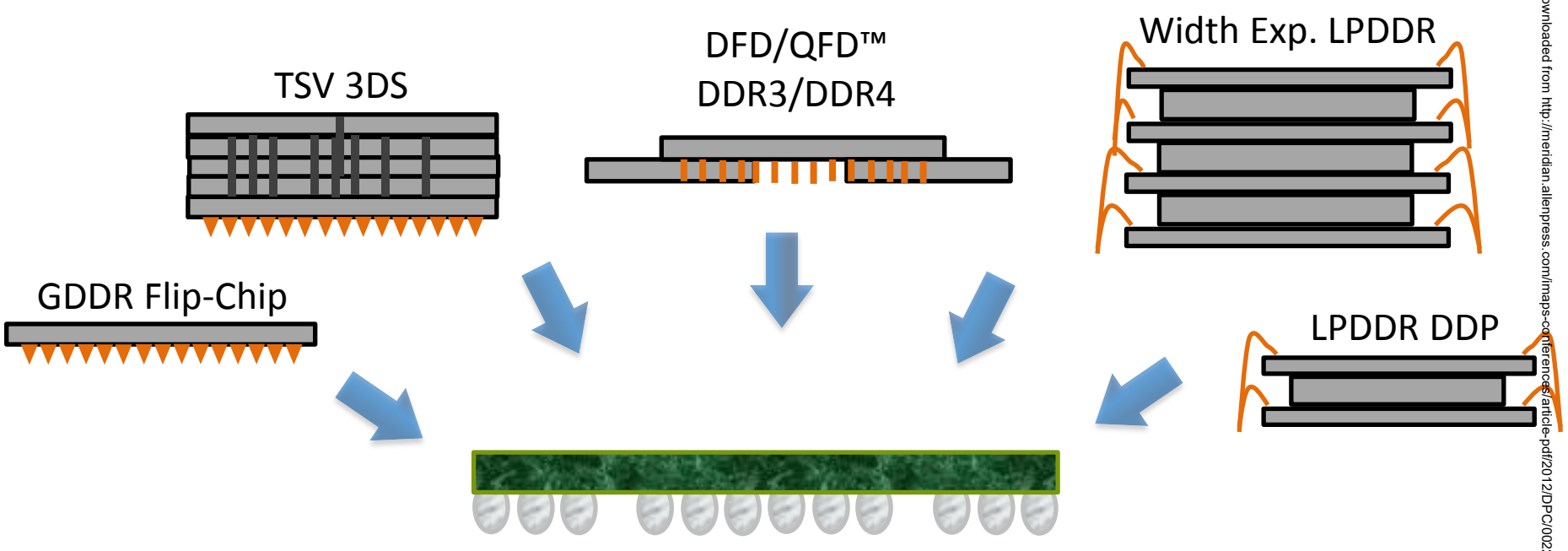


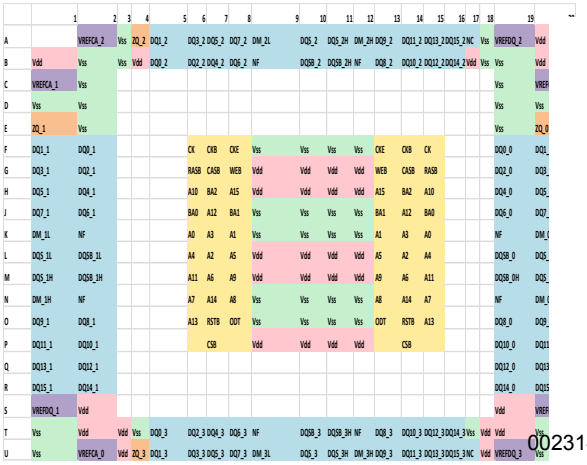
- 300um die-edge to package-edge clearance
- 5.7x7.28mm die placement shown
- 475um bond window edge –to- solder land edge clearance

- 16.0x16.0mm package outline
- 0.8x0.8mm ball pitch
- 1.1mm wide bond windows

invensas™

A Universal Package: DDR & LPDDR Co-Support





002314

Thank You

info@invensas.com