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shaping tomorrow with you

Hybrid Bonding Methods Using Ultra Precision Cutting for 3D-SIC

Taiji Sakai[1)], Nobuhiro Imaizumi[1)], Masataka Mizukoshi[1)]
Masayuki Kawase[2)], Ryoji Tanimoto[2)], Takashi Mori[2)]
Kohei Takeda[3)], Toshio Enami[3)],

FUJITSU LABORATORIES LTD.[1)]
DISCO Corporation[2)]
SEKISUI CHEMICAL CO., LTD.[3)]

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Outline

Background and Objective

- Demand of underfilling for 3D-SIC integration

Hybrid Bonding Technology

- Requirements
- Low temperature Cu-Cu bonding technology

Investigations

Conclusions

System in Package Technology Trends

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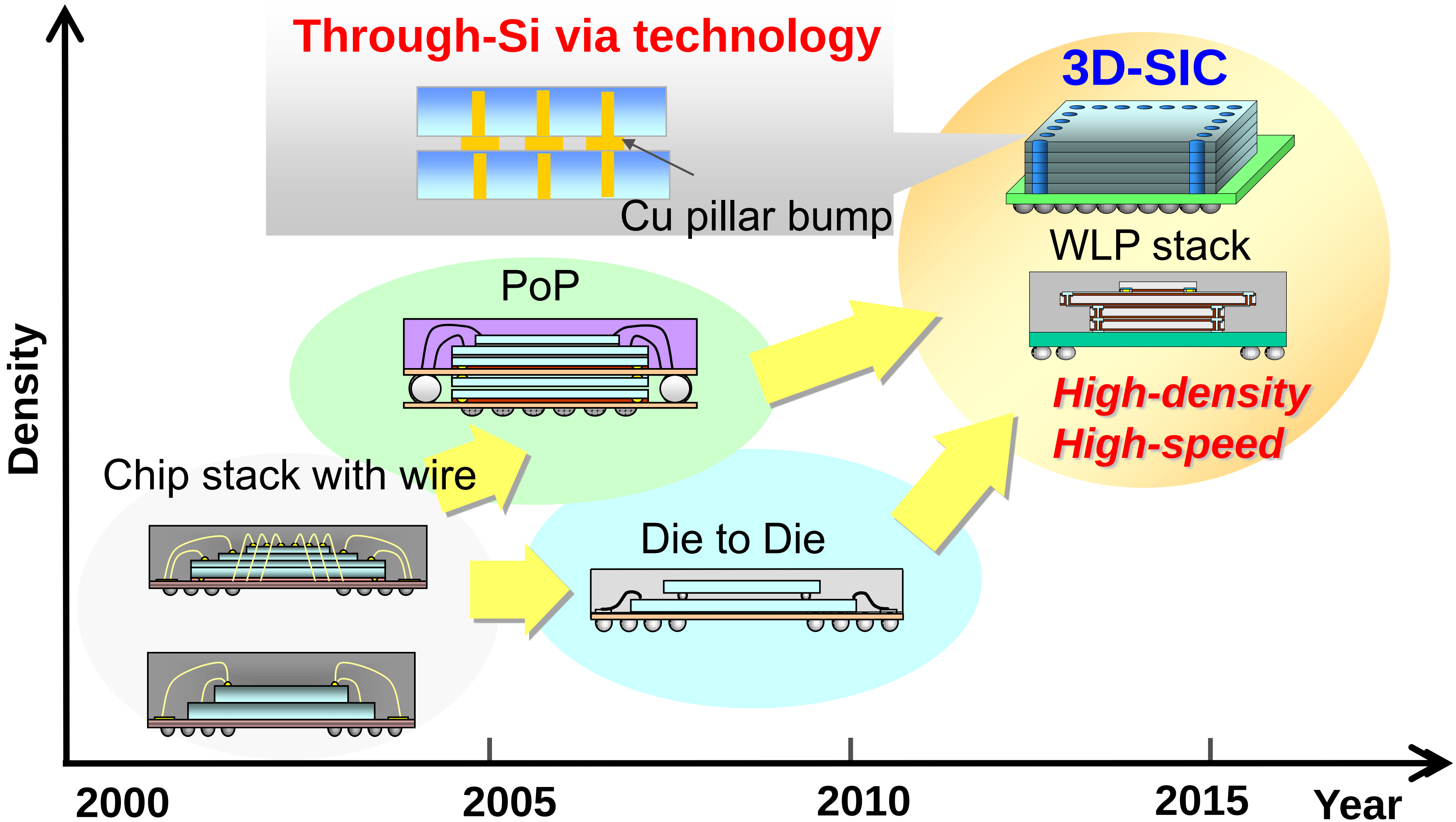

Fine pitch interconnection is the key technology

Fine Pitch Interconnection for 3D-SIC

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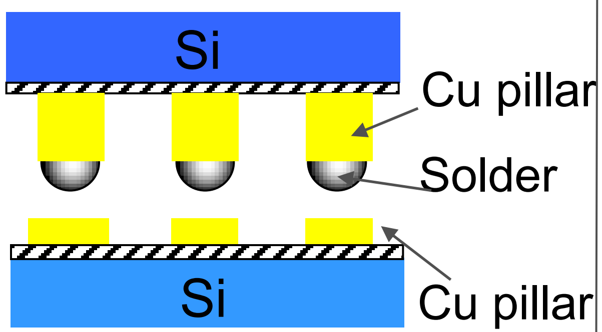
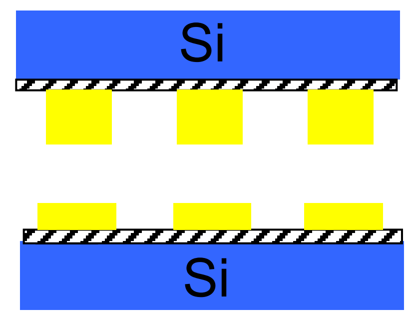
Bump type	Cu pillar + solder	Cu pillar + Cu pillar
Bonding method	Fusion bonding	Solid diffusion bonding by thermocompression
Structure		
Electrical Resistivity	11 μΩcm	1.7 μΩcm
High current density effect	Electromigration	Stable
Available bonding pitch	> 10 μm	>2 μm
Bonding temperature	217-250 °C	200-250 °C *

Cu-Cu bonding has advantages for 3D-SIC

* Reported in Devie Packaging 2011

Demand for 3D-SIC Integration

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Further integrated 3D-SIC

- Bonding pitch <5 µm
- Device gap <10 µm

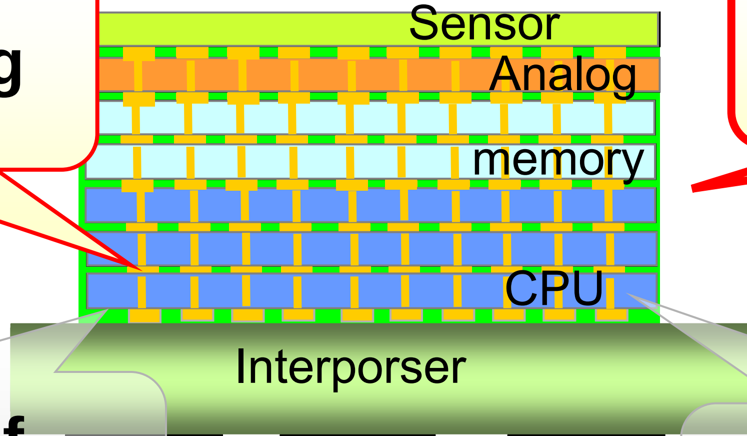
Device Packaging 2011

Cu-Cu bonding

Device Packaging 2012

Undefilling

- Attach thinner ICs
- Protect smaller bonding electrodes



Reliability of stacked ICs

Multichip stacking process

Cu-Cu bonding and underfilling process must be realized

Conventional vs Hybrid Bonding

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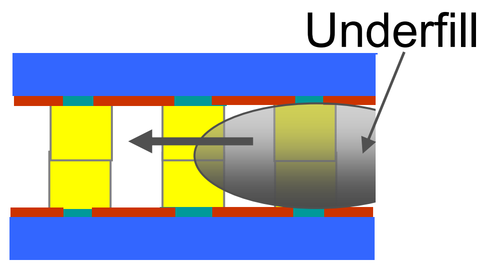
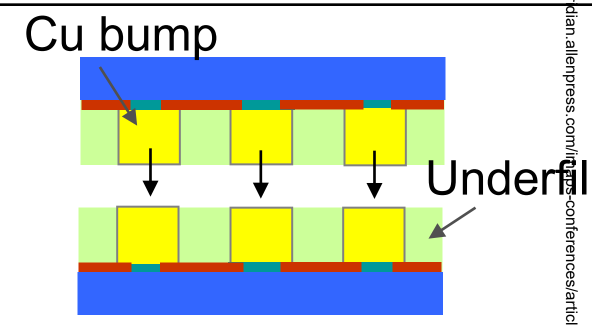
Hybrid bonding is advantageous for 3D-SIC

	Conventional bonding	Hybrid bonding
		
Underfill type	Capillary filling	Pre-applied
Supply area size	Individual chip size	**Wafer size**
Narrow gap filling	Difficult	**Easy**
Degasification	N/A	Potentially affected
Underfill infiltration into interface	N/A	Potentially occurs

Affect to solid diffusion

Objective of the Present Study

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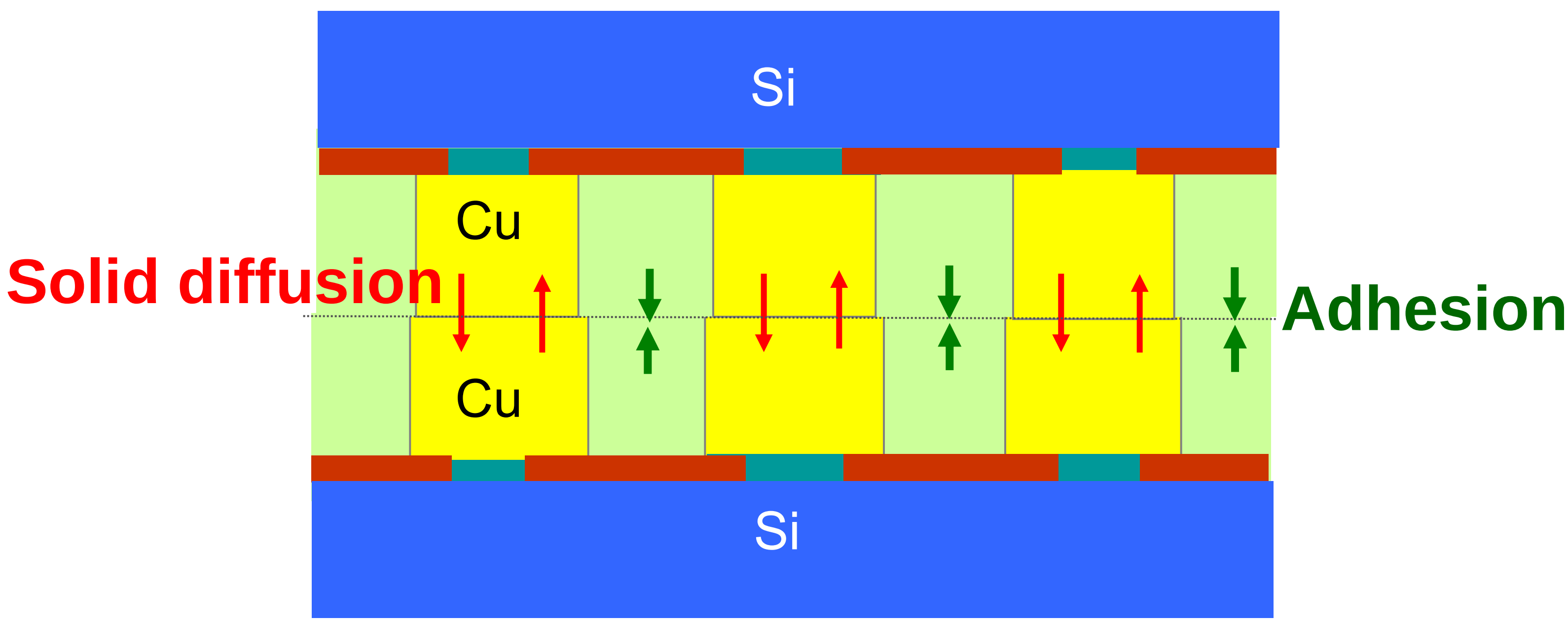
To realize hybrid bonding with Cu-Cu solid diffusion



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Outline

- Background and Objectives
  - Demand of underfilling for 3D-SIC integration
- **Hybrid Bonding Technology**
  - **Requirements**
  - **Low temperature Cu-Cu bonding technology**
- Investigations
- Conclusions

Requirements of Hybrid Bonding

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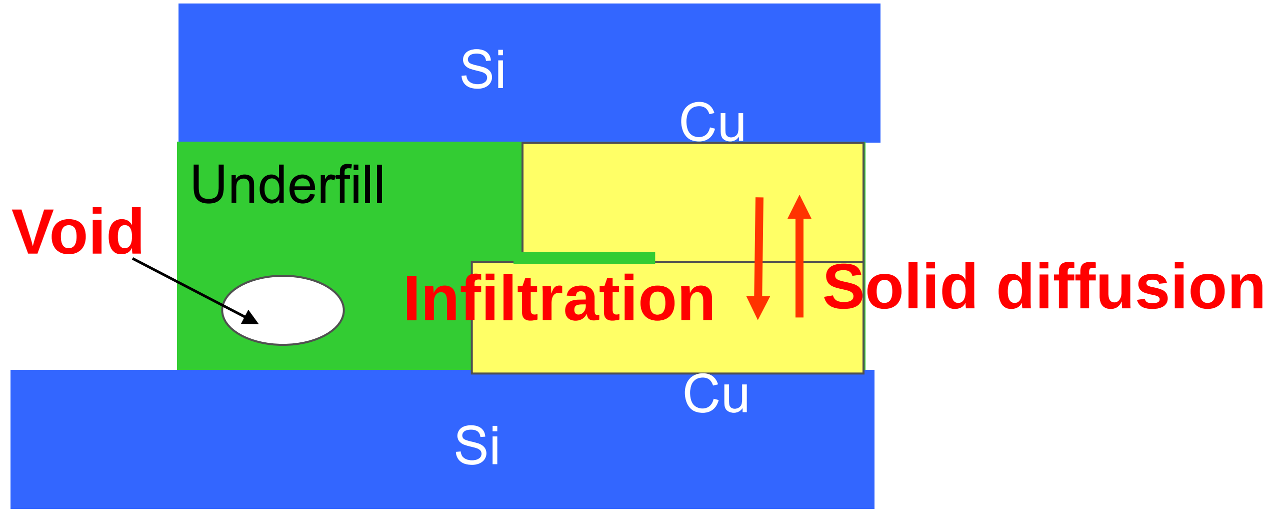
- **Low temperature Cu-Cu bonding**
  - Thermostability of underfill is not too high
- **Cu-Cu solid diffusion**

Device Packaging2011 (without underfill)

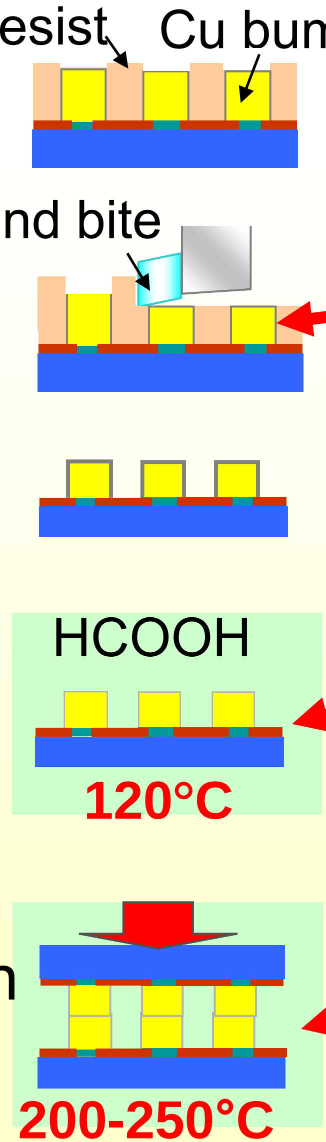
- **No underfill infiltration into bonding interface**
- **No void formation**



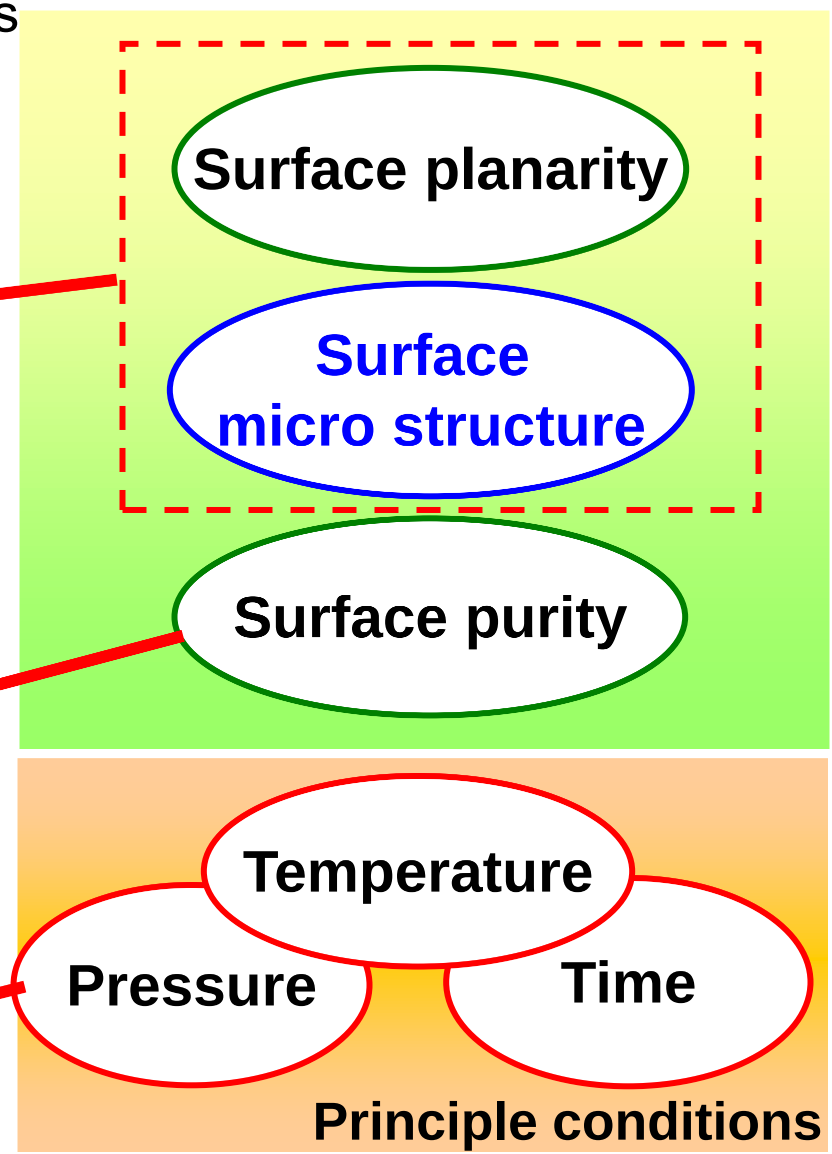
Our Cu-Cu Bonding Process

T. Sakai, et al," DPC 2011

- Electroplating
- **Cutting**
- Resist removal
- **Reduction**
- Thermocompression



Factors that affect Cu-Cu bonding



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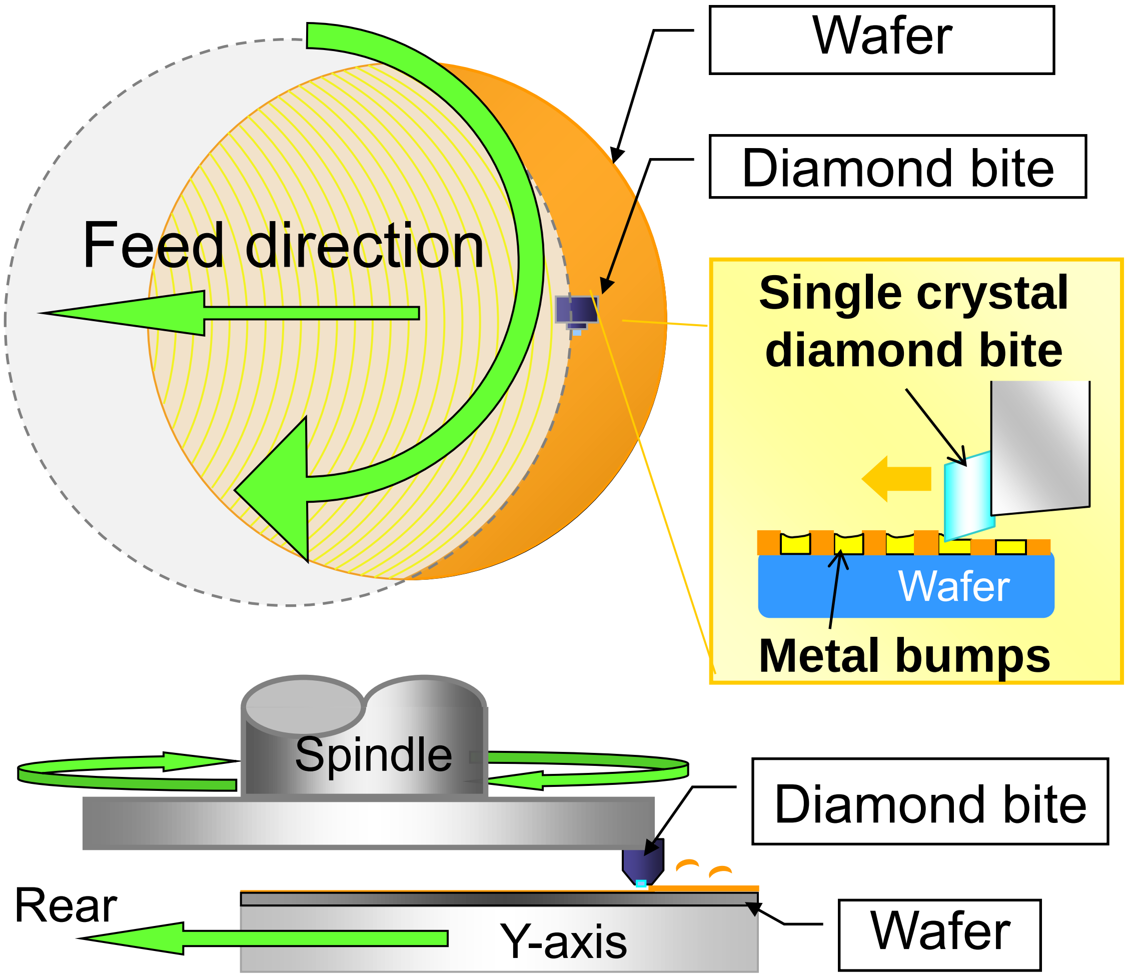
Surface Planarity Improvement

Ultra Precision Cutting by Using Diamond Bite

T. Sakai, et al," IMAPS 2006.



■ Feature

- Creep feed cutting with diamond bite
- Wet / dry process
- Various work shape

Commercialized by DISCO Corporation

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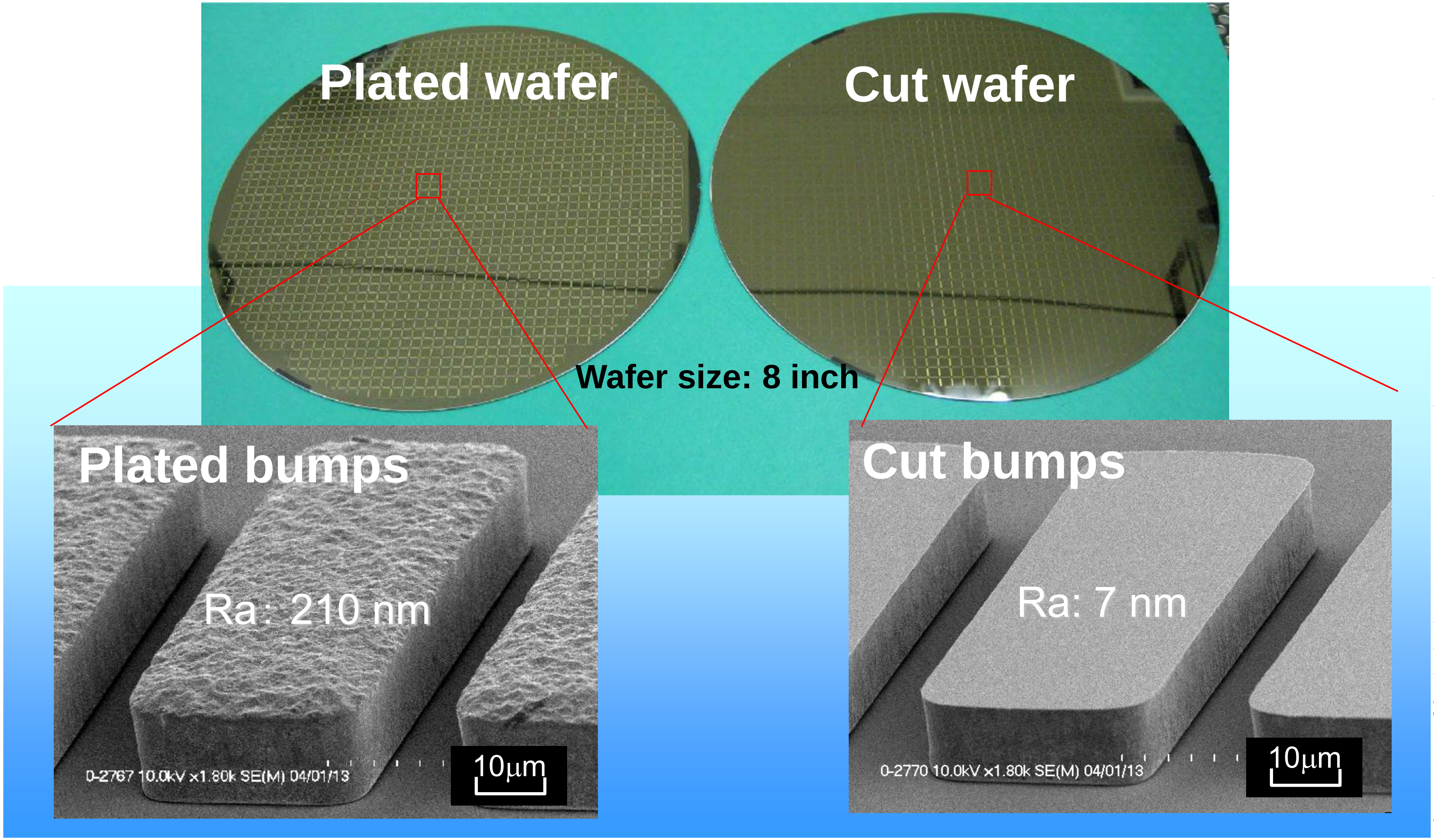
Planarity of Cut Bumps



Highly flat and smooth surfaces could be obtained

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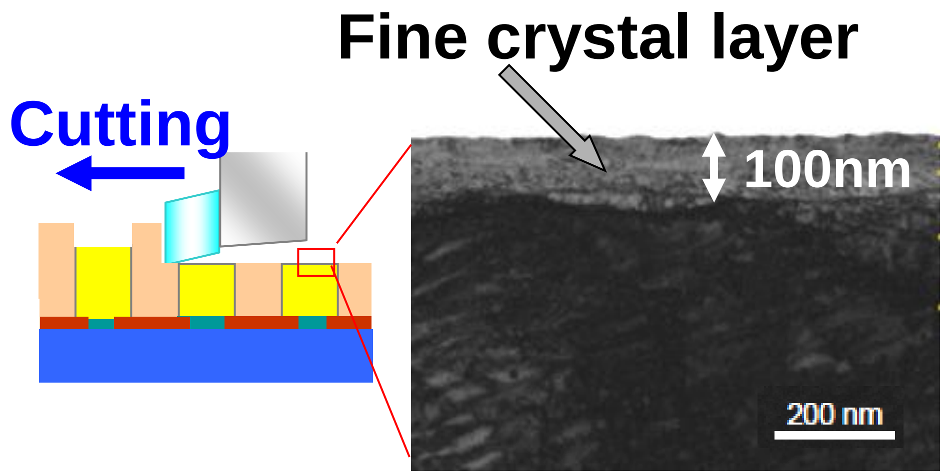
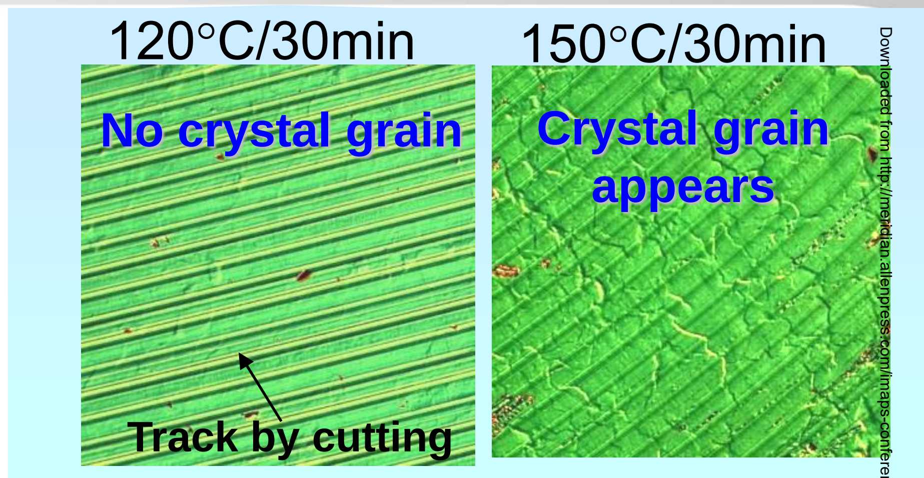
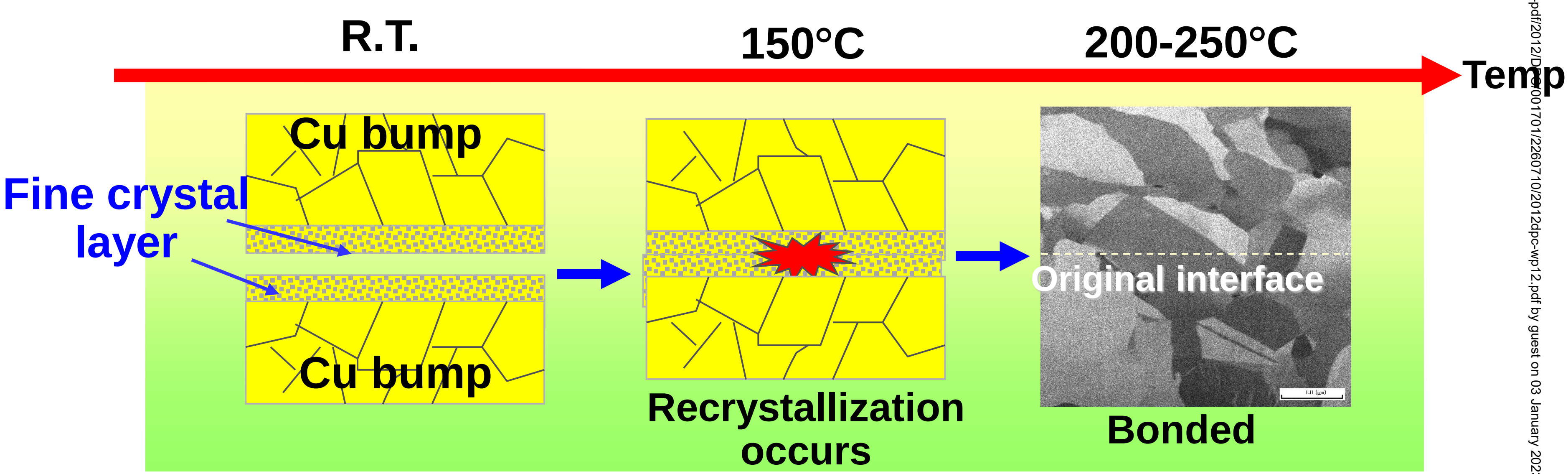
Surface Micro Structure Improvement





Recrystalization at low temperature



Fine crystal layer led to low temperature bonding

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Surface Purity Improvement

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"Reduction" is key

Wet process

- Sulfuric acid
- Citric acid
- Hydrochloric acid

Moisture absorption problem to adhesive

Dry process

- Hydrogen gas
  - High temperature >300°C
- Ar ion beam
  - High vacuum condition
- Formic acid vapor
  - **Low temperature >120°C**

Favorable for hybrid bonding process

We selected formic acid vapor process

Reduction by Formic Acid

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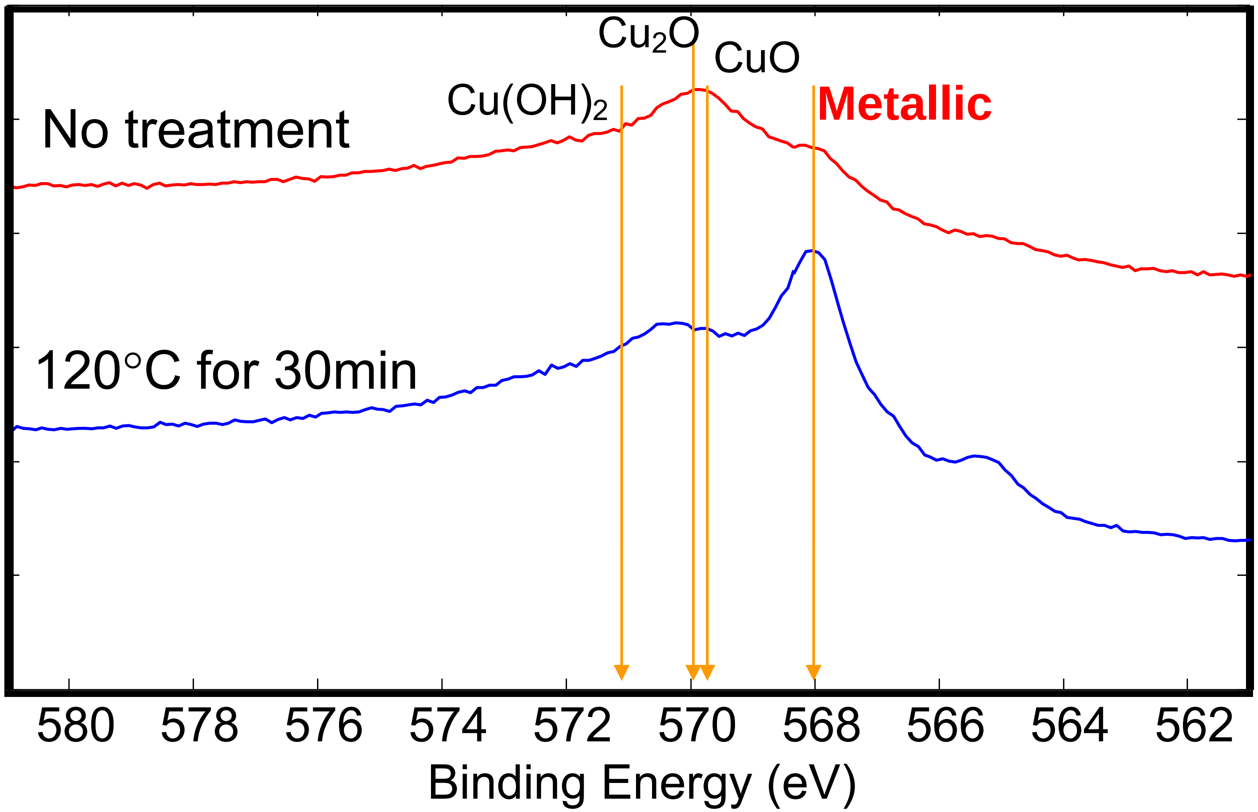
Cu LMN Auger Spectrum by XPS analysis



- Metallic Cu peak was obtained in 120°C for 30min

Low temperature reduction process is possible

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  - Low temperature Cu-Cu bonding technology
- **Investigations**
- Conclusions

Evaluation Sample

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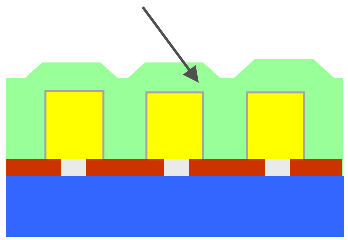
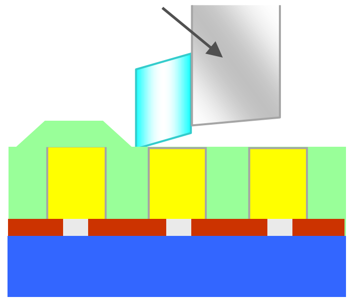
Hybrid structure formation

Underfill (Epoxy)



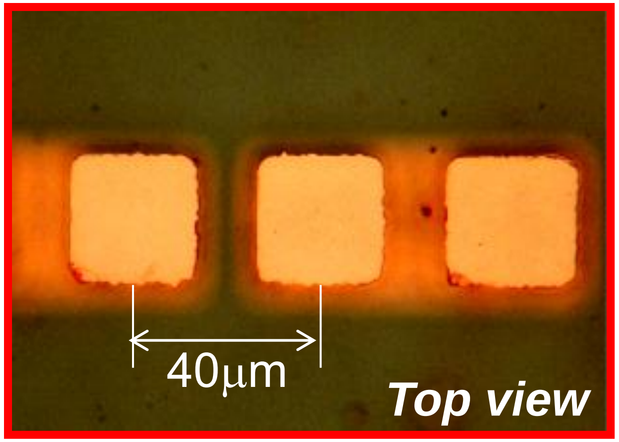
Spin coating on the wafer

Diamond bite



Simultaneously cutting

Cut Cu bump/ underfill surface

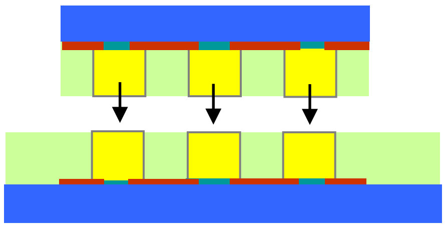


Excellent cutting result

Bonding sample- Die to Die type

		Si chip	Si substrate
Chip size	mm	5×5	15×15
Chip thickness	μm	625	625
Bump size	μm	20×20	25×25
Bump height	μm	10	10

Si chip



Si substrate

Investigated Bonding Process Flow

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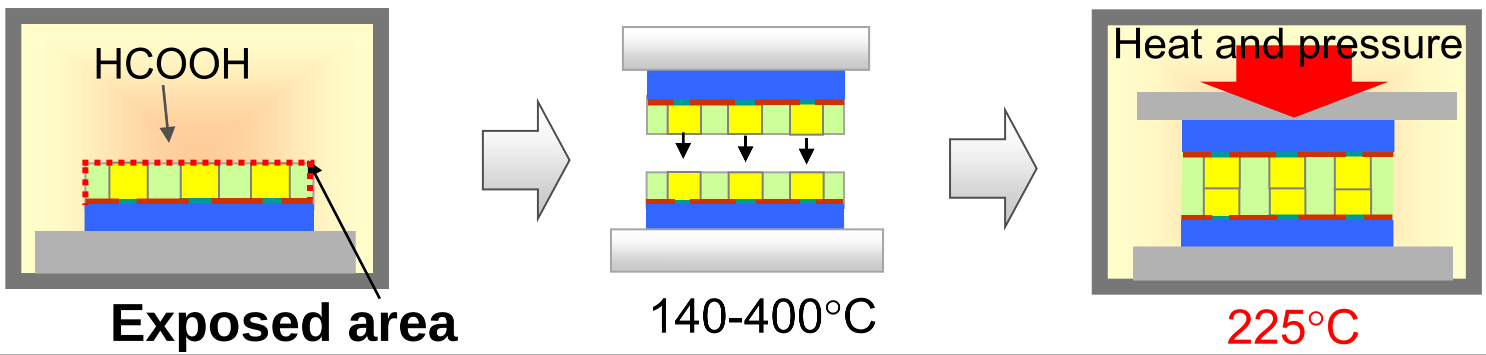
Examine how underfill is exposed by formic acid

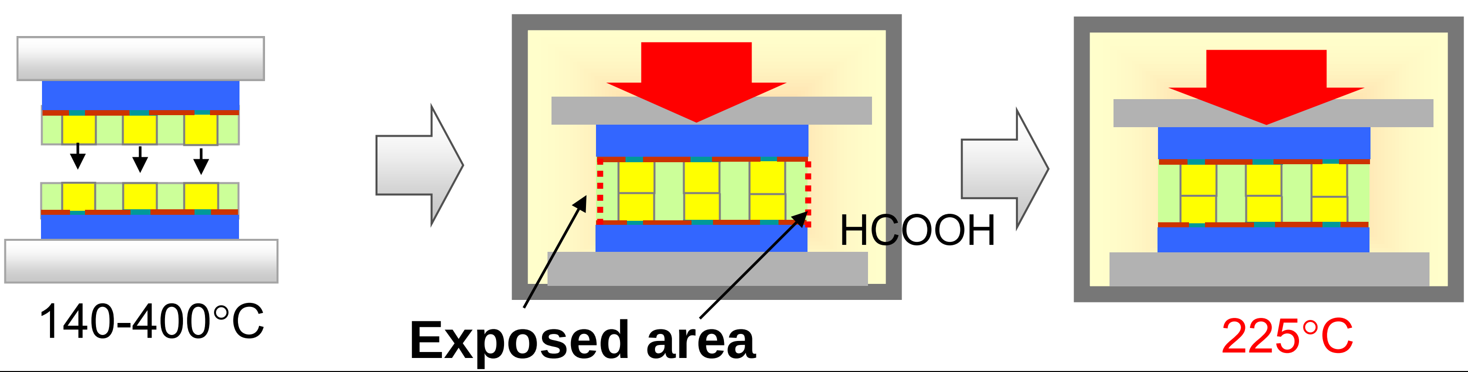
■ Totally exposed by formic acid

Reduction	Temporary bonding	Permanent bonding



■ Partially exposed by formic acid

Temporary bonding	Reduction	Permanent bonding



Investigation Items

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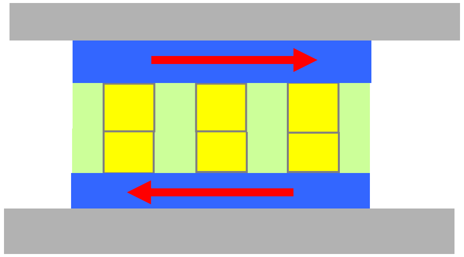
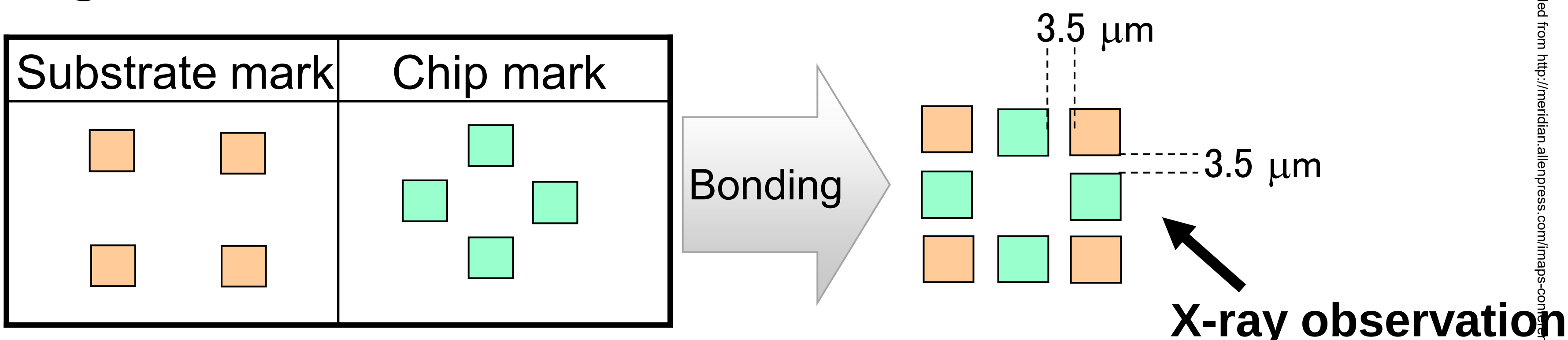
- Bonding mismatch evaluation
- Evaluation of bondability
  - Confirmation of solid diffusion
  - Void observation
- Underfill damage by formic acid
- Formic acid penetrability
- Underfill infiltration into bonding interface



Slip each other

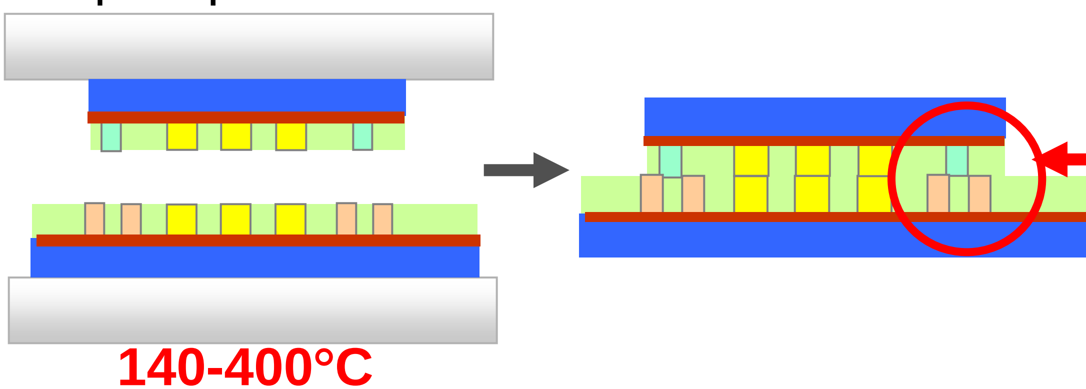
Bonding Mismatch Evaluation

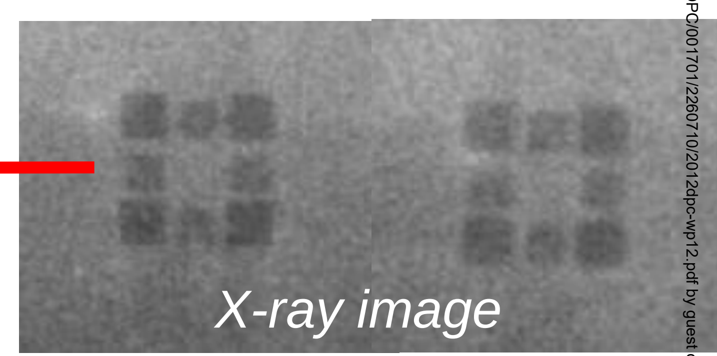
Alignment mark



X-ray images after temporary bonding

Flip chip bonder





All samples were confirmed within 2µm mismatch after temporary bonding

Bonding Mismatch after Permanent Bonding

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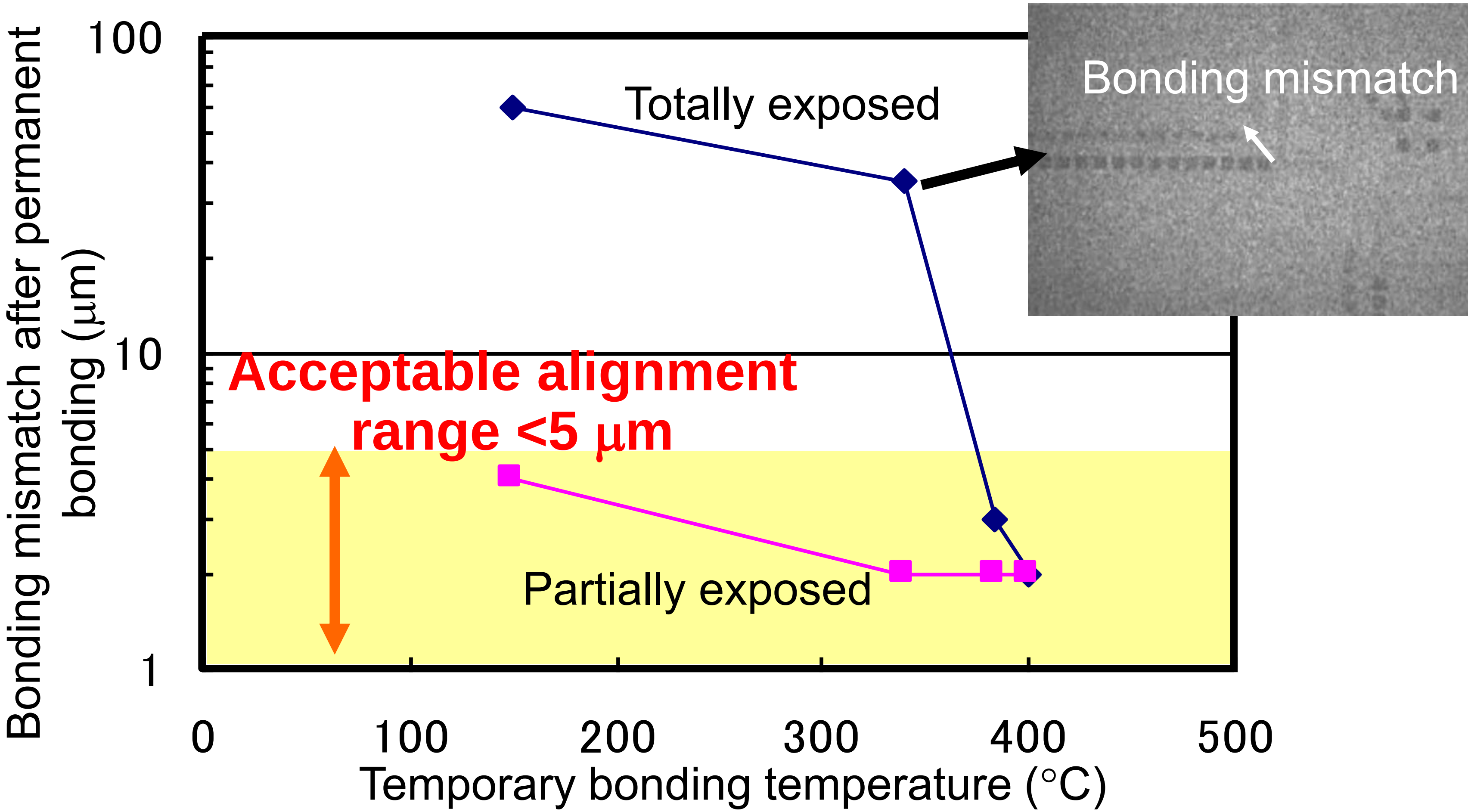

Totally exposed underfill could not sustain arranged location during bonding process

Partially exposed process shows less mismatch

Adhesion Damage by Formic Acid

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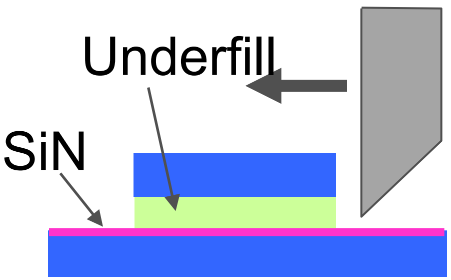
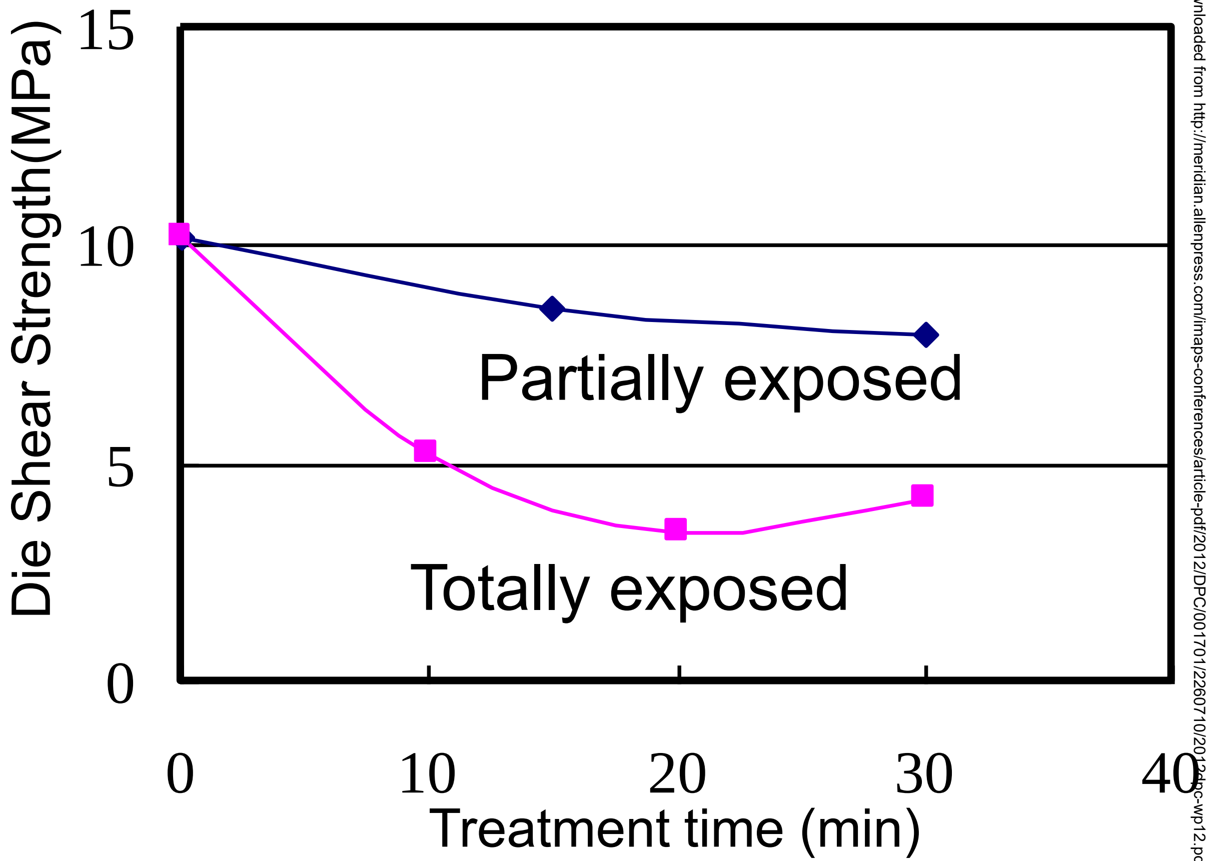
- Die shear testing



- Underfill conditions
  - Partially exposed
  - Totally exposed



Partially exposed: slightly decreases
Totally exposed: decreases below half level of the initial value

Decreases of adhesion strength by formic acid would cause mutual slipping

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Bonding Results

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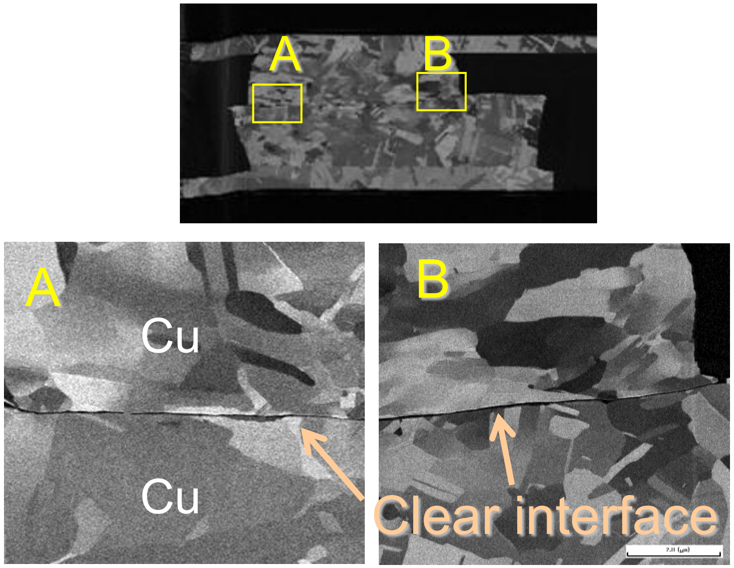
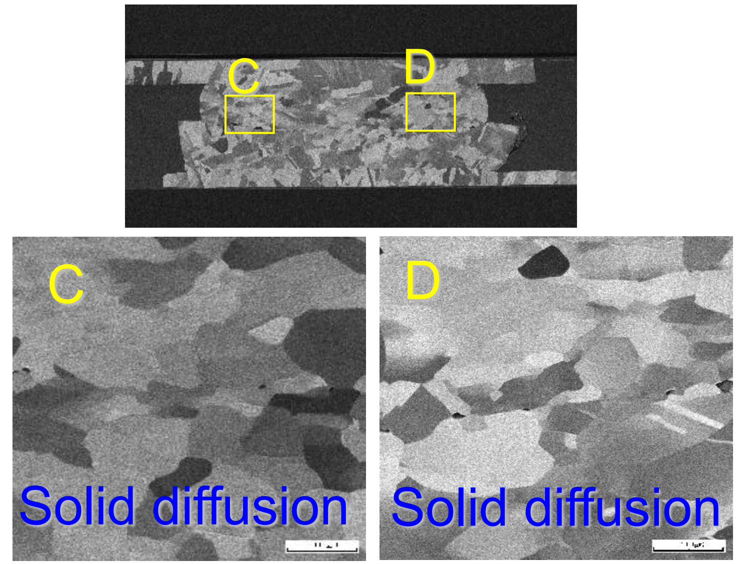
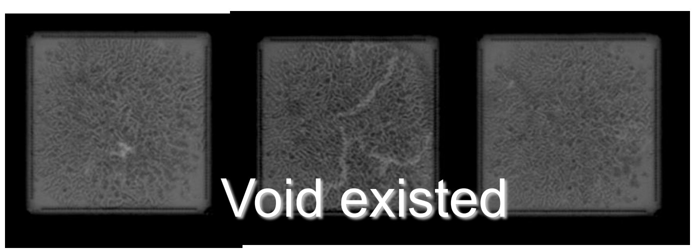
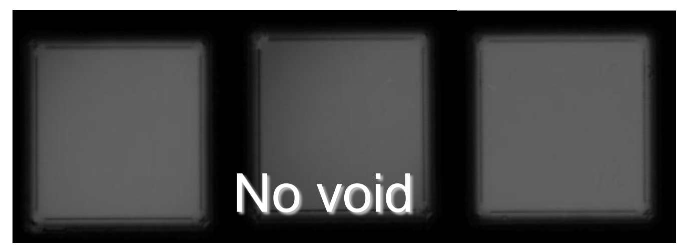
	Totally exposed process	Partially exposed process
	Temporary bonded at 400°C	Temporary bonded at 140°C
Cross sectional images		
C-SAM images		

C-SAM: Constant-depth mode Scaning Acoustic Microscorpe

Solid diffusion and voidless bonding could be achieved in partially exposed process

Underfill Damage by Formic Acid

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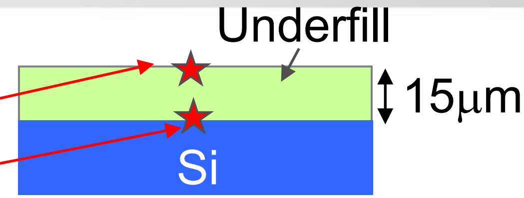
Microscopic FT-IR analysis

1. Uncured
2. Formic acid/ top side
3. Formic acid/ Si side
4. Completely cured



Epoxy hardening

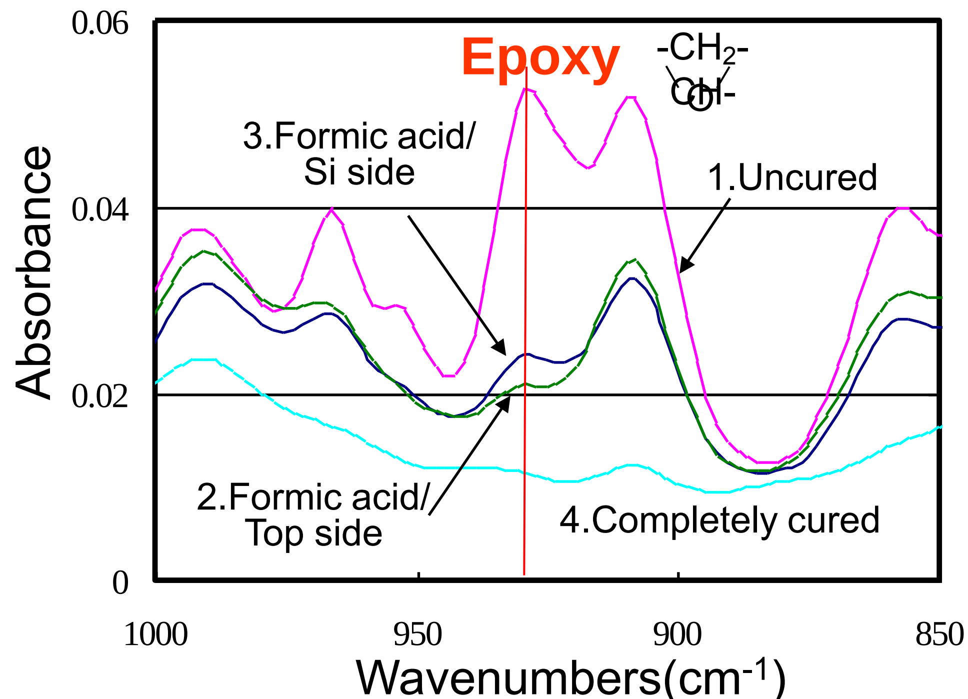
↓

CH_2-O-CH- peak decreases

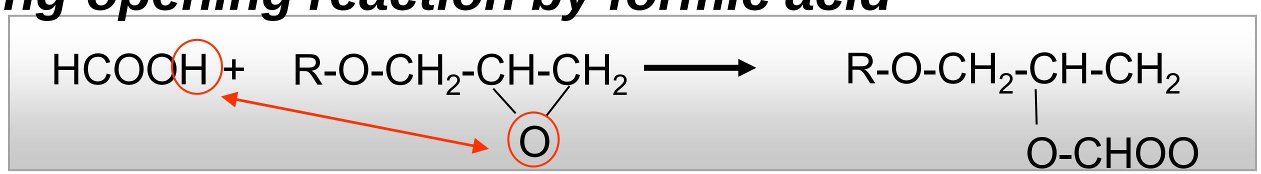
Normalized cure degree

Formic acid/ top side: 88%

Formic acid/ Si side: 70%



Ring-opening reaction by formic acid



Epoxy hardening propagates on top side of underfill

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Problems of Totally Exposed Process

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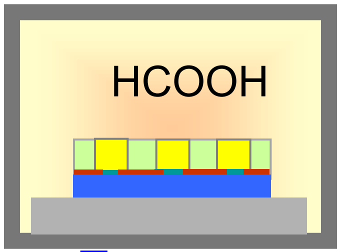
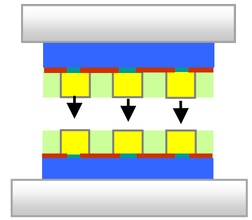
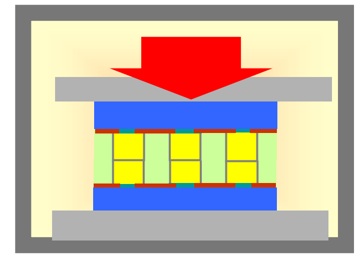
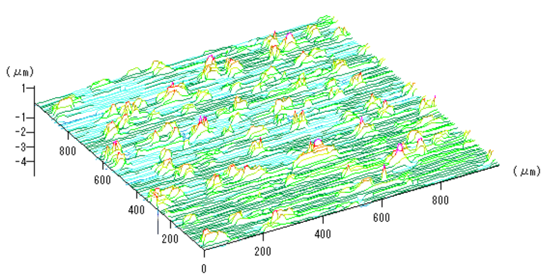
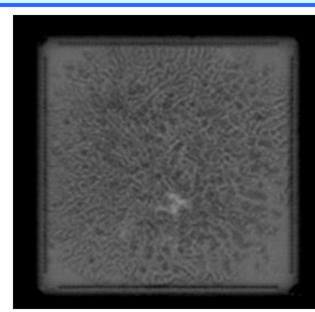
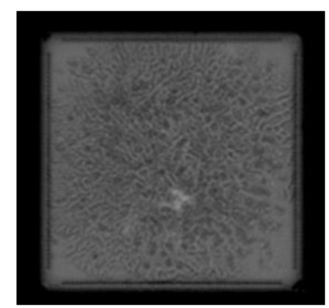
Reduction	Temporary bonding	Permanent bonding
		
Face up	140-400 °C	225 °C

Decrease of adhesion strength	High temperature condition is required > 400°C	Dispersion of bonding force leads to no solid diffusion
Lost of smooth surface	Void formation	Void formation







It is difficult to achieve voidless and solid diffusion

Advantage of Partially Exposed Process

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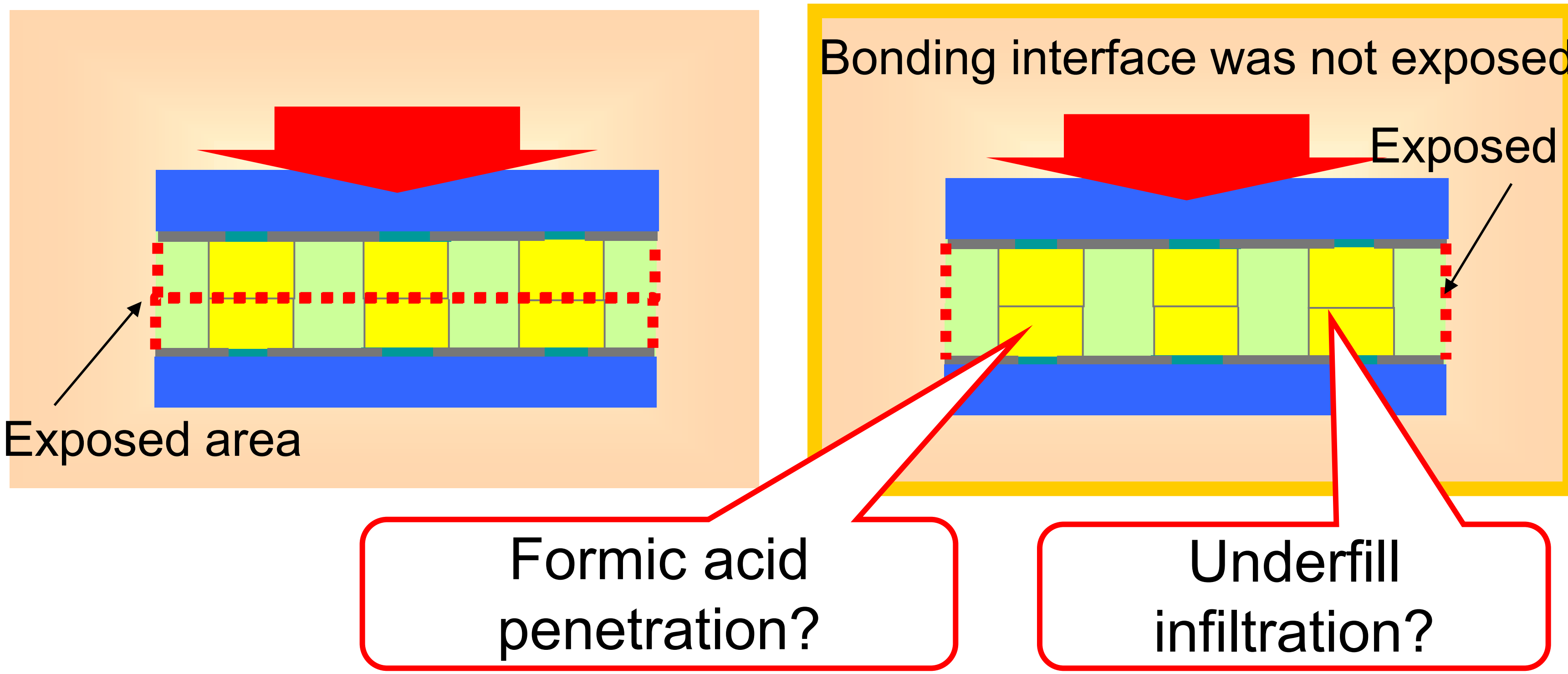
Underfill adhesion can be maintained.

Totally exposed

Partially exposed



Compare two conditions by TEM

- N_2 atomosphere
- Formic acid vapor

EDX analysis

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Formic Acid Penetration

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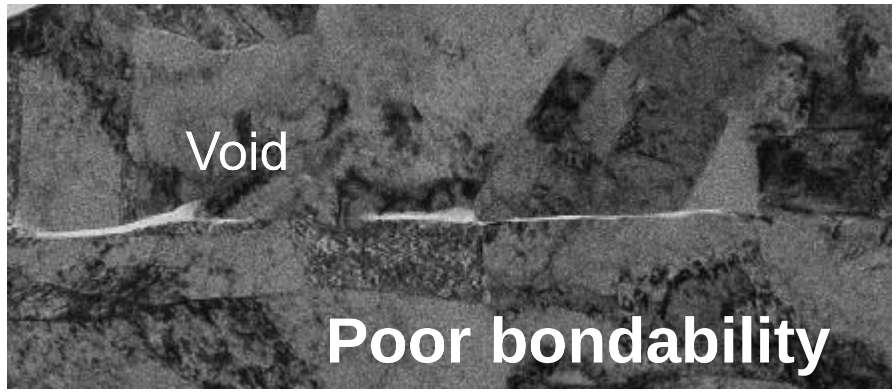
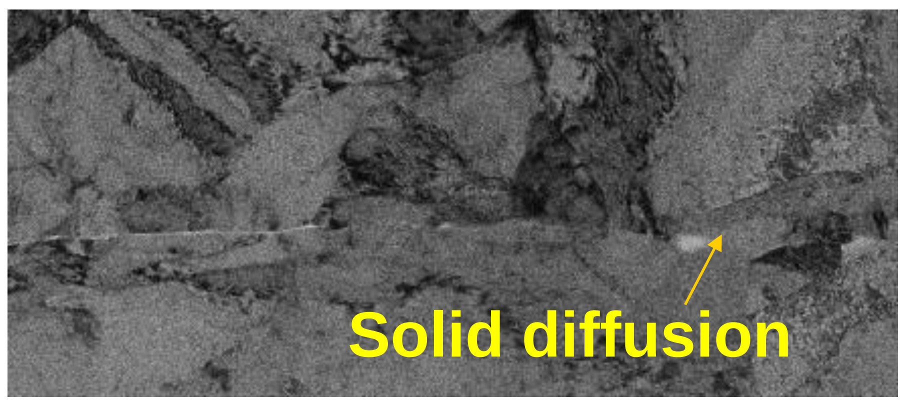
Void exists between interface under N_2 atmosphere condition.

N_2 atmosphere



Formic acid



Formic acid penetrates into the bonding interface

Examination of Undefill Infiltration

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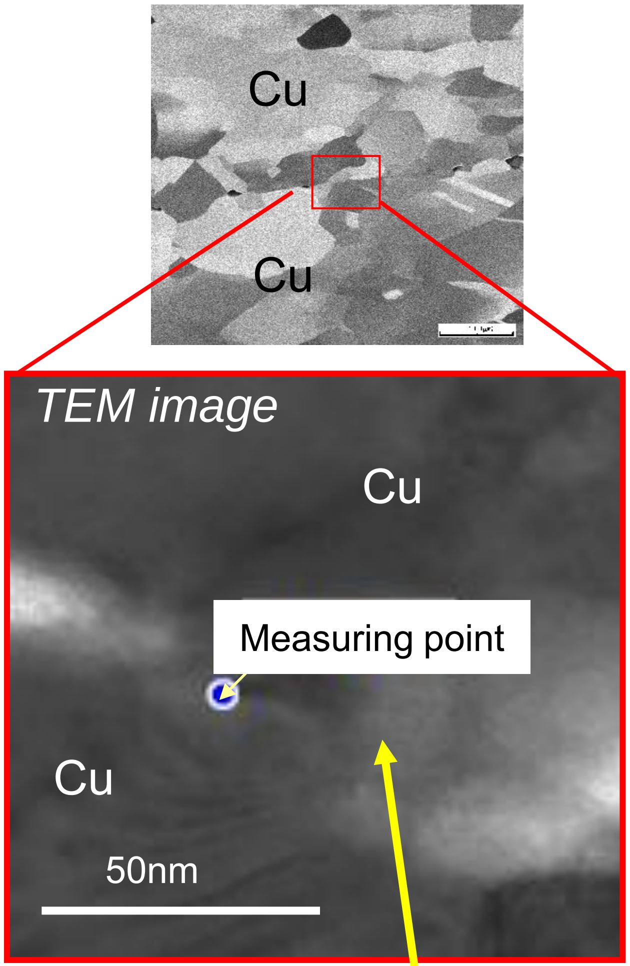
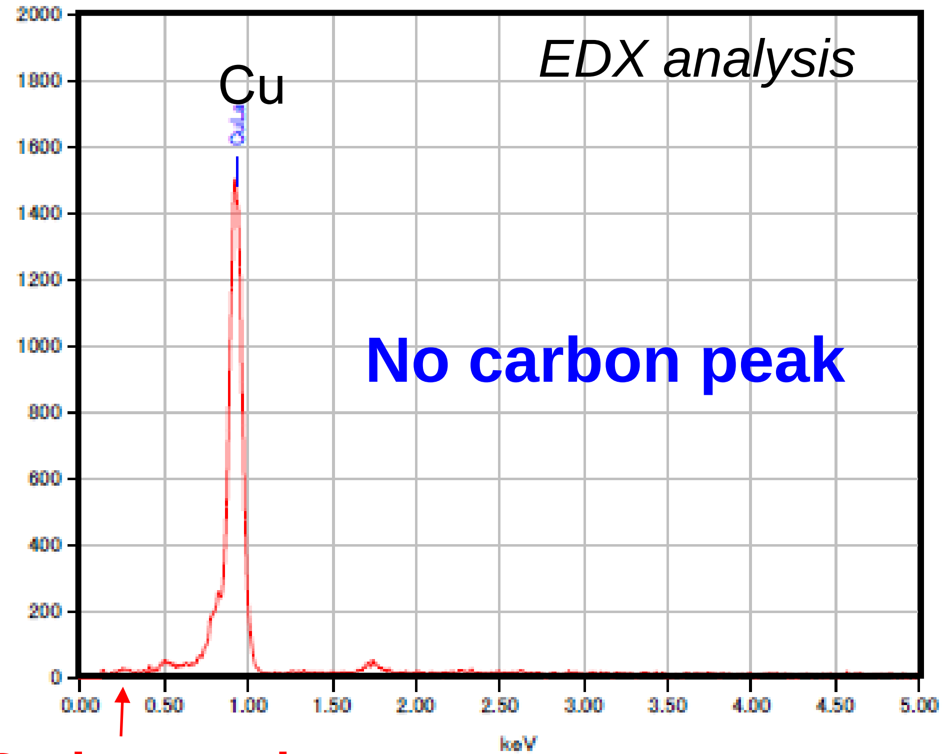
Bonding interface of partially exposed process





Cu-Cu metallic bond was confirmed

No underfill infiltration into the bonding interface

Conclusions

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- Underfill and Cu bumps can be simultaneously cut together by diamond bite with no residue on bump.
- Partially exposed process where the exposure area by formic acid is limited can achieve solid diffusion and no void formation.
- It is considered that formic acid penetrates into the bonding interface and removes oxidation layer.
- There is no underfill infiltration into the bonding interface in partially exposed process.

We have developed both underfilling and Cu-Cu solid diffusion process, which are promising methods for 3D-SIC.

Multi chip stacking process and reliability of stacked ICs are for the future work.

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