TSV Market Drivers, Demand & Product Readiness

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SVP, Adv. 3D Interconnect Platform Develop

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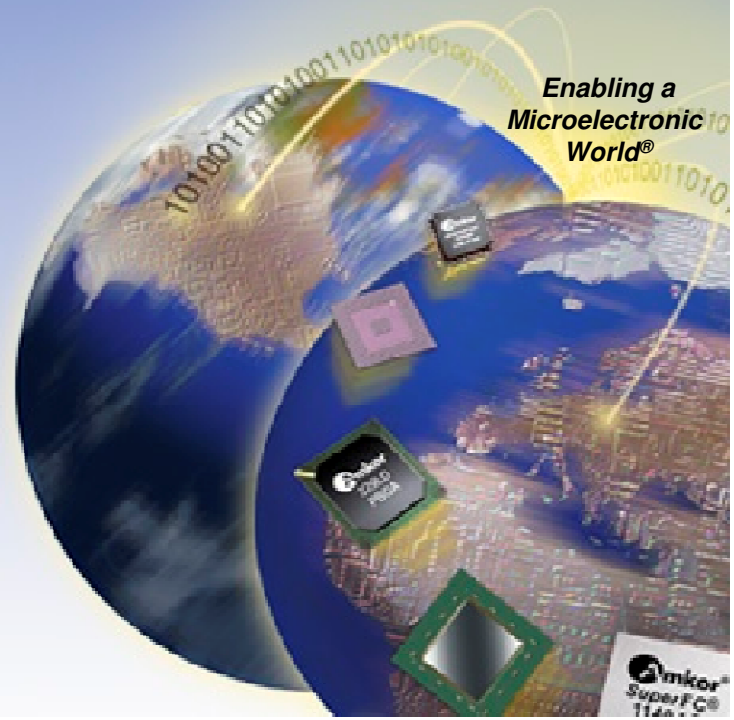


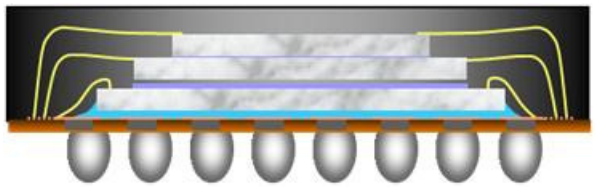
Topics

- TSV Platform Drivers
- Interposer Supply Chain Logistics
- Product Offerings & Timing
- Conclusion

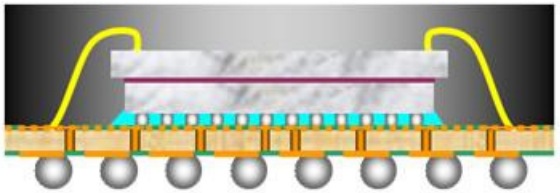
TSV Platform Drivers

"Technology Convergence"

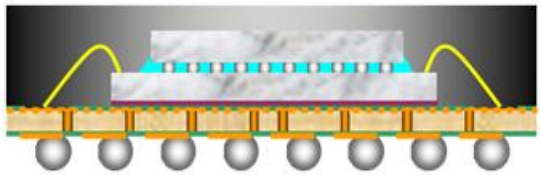
Stacked CSP (SCSP) – Migration *to TSV*



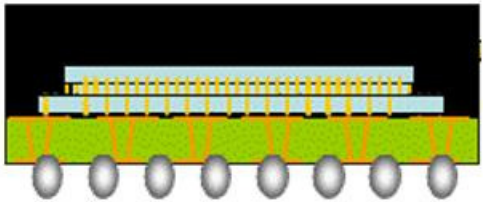
Stacked CSP



FlipStack® CSP



F2F FlipStack®



TSV Stacked CSP

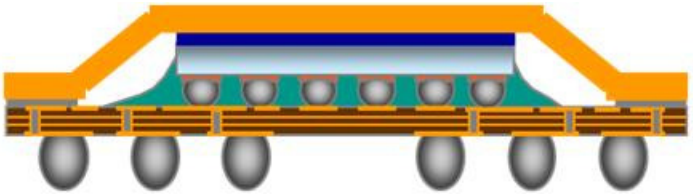
Performance Driven

Compared to POP Memory

- *8x performance in bandwidth*
- *50% power savings*

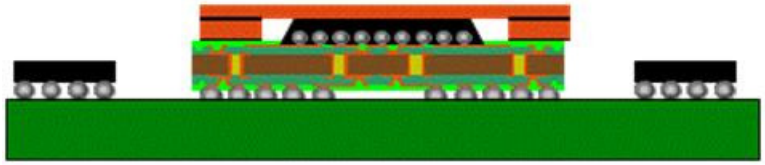
Courtesy of Samsung

FCBGA – Migration *to TSV*

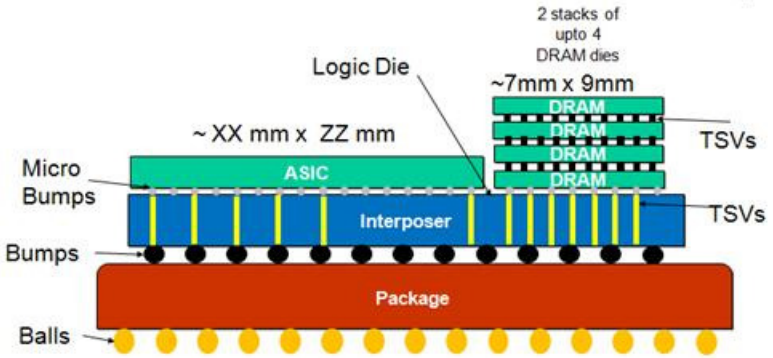


Logic with
Embedded Memory

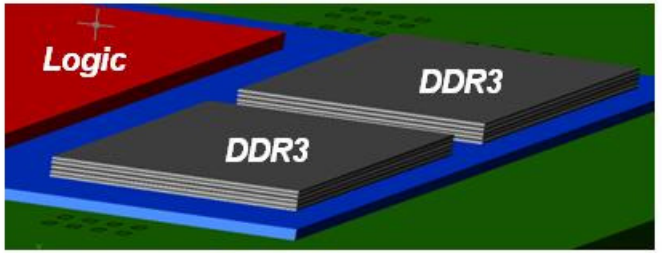
Logic and Memory
in Same Module



Logic and Memory
in Separate Packages



TSV Stacked BGA



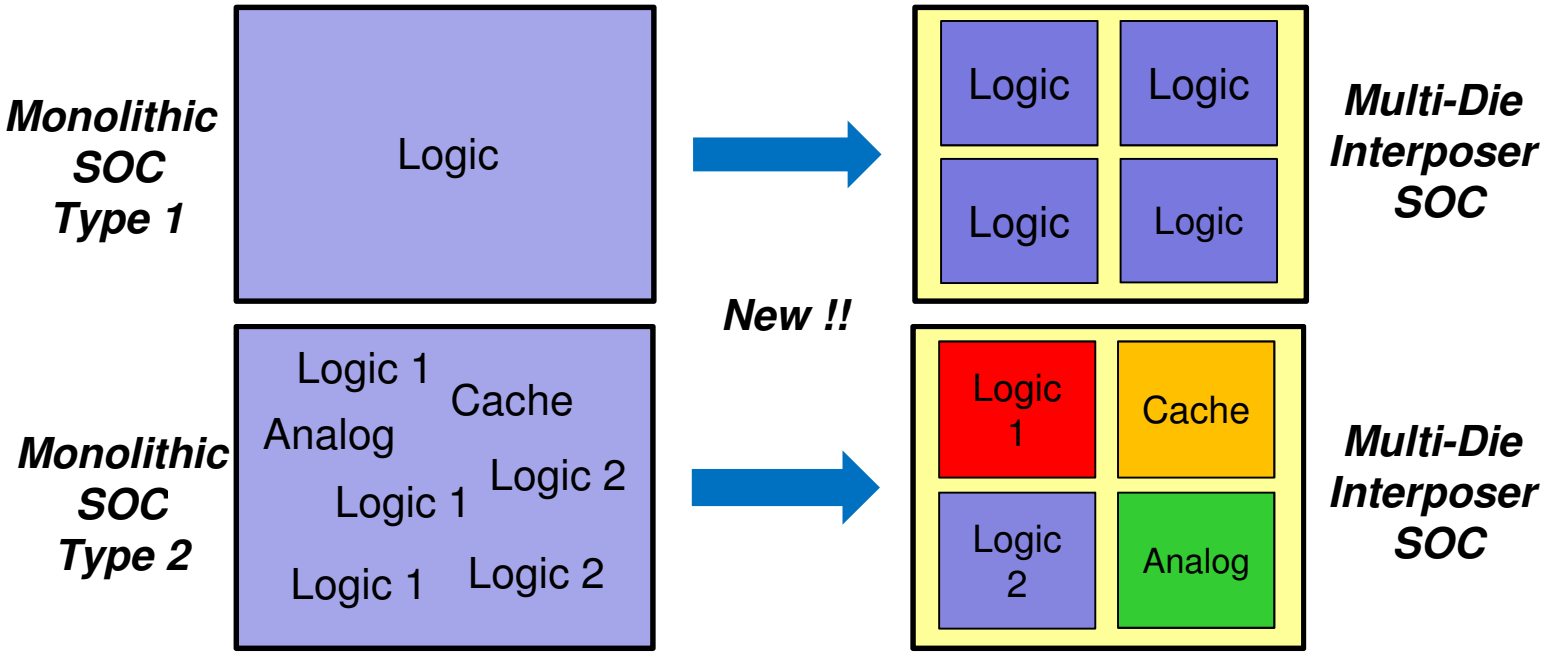
Performance & System Level
Cost Driven

TSV Product Segments

- **3D Vertical Stacking**
  - Memory and Application Processor Driven
  - Today CSP focused on 28nm CMOS… scaling to 20/22nm
  - Application Processors almost exclusively moving to OSAT finished wafer process flows

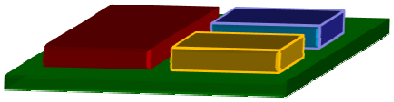
- **2.5D Interposer – Side by Side Stacking**
  - Network, GPU and CPU driven
  - All large package body focused
  - All large silicon interposer focused (near retical size)
  - Both Foundry finished and OSAT finished wafer process flows being used

3DIC TSV Product Opportunities



- Focus process node development on specific application functionalities
  - ✓ Reduces complexity and mask layer count of process node
  - ✓ Reduces advanced process node 'Time to Market'
  - ✓ Improves wafer yield
  - ✓ Reduces wafer start cost
- Improves performance, power, and area of each application functionality

Primary Drivers for Interposers

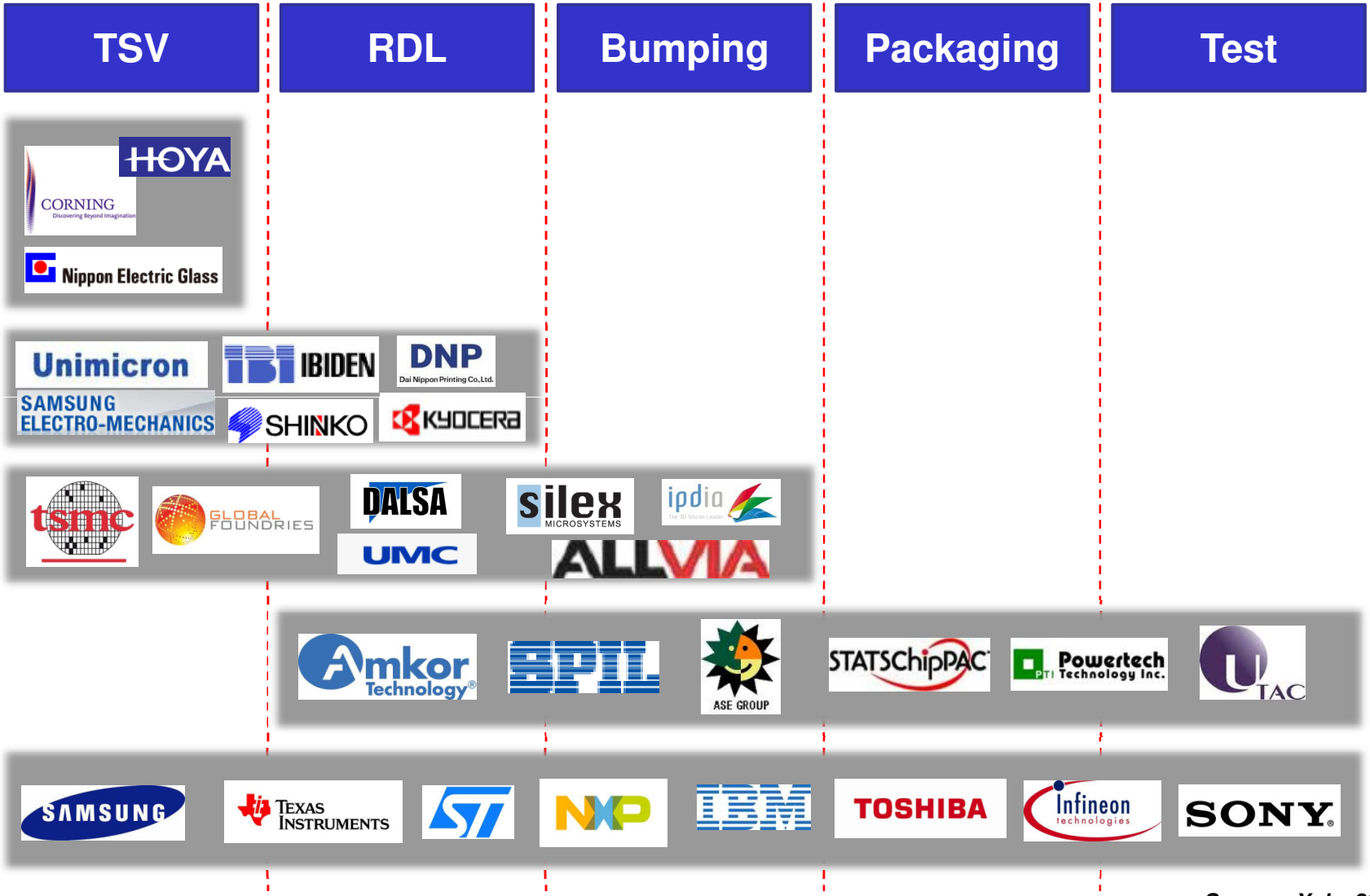
	Memory Bus Speed	Lower Power	Fab Yield	Cost	Stress Reduction in Top Die
Si Interp^T + DDR^T + Logic 	Wide Parallel Busses	Wide Parallel Busses	Departition Fewer SoC Layers	System Level Reduction	✓
Si Interp^T + Logic 		Gate to Gate Routing between Die	Deconstruct into Smaller Die	Fab Yield Improve = Cost Reduction	✓
Si Interp^T + Logic + SERDES 			Departition (e-DRAM)	System Level Reduction	✓

Interposer Supply Chain Logistics

Potential Interposer Technologies

- **Laminate (Organic)**
  - Delivered in large panel format (500x500mm typ.) with film based dielectrics
  - Several elite substrate manufacturers investigating today
- **Glass**
  - Can be delivered in panel (large) or wafer (8”) format at target thickness
  - Several companies investing in applicable capability to support packaged semiconductor products
- **Silicon**
  - Can be delivered in 8” or 12”
  - Several companies supporting this product space & a few others investigating
  - Leveraging idle foundry space on legacy node technologies

Who is Doing What?



Source : Yole, 2010

Interposer Supply Chain Challenges

- **Glass**
  - Panel format is strongest asset ; leveraging panel display market
    - Panel format presents challenges for CMP based activities (i.e. damascene processing)
    - More compatible with polymer dielectrics and ≥ 5µm line/space
    - Large panel plating process & Cu thickness variation
  - Via creation still very expensive in glass

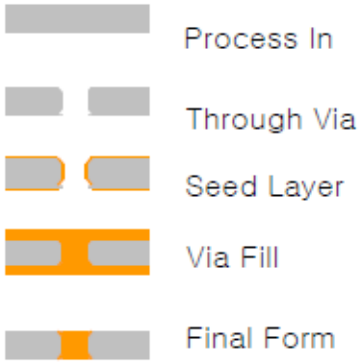
- **Laminate (organic)**
  - Elite '5' substrate suppliers targeting this space
  - Limited to ≥ 8µm line/space today and 40µm vias on 85µm pads
    - Development targeted at 5µm line/space ….but several years away
    - 5µm line/space requires stepper, and special resist technology
    - Via size/pad consumes too much space ; latency issues will limit adoption

Laminate vs Silicon Interposer

- **Through via by laser drilling or mechanical punching**

Si Interposer		S^3 Interposer
Wafer	Core Substrate Type	Panel
Silicon (3ppm/K)	Core Material	Organic (5ppm/K)
Dry Etch	Core Through Hole	Laser Via
PVD+Cu Plating (Semiconductor Process)	Through Hole Filling	E'less Cu+Cu Plating (PCB Process)
Wafer Thinning	Total Thickness Control	Core Thickness
100% (8 inch)	Net Die	135% (200 x 250 mm^2)

12 inch = primary path

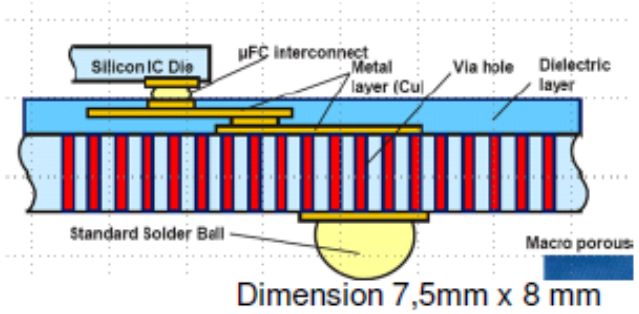


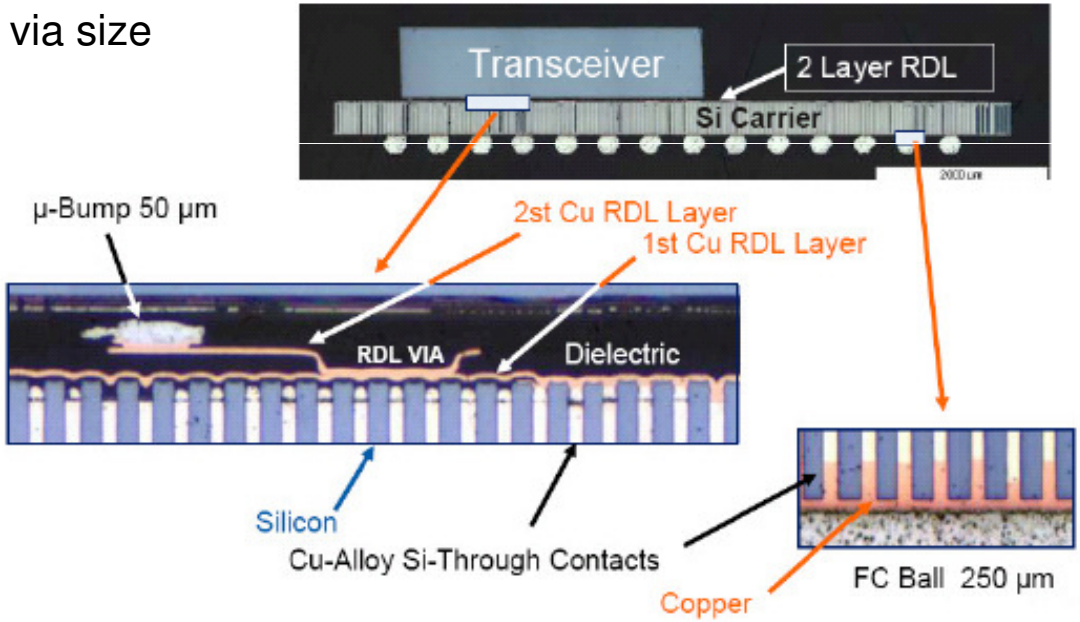
60~300µm available

Source : Samsung Electro-Mechanics

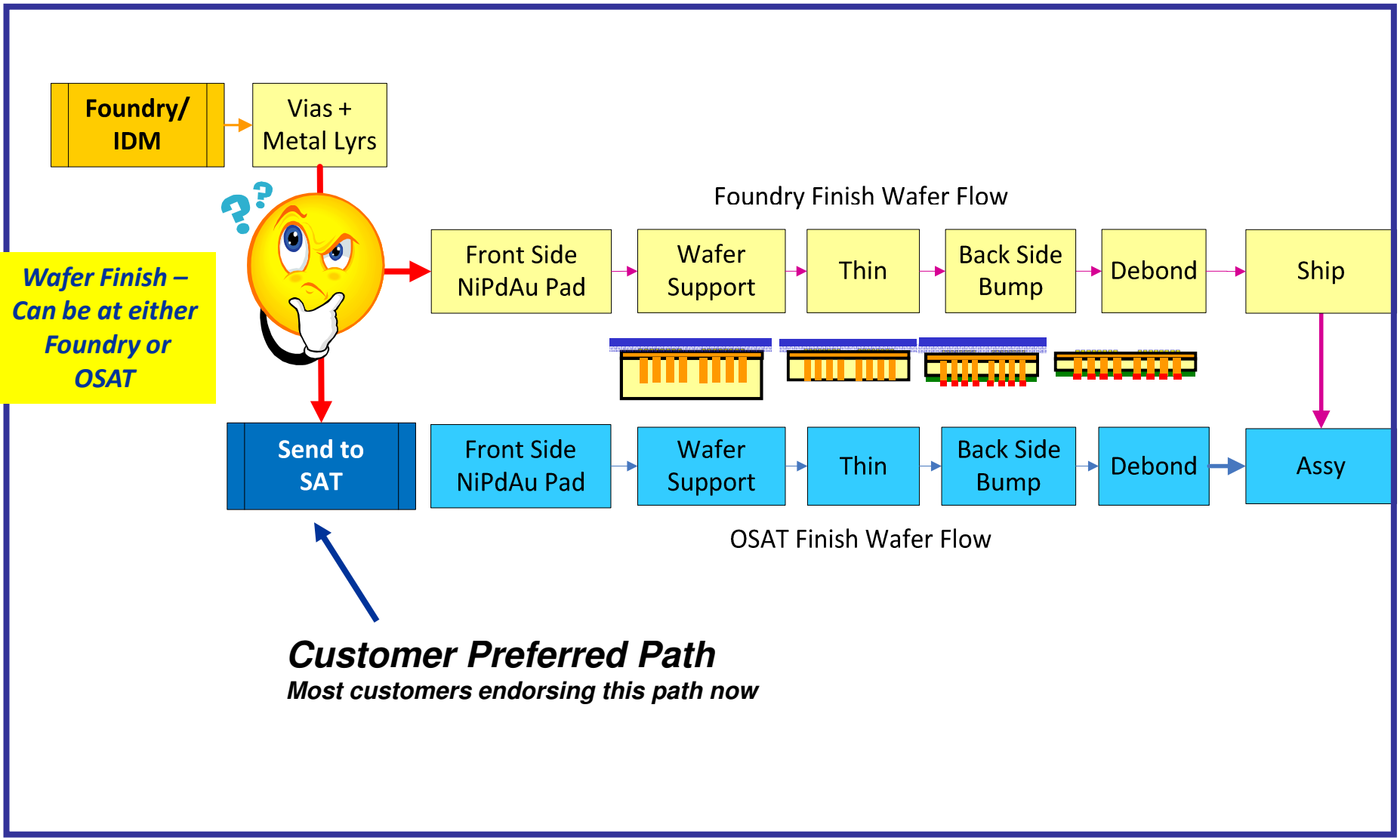
Silicon Interposer as Substrate

- **RF Module – Mobile Transceiver**
  - RDL at 20µm line/space
  - ~8µm dia. & 300µm deep TSV
  - Laminate could play …but via / pad?
  - Glass a better fit due to via size



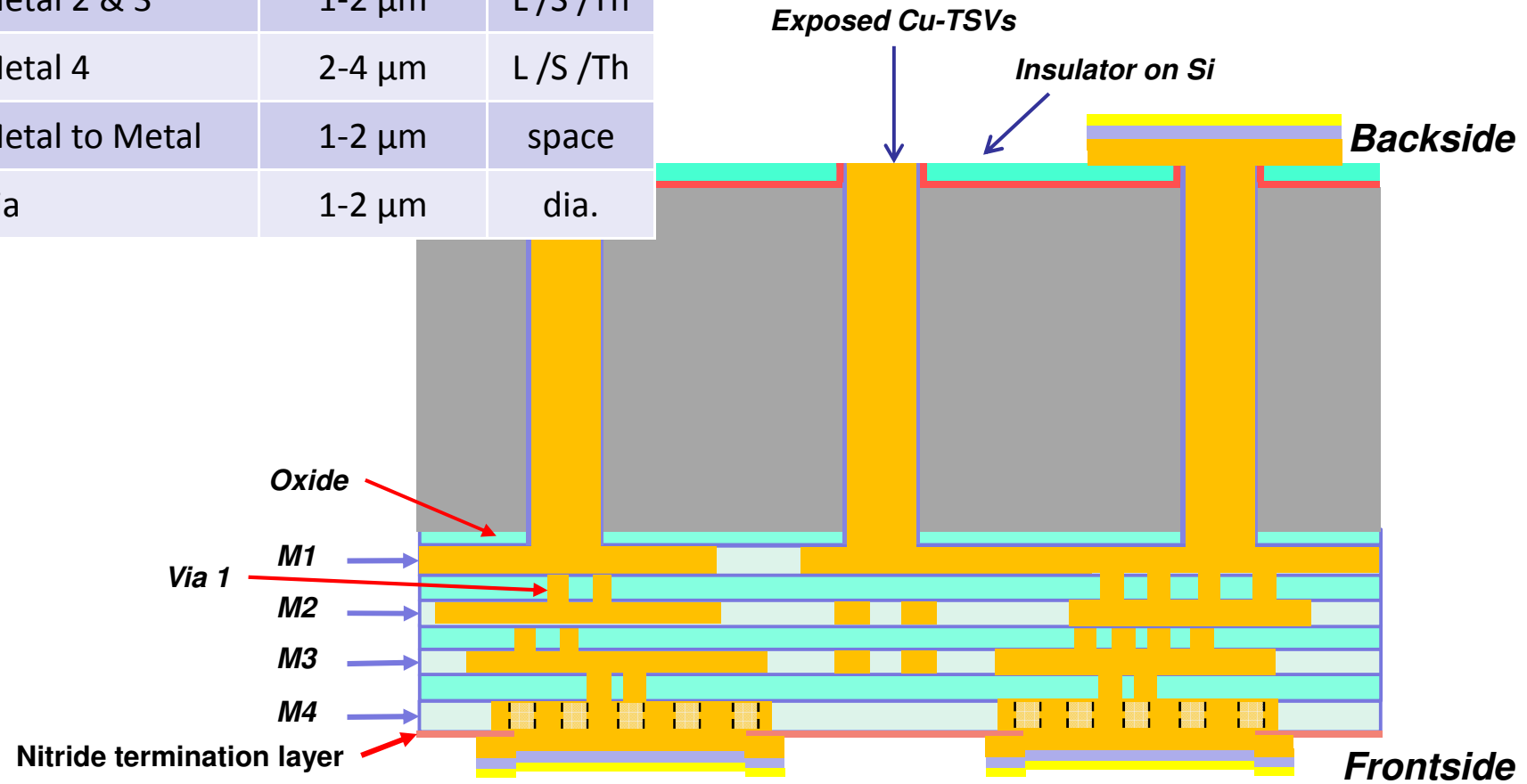


Interposer Supply Chain Issues – Silicon



Predominant Interposer Designs

Feature	Spec	Note
TSV dia./ depth	10/100 µm	finished
Metal 1	1 µm	L /S /Th
Metal 2 & 3	1-2 µm	L /S /Th
Metal 4	2-4 µm	L /S /Th
Metal to Metal	1-2 µm	space
Via	1-2 µm	dia.



Silicon Interposer Supply Chain

- **Sources**
  - Several foundry sources interested in manufacturing silicon interposers
  - A couple of sources already delivering fully functional wafers
- **Activity**
  - Significant activity underway
  - General target is 100µm as finished thickness with some backside RDL
  - Some with passive components on top side of interposer
  - Both heterogeneous and homogeneous die layouts
- **Challenges**
  - Design rules are aggressive < 2µm line/space with up to 5µm vias
  - Design rules fit low technology node BEOL silicon very well
  - Copper damascene (dual) & 300mm wafer requirement don't necessarily match up with idle capacity

Interposer Supply Chain Summary

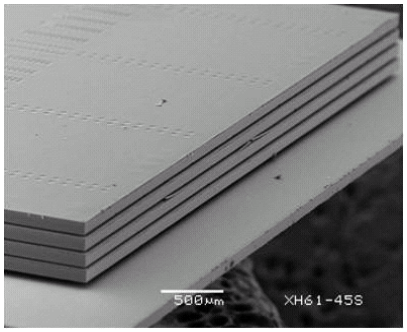
- **General**
  - Need to strengthen supply chain ; must entertain many alternative solutions
- **Laminate (Organic)**
  - Several companies reviewing cost add allowance & volumes to justify investment
  - Current limitations in via/pad design rules will limit market scope / application
- **Glass**
  - Panel size is best attribute ; LCD / flexible display in broad use
  - Via generation cost and plating distribution challenges will limit adoption
- **Silicon**
  - Foundries dominating supply chain, but only '3' real players today
  - Ultimately, cost needs to be in-line with market pricing to allow broad adoption

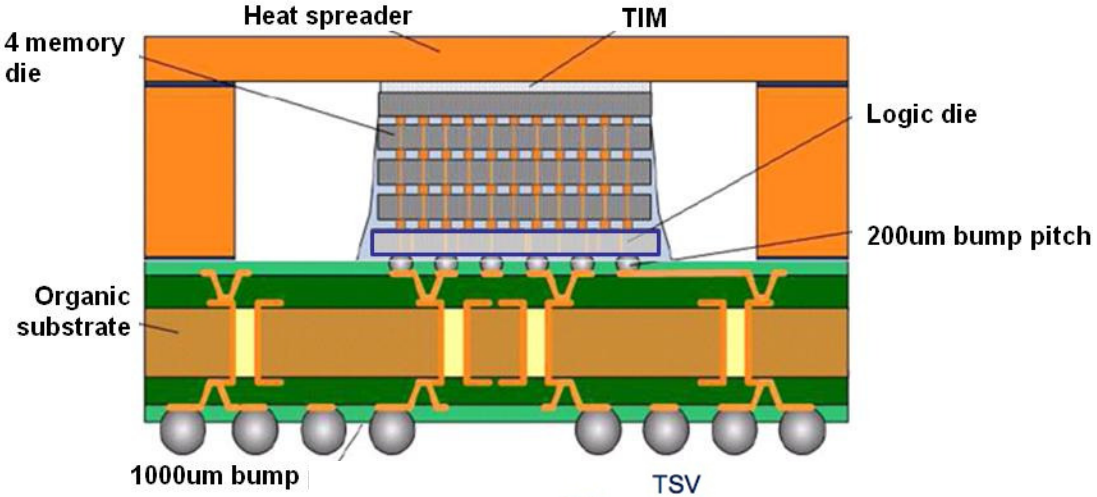
TSV Products Entering Market

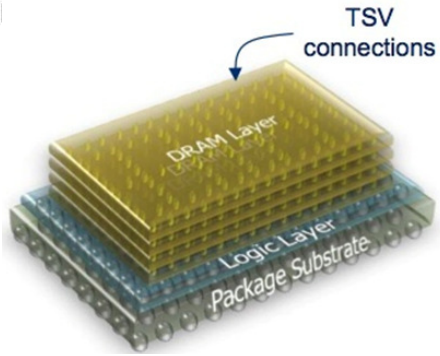
"Over Next Few Years"

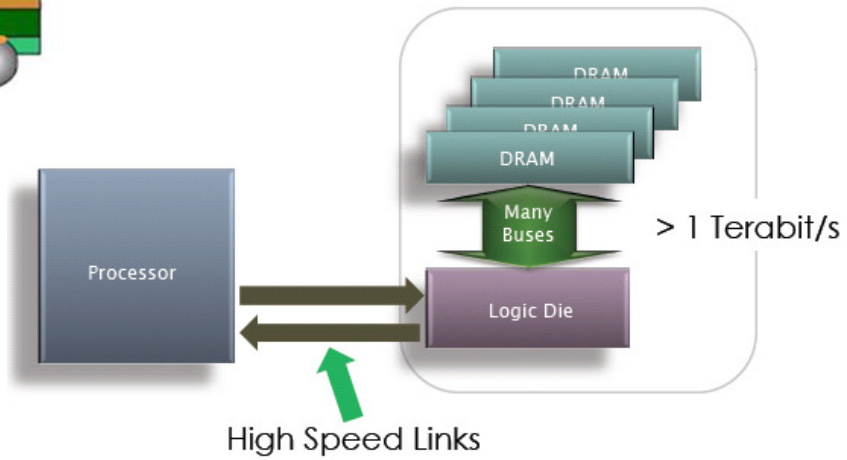
3D CSP Based Vertical Stacks

- **Memory**
  - Very high bandwidth at > 1 Tb/sec
  - Used for high performance server & super computer (HPC)
  - Eventually, Wide I/O DDR



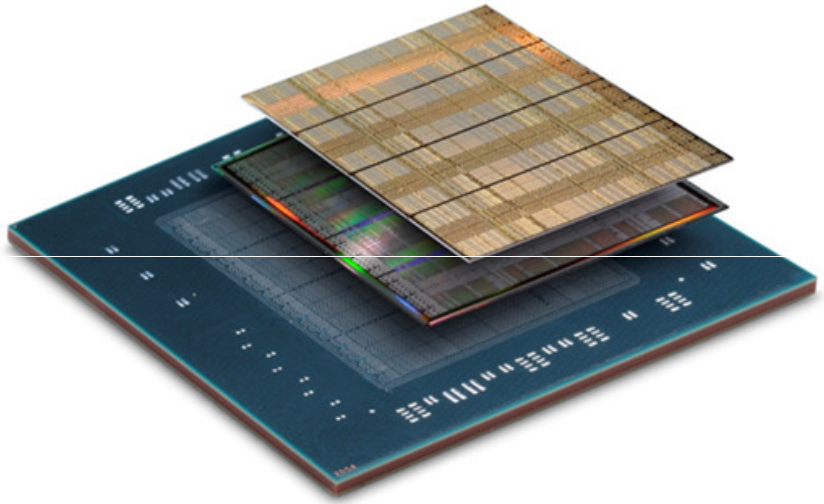






2.5D Silicon Interposer Based Product

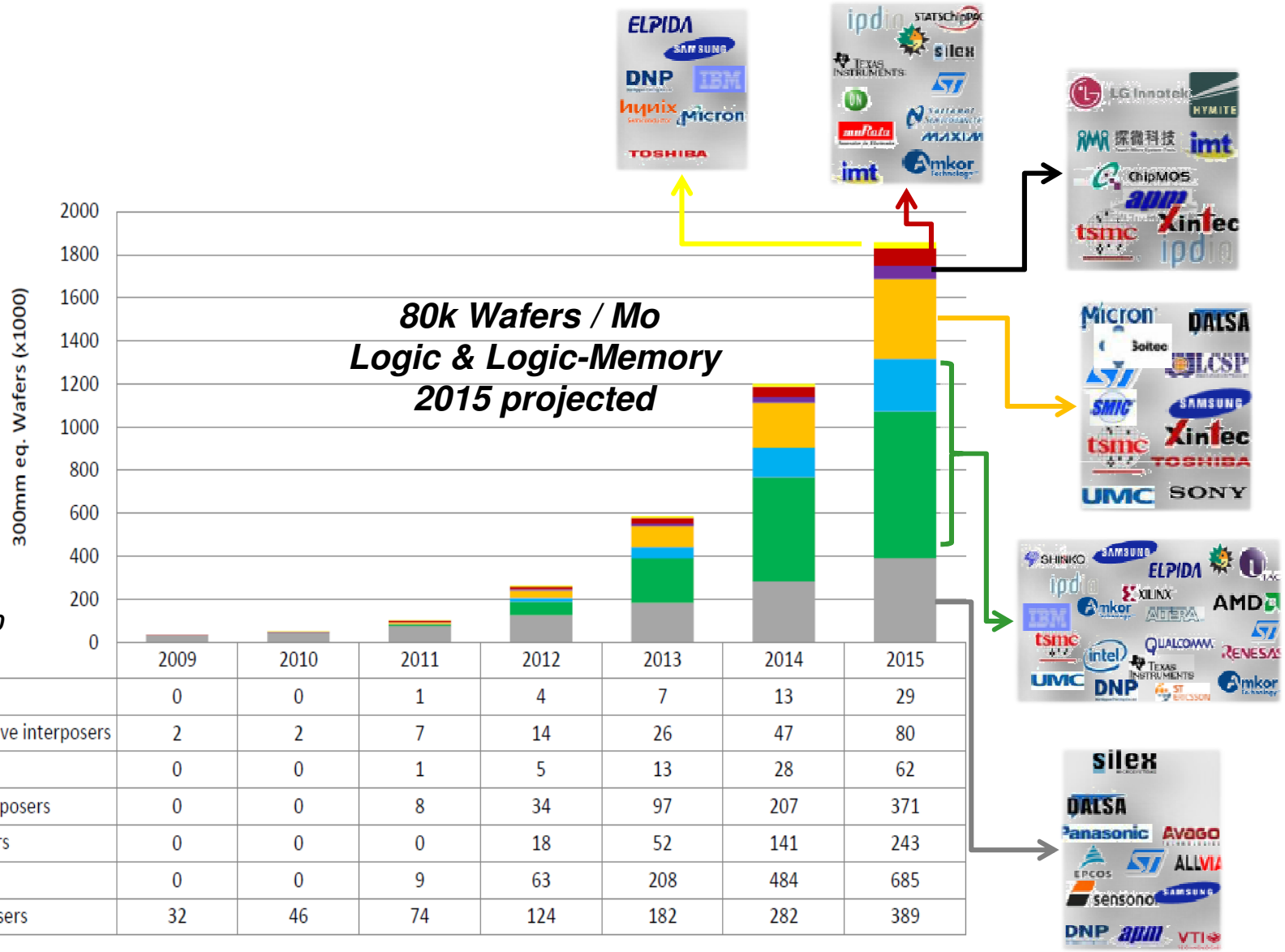
- **FPGA Package Build Structure**
  - ✓ Design increases logic capacity while reducing power
  - ✓ 100X improvement in inter-die bandwidth / watt
  - ✓ 50% power reduction from 40nm
  - ✓ 5x reduction in latency
  - ✓ 20x denser wire pitch
  - – FPGA ~ 8mm x 24mm
    - ▪ > 50,000 µbumps per die
    - ▪ > 200,000 total µbumps per package
  - – Interposer ~ 31mm x 25mm
    - ▪ ~20,000 C4 bumps per interposer
    - ▪ minimizes heat flux issues
  - – Substrate
    - ▪ 45mm body with ~ 2000 BGA balls



Ramping into production Today !!

Xilinx's Virtex-7® 2000T device showing from top to bottom the packaging substrate, the silicon interposer & 4 FPGA die (courtesy of Xilinx)

2.5D Interposer Wafer Forecast by Application

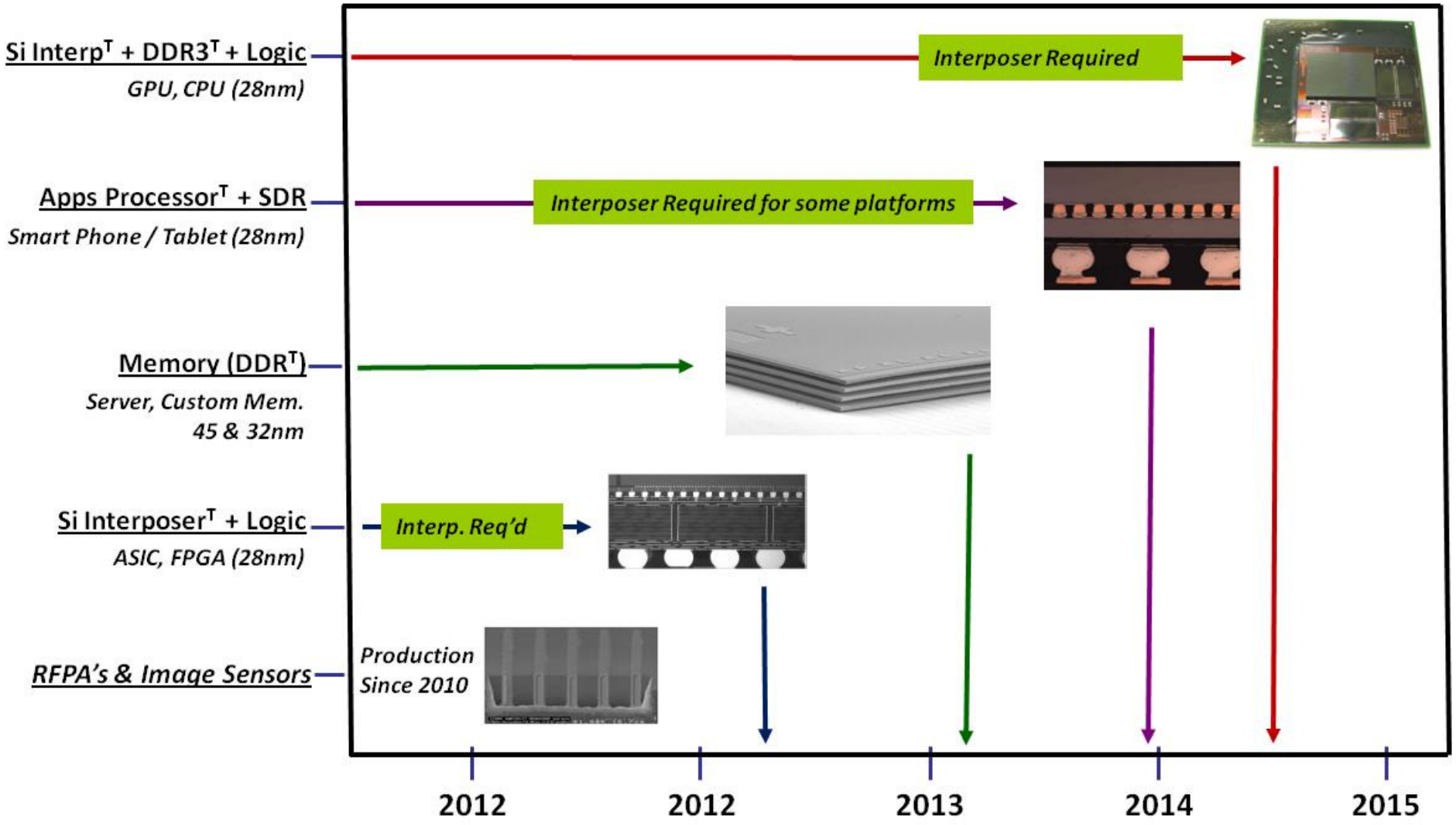


Source : Yole, 2010

	2009	2010	2011	2012	2013	2014	2015
memory only interposers	0	0	1	4	7	13	29
RF / Power / Analog passive interposers	2	2	7	14	26	47	80
HB-LED interposers	0	0	1	5	13	28	62
CMOS image sensor interposers	0	0	8	34	97	207	371
Logic+memory interposers	0	0	0	18	52	141	243
Logic-only interposers	0	0	9	63	208	484	685
MEMS & Sensors interposers	32	46	74	124	182	282	389

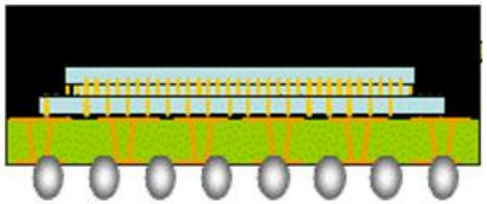
Expect compound annual growth > 80% over next 3 years through 2015 (300mm eq.)

TSV General Production Intercepts

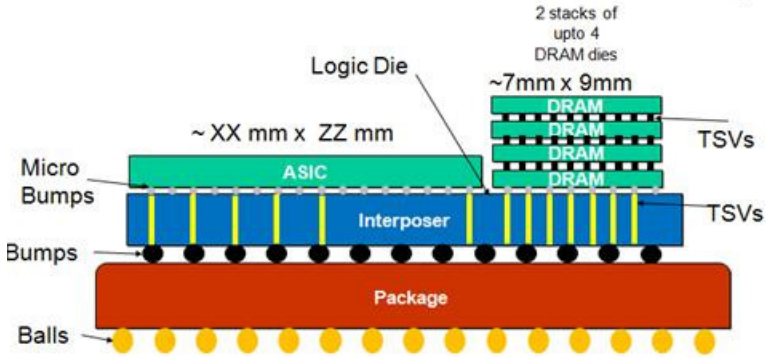


Die with TSV indicated by = T

Conclusion :TSV Product Future is 'Very Bright'



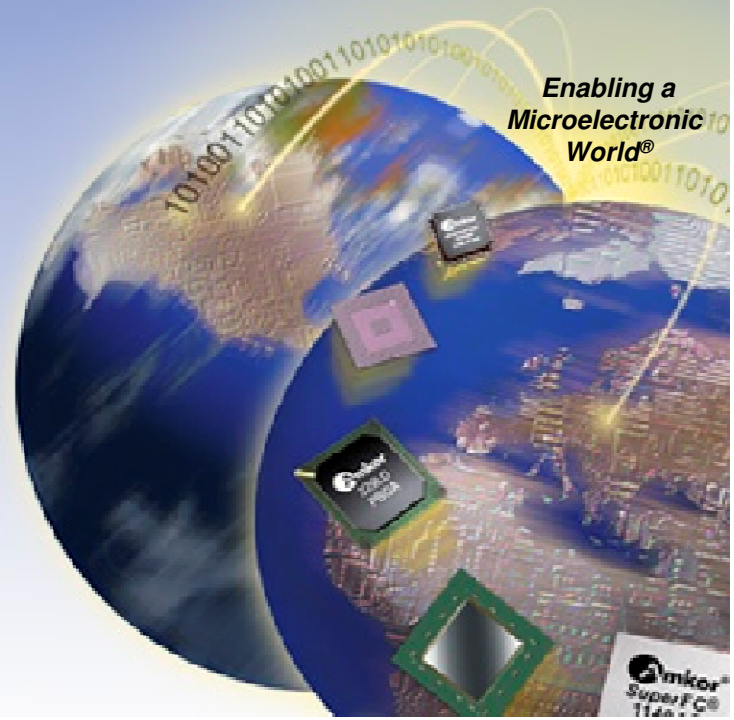
TSV Stacked CSP



TSV Stacked BGA

- Interest and activity accelerating
- 3D CSP Form Factor Improvement
- 2.5D Reduces Complexity
  - ✓ Reduces mask layer count of process node
  - ✓ Reduces advanced process node 'Time to Market'
  - ✓ Improves wafer yield
  - ✓ Reduces wafer start cost
- Both Improve Performance & Reduces Power Requirement

Thank You!



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