Temporary Wafer Bonding Materials and Processes

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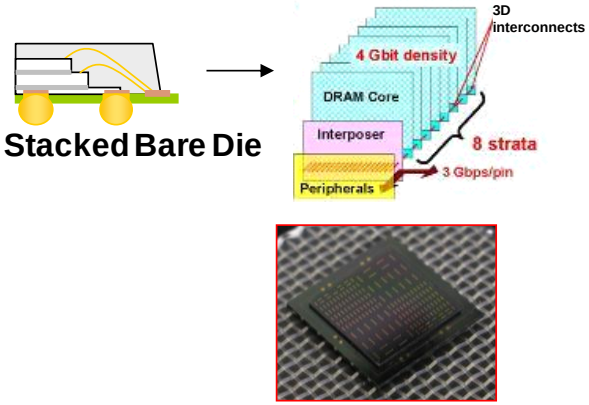
Outline

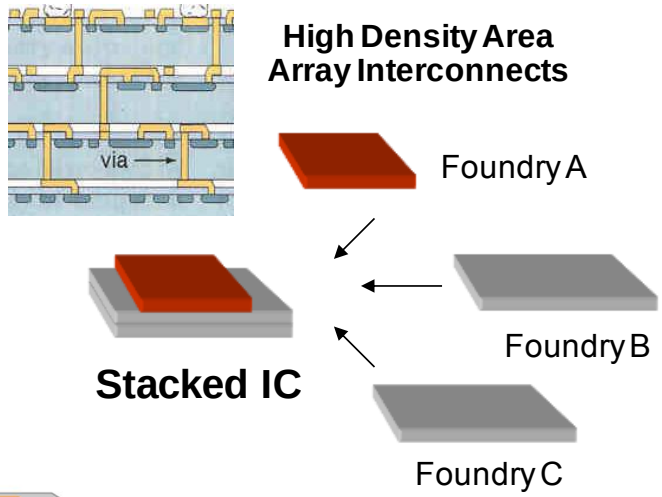
- Introduction:
  - 3D integration technology development at RTI
  - Temporary bond materials and methods
- Temporary bonding for 3D-IC applications
  - Process flow
  - Requirements of temporary bond materials
  - Results – process compatibility, dicing, and bond yield
- Temporary bonding for silicon interposer applications
  - Process flow
  - Requirements of temporary bond materials
  - Results – cure of spin on dielectrics, debonding

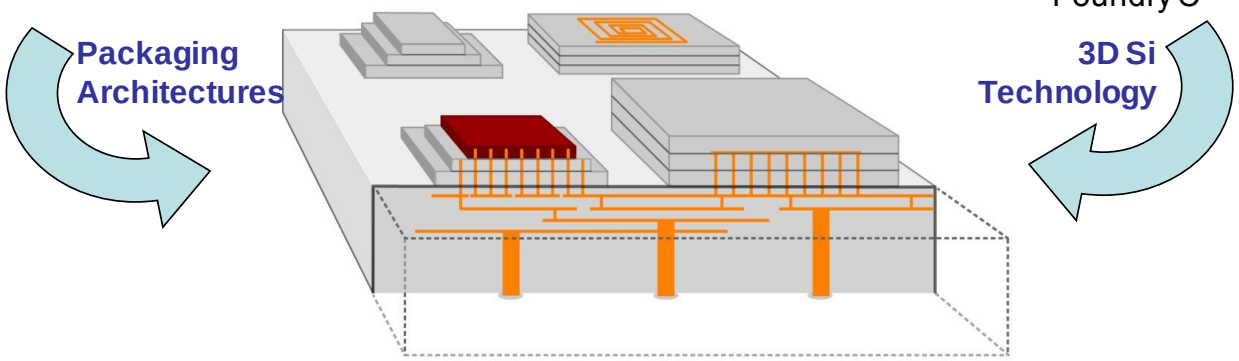
3-D Integration Technology Landscape

3-D Packaging



3-D IC





Silicon Interposer

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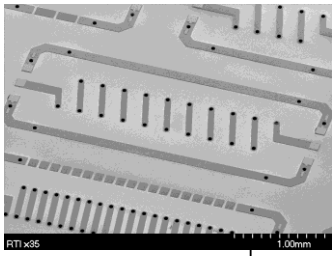
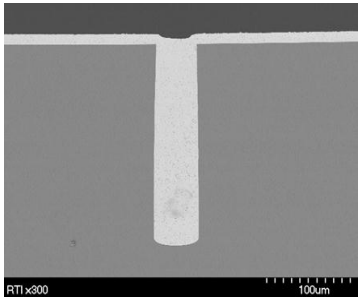
3D Integrated Electronics at RTI

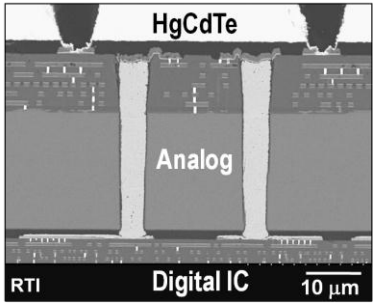
Integrated Passives

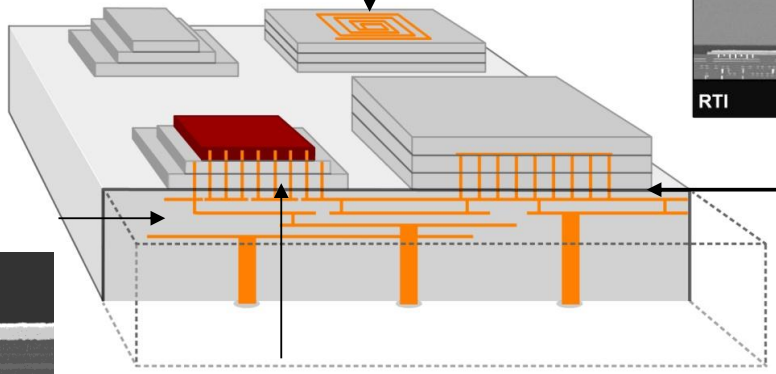


Through-Silicon Vias

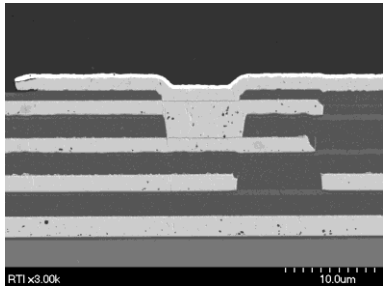


Heterogeneous Integration

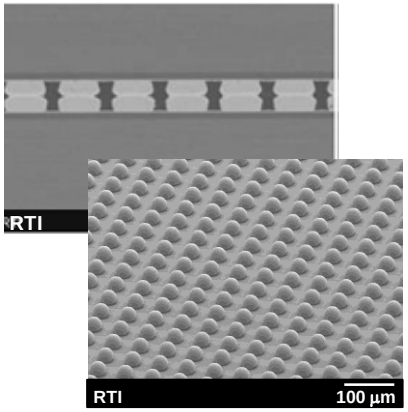




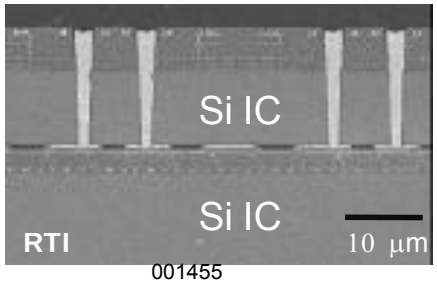
Silicon Carrier



Metal-Metal Bonding



High Density TSVs



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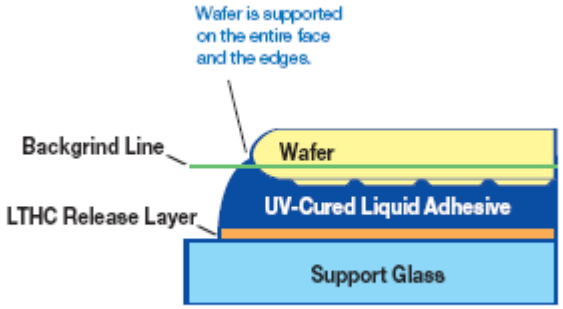
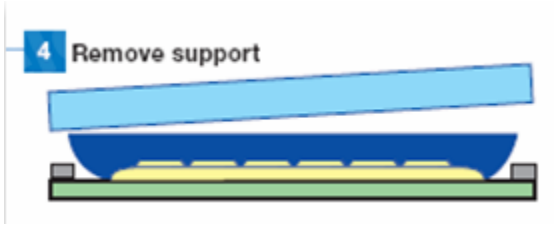
Temporary Wafer Bonding Materials

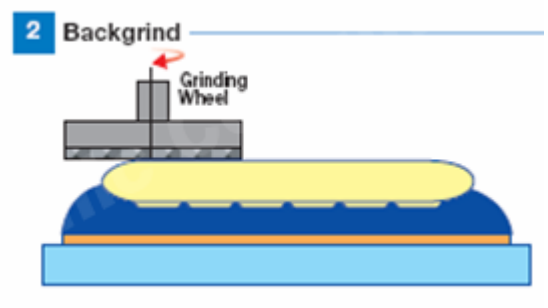
- 3D integration → increased demands on temporary bonds
- Thinning process is now just the beginning
- Materials suppliers have developed many different temporary wafer bonding solutions

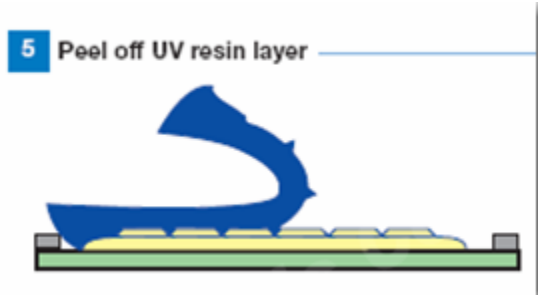
Company	Material	Bonding	Carrier	Debond	Debond Temp (˚C)	Equipment
3M	Acrylic adh	UV	glass	YAG laser	RT On flex frame	Suss, Tazmo
Brewer	thermoplastic	thermal	Si / glass	Thermal slide	180	EVG, Suss
Brewer (Zonebond®)	thermoplastic	thermal	Si / glass	solvent	RT	EVG, Suss
DuPont	PI	thermal	glass	Excimer laser	RT On flex frame	Suss
TMAT	Silicone elastomer	thermal	Si / glass	mechanical	RT On flex frame	Suss
TOK	NA	thermal	glass	solvent	RT	TOK

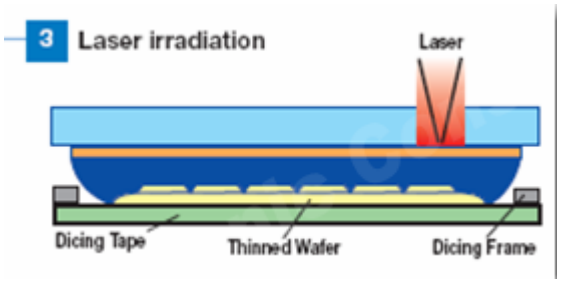
3M™ Wafer Support System









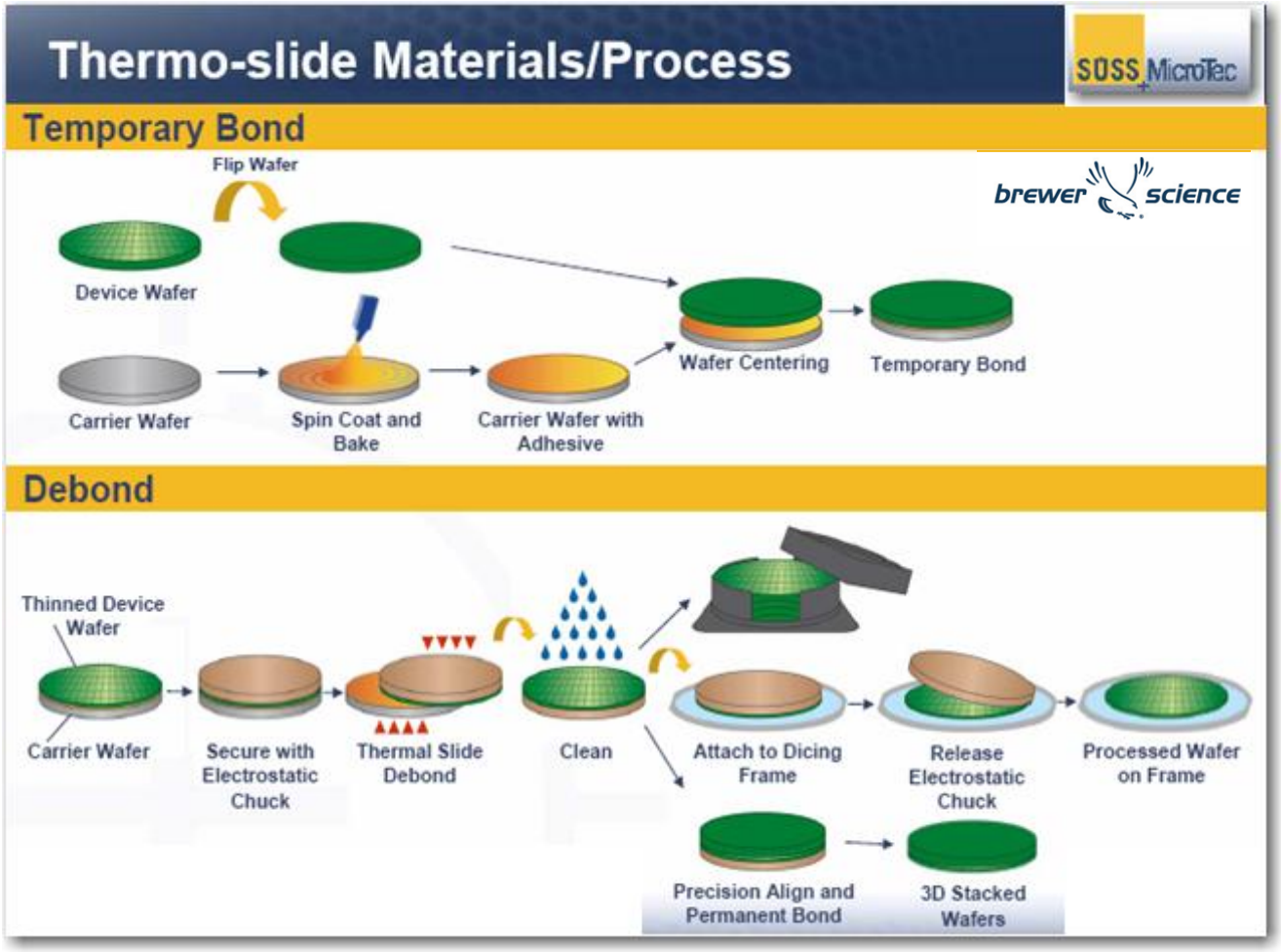


- LC3200 – Low Temperature
  - *60+ minutes @150C, Several minutes @ 180 °C*
- LC4200 – Intermediate temperature
  - *90 minutes @ 180 °C, Several minutes @ 200 °C*
  - *Low outgassing – back metal deposition, annealing*
- LC5200 – High temperature
  - *2 hours @ 200 °C, 1 hour @ 250 °C + Reflow Cycles at 260 °C*

001457

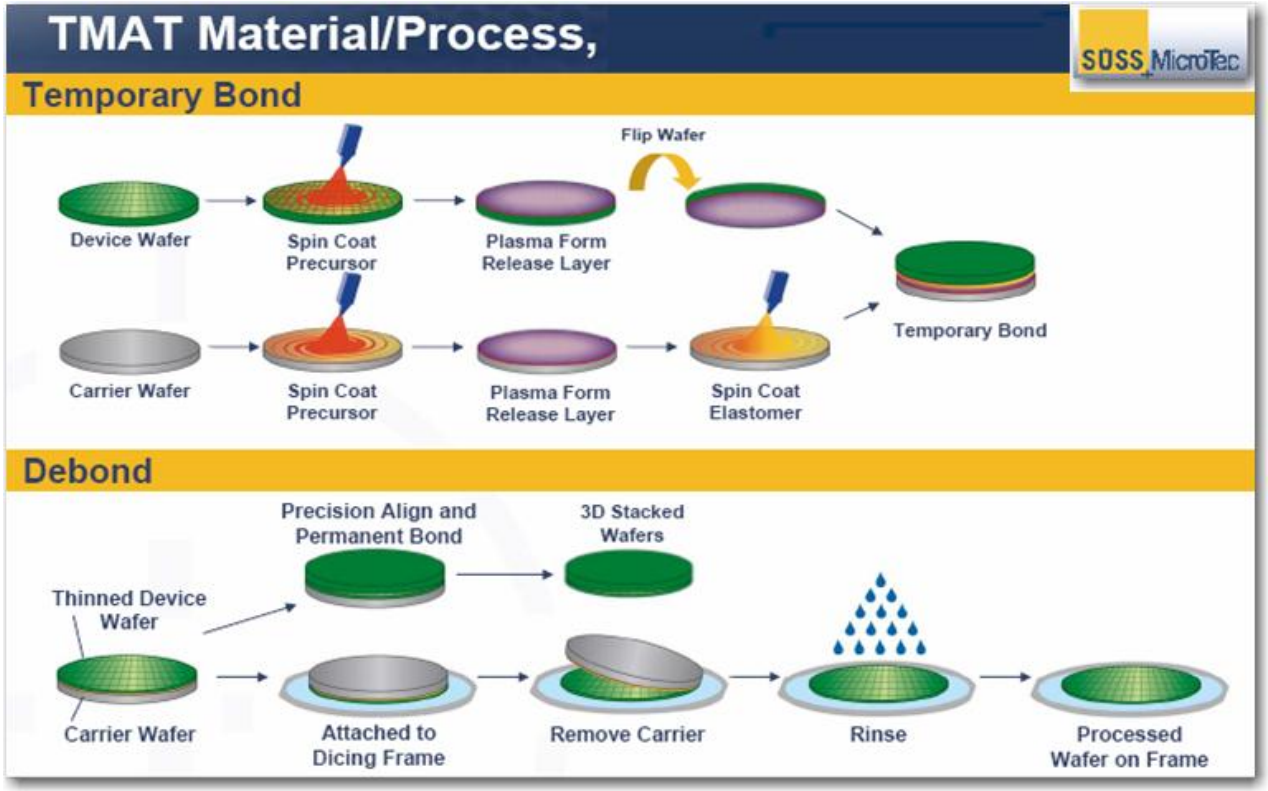
From: 3M Electronics Markets Materials Division

Brewer ZoneBOND™ and WaferBOND™



- WaferBOND has full adhesive coverage – slide off
- ZoneBOND has low tack zone in wafer center – solvent release

Thin Materials AG

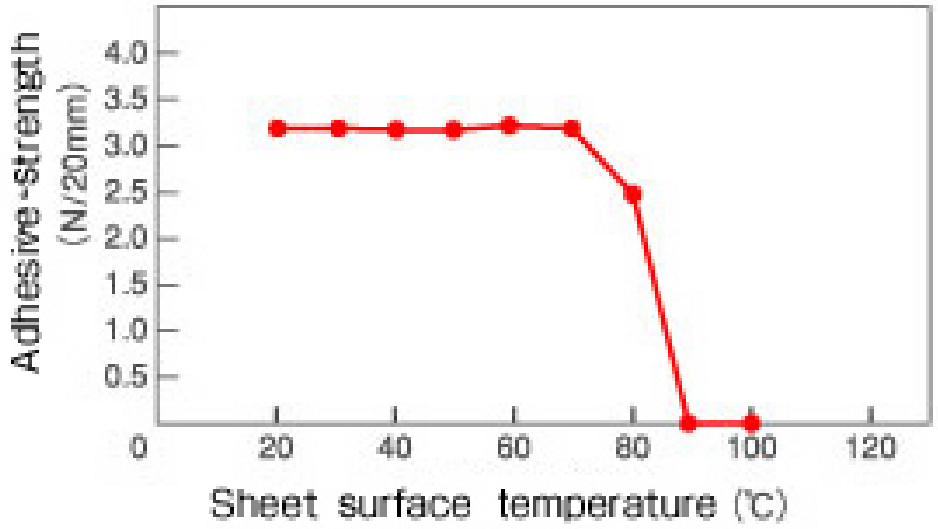


- The wafers are first coated with a thin (few hundred nm) proprietary release layer and subsequently bonded with silicone elastomer at 180° C.
- Wafer thinning down to 50 um and heat resistance above 250° C has been documented

From: Suss MicroTec and Thin Materials AG

Nitto Denko Revalpha

- Double sided tape with pressure sensitive adhesive and…
- **Thermal release adhesive** – abruptly loses adhesion at release temperature
- Many different adhesive strengths and release temperatures available
- Used in electronic component manufacturing



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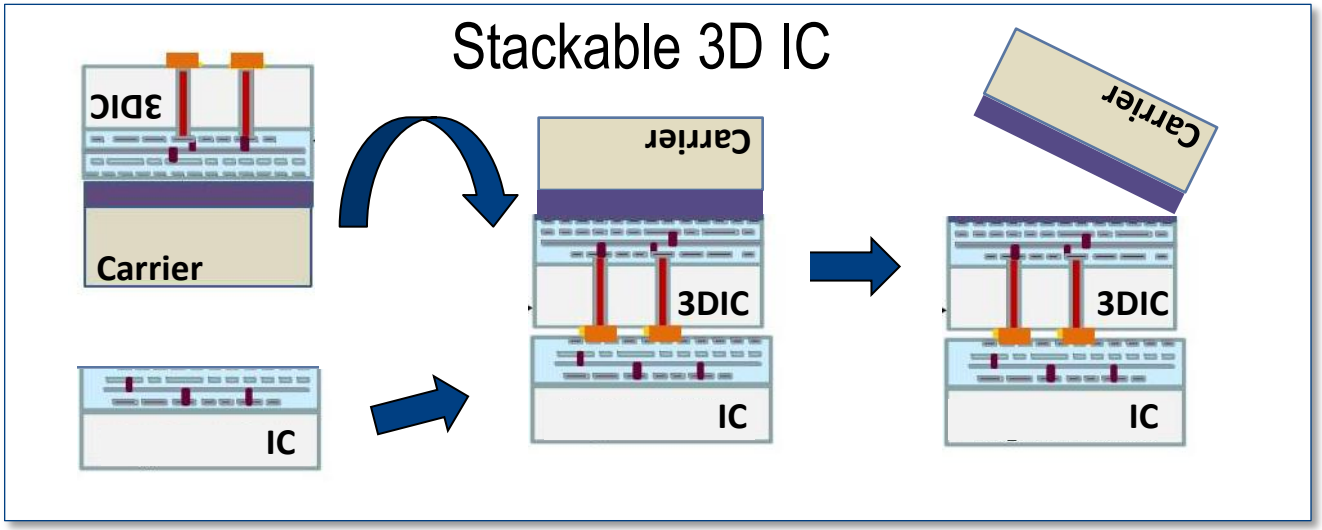
From: Nitto Denko

Temporary Bonding for 3D IC



Application

Face up, stackable 3D IC

- 15 um thin silicon
- 10 um pitch interconnects
- backside TSV reveal
- backside CuSn bumps

Requirements

Temporary bond must be compatible with:

- Thinning
- PECVD
- Lithography
- Electroplating

- Dicing on Carrier
- Cu/Sn bonding at 250C

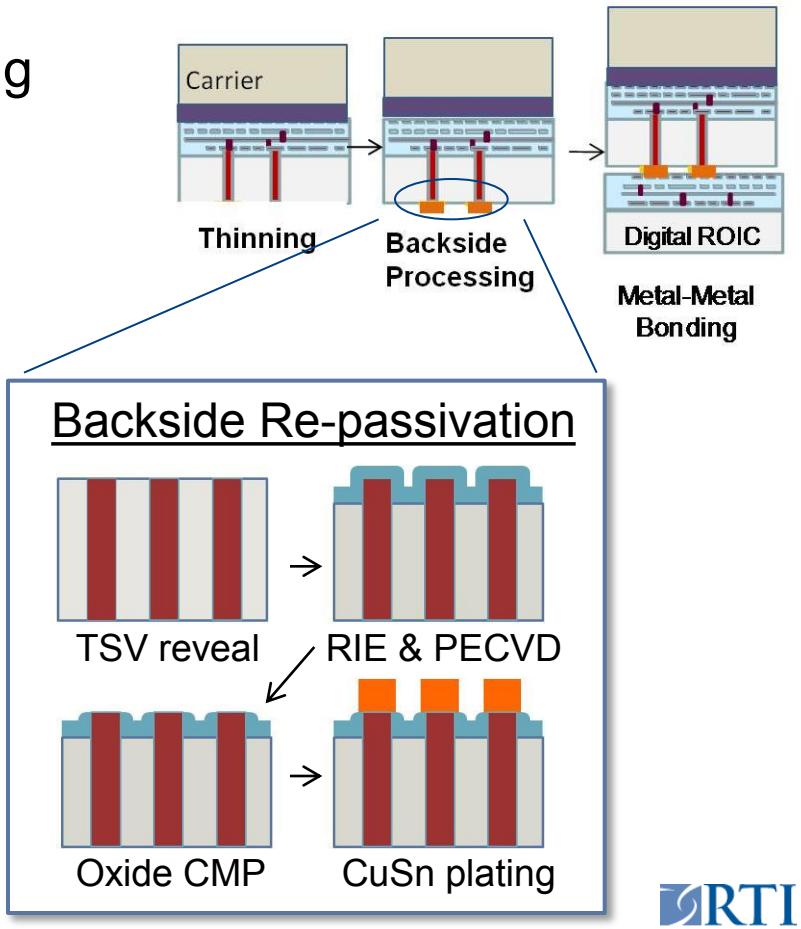
Process Flow – 3D IC

Temporary bond materials evaluated for the following process steps:

- Temporary wafer bonding and thinning
- Re-passivation
  - PECVD oxide at 150 C
  - Oxide CMP
- Formation of Cu/Sn interconnects
  - Lithography
  - Electroplating
  - Strip and seed etch
- Dicing on carrier
- CuSn bonding and de-mount

First lot → backside processing only

Second lot → full process w/ TSVs



Observed Process Compatibility

Temporary Bond	Temporary Bond Type	Thinning	PECVD Oxide	Litho-graphy	Electro-plating	Dicing on Carrier	Die Bonding & Release
Nitto Denko Revalpha	Thermal Release Tape	Good	Treatment Needed	Solvent susceptible	Good	Special conditions	< 200 C bonding only
Brewer Science WaferBOND	Thermo-plastic	Good	Flows at edge	Good	Good	Good	Flows during bonding
Thin Materials TMAT	Mechanical Release	Good	Good	Good	Good	Special conditions	Good

Criteria

- Thinning
  - TTV of materials
  - Cracks in thin wafer
- PECVD oxide deposition
  - Adhesion loss
- Lithographic processes
  - Loss in resolution
  - Chemical resistance
- Electroplating
  - Seed layer edge continuity
  - Compatibility w/ acid
- Dicing on carrier
  - Adhesion and chipping
- Die bonding
  - Bond yield
  - Carrier release

001463

Observed Process Compatibility

Temporary Bond	Temporary Bond Type	Thinning	PECVD Oxide	Litho-graphy	Electro-plating	Dicing on Carrier	Die Bonding & Release
Nitto Denko Revalpha	Thermal Release Tape	Good	Treatment Needed	Solvent susceptible	Good	Special conditions	< 200 C bonding only
Brewer Science WaferBOND	Thermo-plastic	Good	Flows at edge	Good	Good	Good	Flows during bonding
Thin Materials TMAT	Mechanical Release	Good	Good	Good	Good	Special conditions	Good

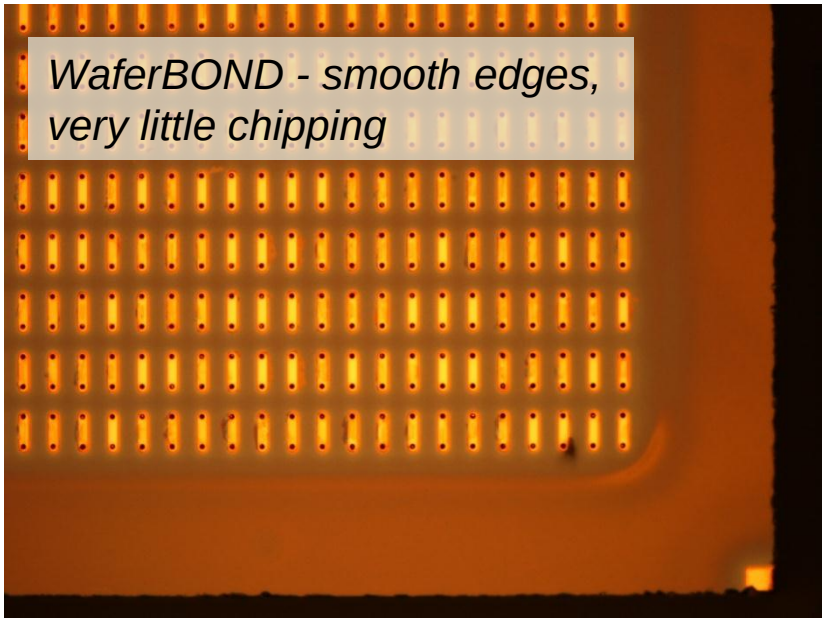
Evaluated in 2nd lot

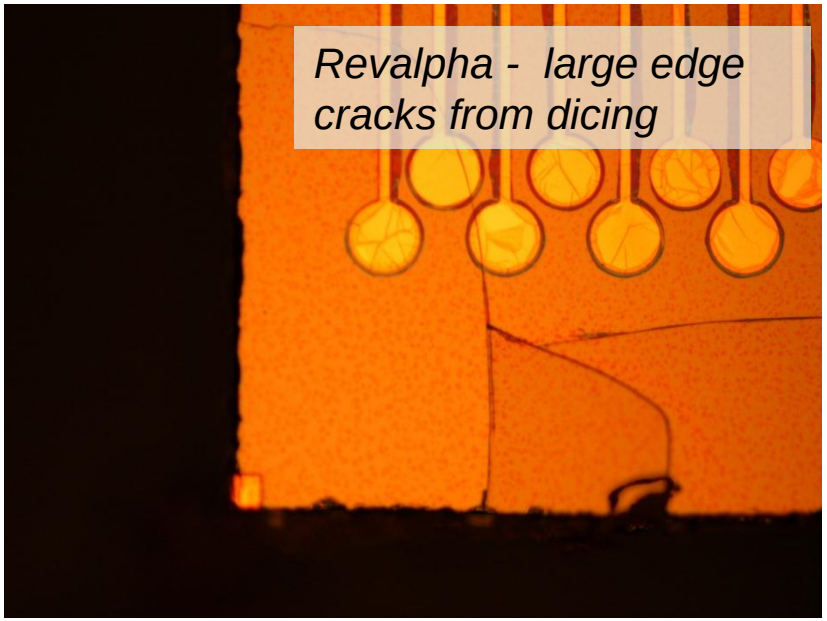
Criteria

- Thinning
  - TTV of materials
  - Cracks in thin wafer
- PECVD oxide deposition
  - Adhesion loss
- Lithographic processes
  - Loss in resolution
  - Chemical resistance
- Electroplating
  - Seed layer edge continuity
  - Compatibility w/ acid
- Dicing on carrier
  - Adhesion and chipping
- Die bonding
  - Bond yield
  - Carrier release

001464

Dicing on Carrier



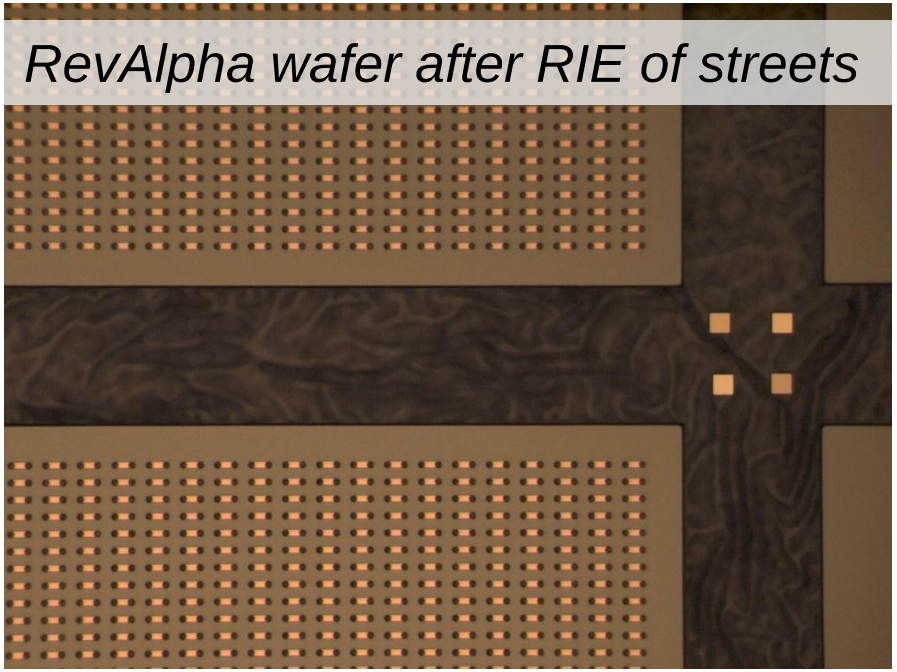


TMAT wafer delaminated during standard dicing (not shown)

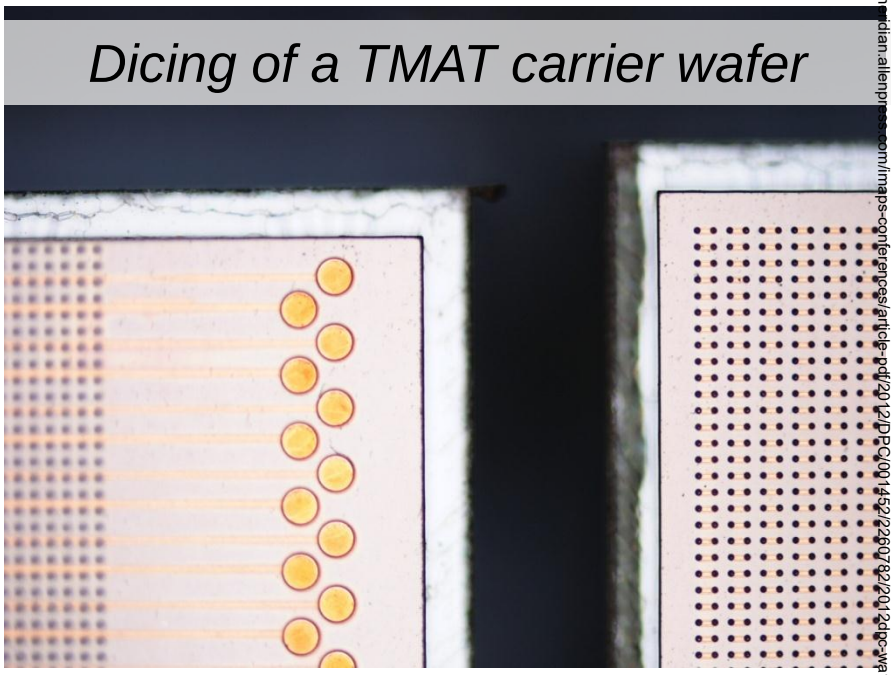
WaferBOND was compatible with standard dicing through thin Si and carrier

Dicing on Carrier

RevAlpha wafer after RIE of streets

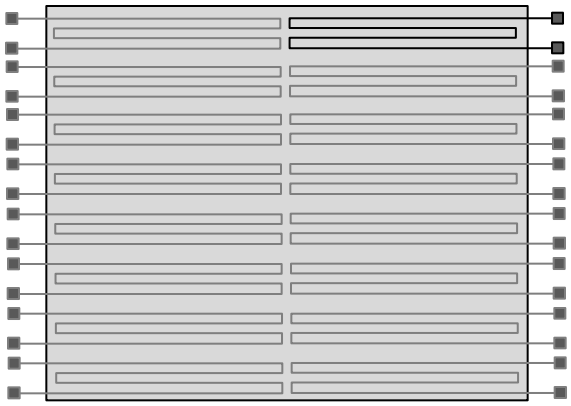


Dicing of a TMAT carrier wafer



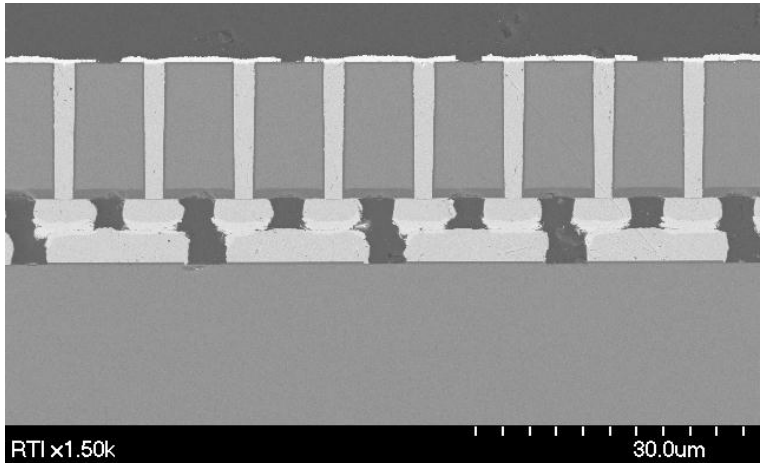
Edge cracking (RevAlpha) & delamination (TMAT) were eliminated by DRIE singulation of thin Si, then carrier wafer dicing

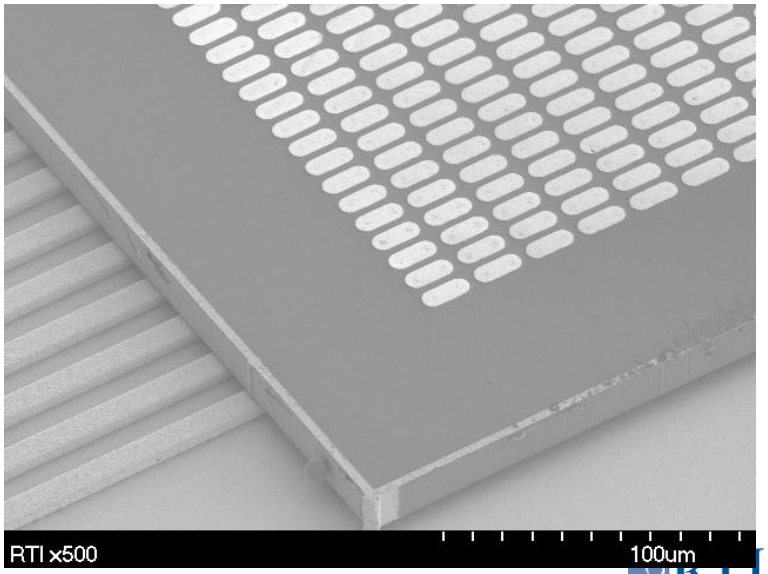
Bonding and Electrical Test



640x512 Cu/Sn - Cu microbump array

1272 bump bonds per channel





- After bonding and carrier release, 2-wire resistance measurements were made on all channels to check for:
  - Channel resistance
  - No. of channel opens
  - No. of shorts between rows
  - Extrapolated bond yield

Thin Die Bond Yield

Temp Bonding Material:	WaferBond 9001	TMAT
Cu/Sn - Cu Bond Conditions	250°C for 180sec	250°C for 180sec
# of Bonded Die Tested	8	9
Median Channel Resistance	596 - 721 Ω	603 - 652 Ω
# of Open Channels	0 - 5 (avg. = 2)	1 - 23 (avg. = 8)
# of Channels Containing Shorts (channel R < 550 Ω)	4 - 18 (avg. = 9)	7 - 59 (avg. = 19)
Channel Electrical Yield (%)	98.0 - 100 (avg. = 99.2)	91.0-99.6 (avg. = 96.9)
Extrapolated Bond Yield (%)	≥99.998	≥99.993

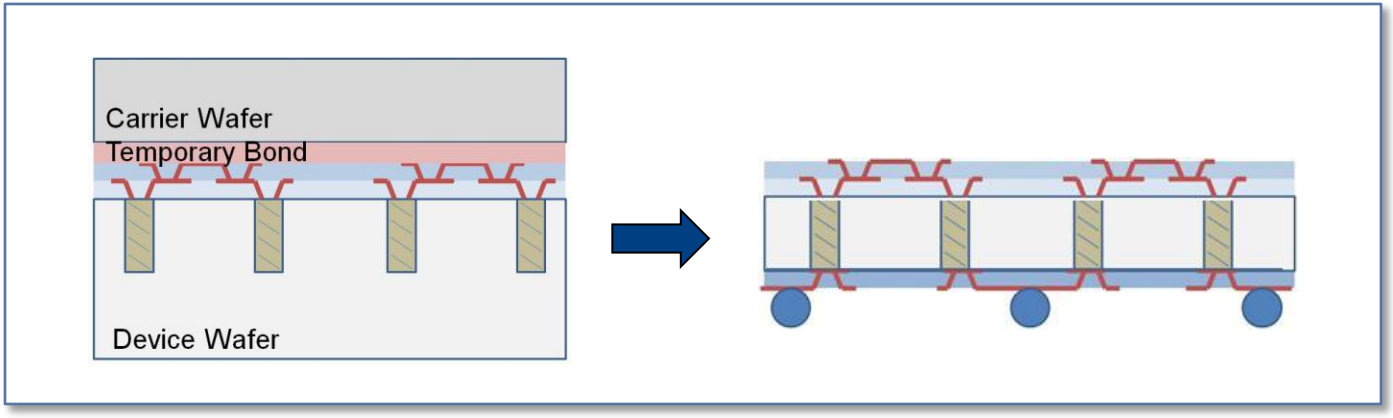
Both temporary bond materials resulted in excellent bond yield and clean release of the carrier die

- Similar to full thickness die bonding yield

Temporary Bonding for 3D IC - Conclusions

- Backside thin Si processing, oxide CMP, and singulation successfully demonstrated on three temporary carrier materials
- Die bonding & release successful on both WaferBOND and TMAT temporary bond materials
  - TMAT exhibits good resistance to all backside processes and good mechanical support during die bonding
    - Does not deform or flow during PECVD oxide deposition
    - Does not squeeze out during bonding (could work with pre-dispensed underfills)
    - Requires “dice-by-etch” of thin silicon
  - WaferBOND exhibited some flow in the edge bead during PECVD processing but good mechanical support and excellent die bonding results
    - PECVD oxide deposition caused WaferBOND to soften and flow at exposed wafer edge
    - Squeezes out during bonding (pre-dispensed underfills?)

Temporary Bonding for Silicon Interposer



Application

Thinned silicon interposer

- 50 - 200 um thin silicon
- 10 - 50 um Cu filled TSVs
- backside polymer dielectric
- backside solder bumps

Requirements

Temporary bond must be compatible with:

- Thinning
- PECVD
- Lithography
- Electroplating

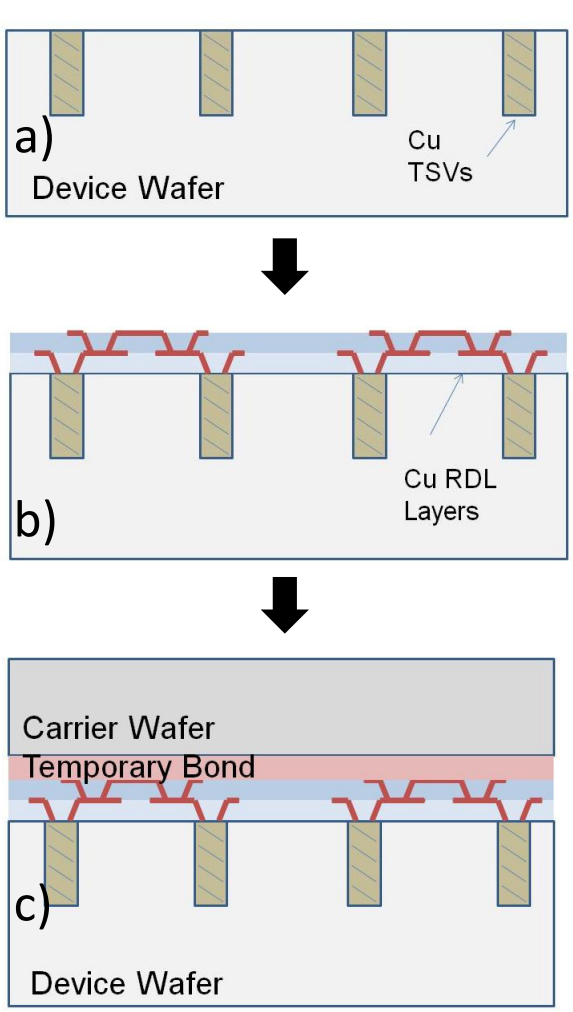
- Polymer cures at 190 – 250 C
- SnAg reflow at 250 C

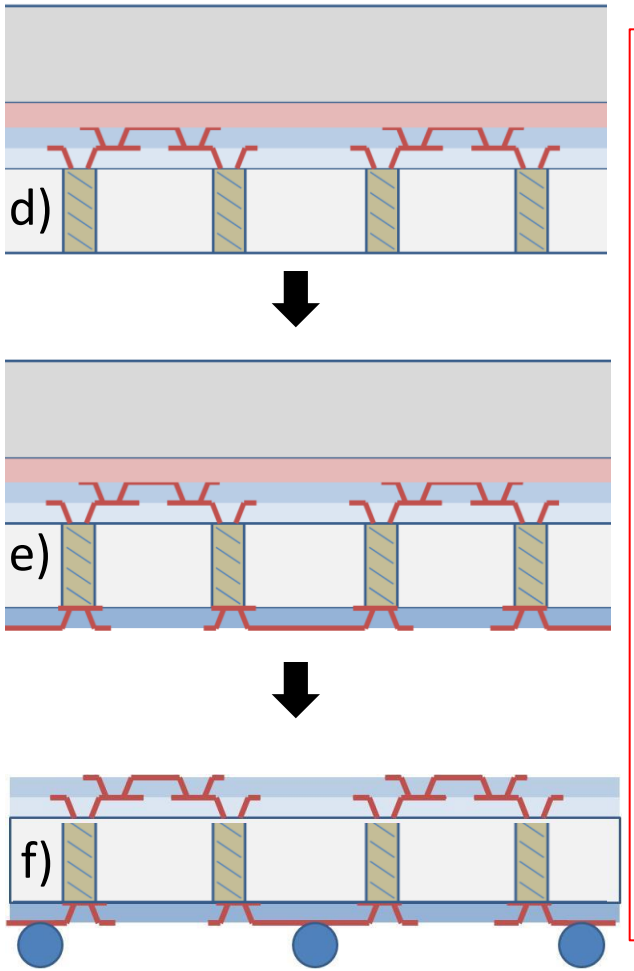
Process Flow – Silicon Interposer Test Vehicle

TSV etch and fill

Front side RDL

Temporary wafer bonding





Thinning and TSV reveal

Backside RDL (dielectric curing at 190 – 250 C)

Bumping, singulation, & bonding

On Carrier

001471

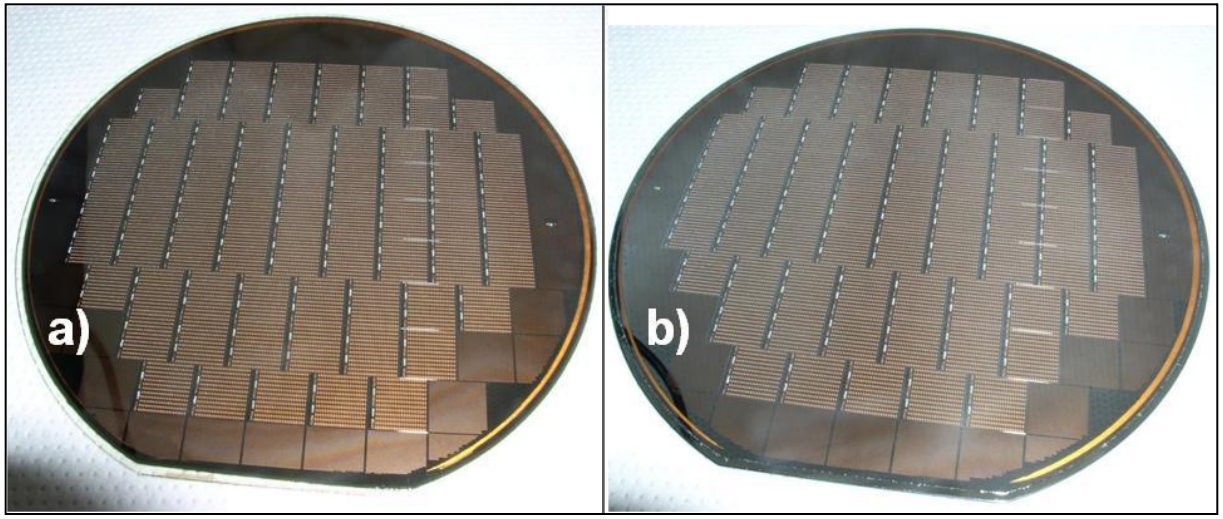
Backside RDL & Dielectric

- Three common spin-on dielectrics were imaged and cured on 100 μm thin silicon on 3M WSS and WaferBOND 9001
- Wafers were monitored for adhesion loss after cure

Wafers	Backside Passivation Material			Bond Pad	Carrier Removal
	ALX	PBO	BCB		
WB-1	X			Ball	Die
WB-2		X		Pad	Die
WB-3			X	Ball	Die
3M-1	X			Ball	Wafer
3M-2		X		Pad/Ball	Die
3M-3			X	Ball	Wafer

- Lot already in progress will examine integration of 25 x 100 μm and 50 x 200 μm vias with dielectric cures

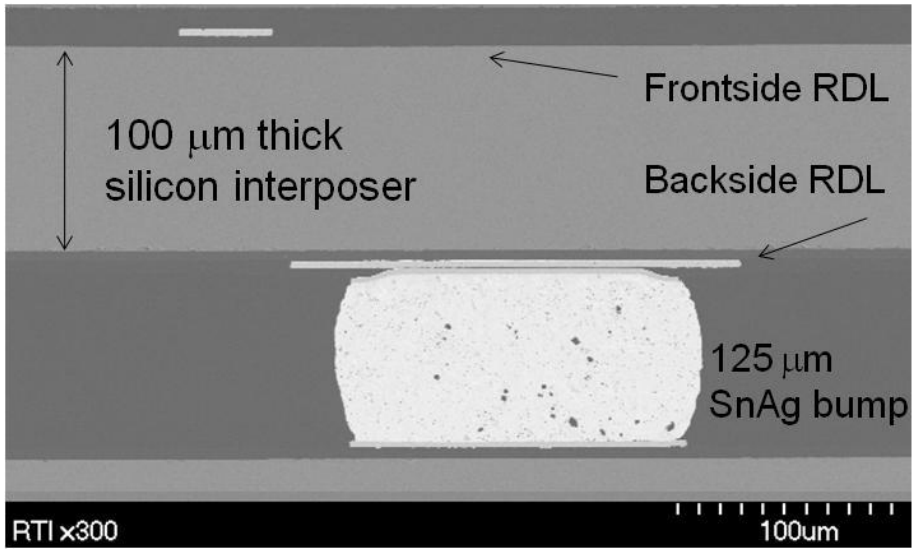
Backside RDL & Dielectric



100 μm thin silicon wafers after back side RDL processing on:
a) 3M WSS and
b) WaferBOND 9001

- No signs of adhesion loss were see on either temporary bond material after dielectric cures at 190 C, 200 C, and 250 C
- Both materials also exhibited good resistance to lithography, electroplating, and wet etching processes

Debonding

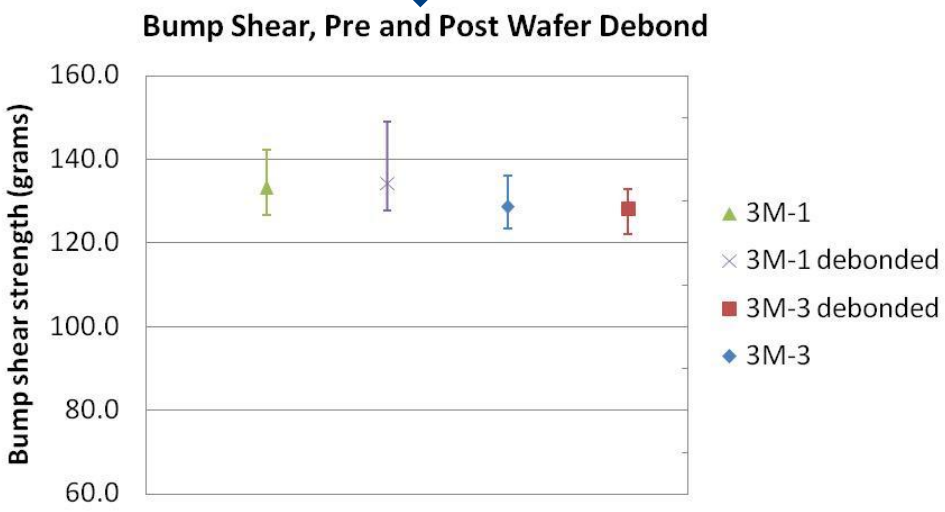


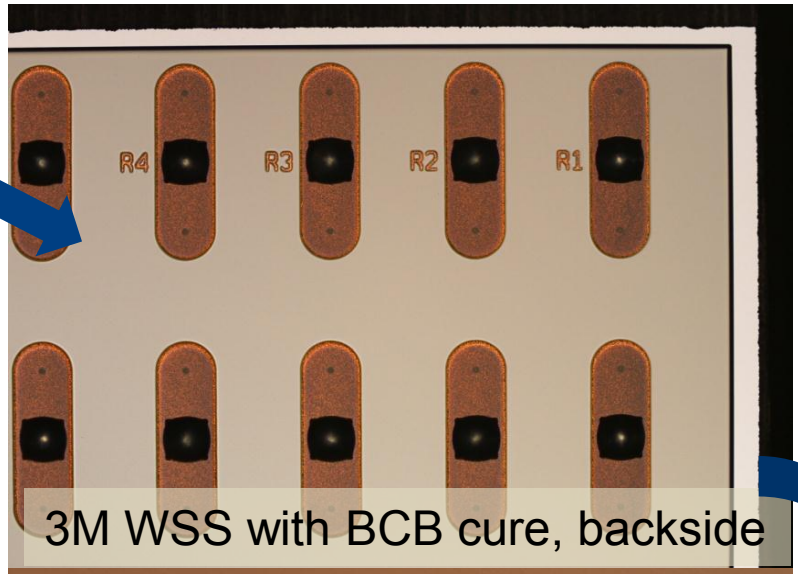
- Debonding of WaferBOND carriers done at die level
  - Reflow of bumps at 250 C
  - Removal of carrier at 180 C
- Debonding of 3M WSS carriers done at wafer level
  - 2nd carrier to protect bumps
  - Diced from backside

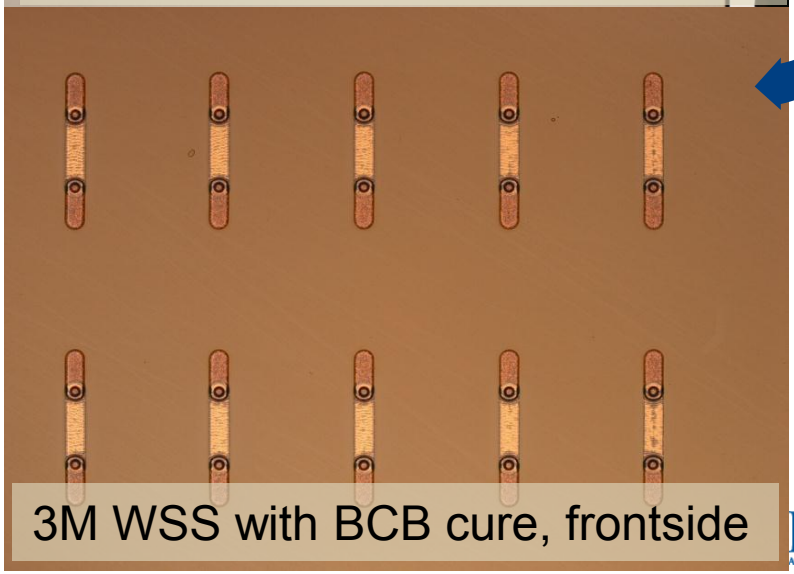
Debonding

No significant debond residue was observed on either bond technology with *any of the backside dielectrics*

No change in bump shear strength after 3M WSS debond process (WaferBOND not tested)







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Conclusions

- Temporary bond materials integrated into fabrication process for 3D-IC and interposer applications
- Demonstrated 15 μm thin 3D-IC test vehicle
  - 10 μm pitch area array of TSVs and Cu/Sn-Cu interconnects
  - Both temporary bonds > 99.99% yield of TSVs and interconnects
- Demonstrated 100 μm thin interposer test vehicle
  - Curing of common dielectrics on thinned wafers
  - 2nd lot with 25 x 100 μm Cu filled TSVs in progress
- Temporary bond materials have trade-offs in process compatibility, maximum temperature, ease of release, etc
- Application specific decisions on material type must be made