DfR Solutions

reliability designed, reliability delivered

Predicting Reliability of Zero-Level

Through Silicon Via (TSV)

Presented by Greg Caswell – DfR Solutions

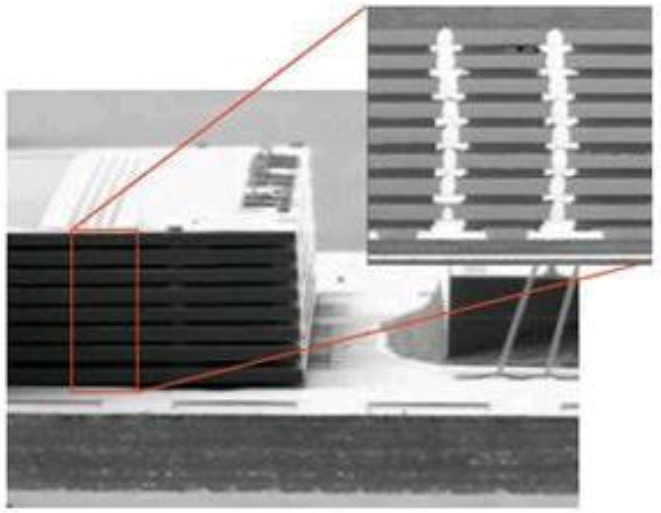
IMAPS Device Packaging Conference 2012

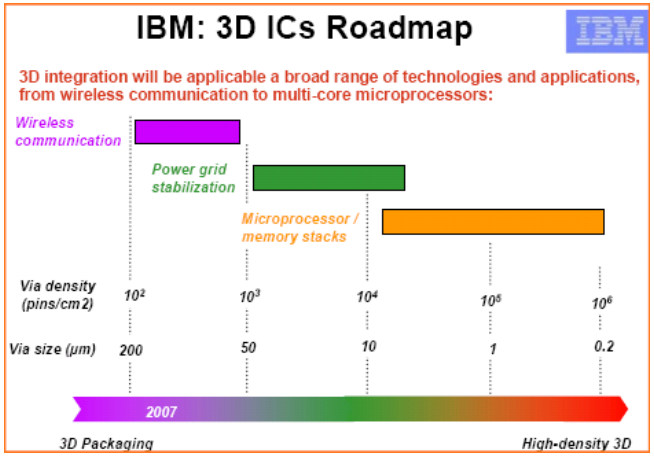
Through-Silicon-Vias

- Through Silicon Vias (TSV) are the next generation technology for system in package devices
  - Similar to plated through holes in a PCB
- Promised advantages include
  - Thinner packages
  - Greater level of integration between active die.
- Process still being optimized and cost must be reduced for widespread adoption.

TSVs (cont.)

- Concept mentioned in patent by Harris in 1995 (5682062)
- First patent mentioning TSV is with Micron in 2002 (6800930)
- Commercial launch is expected between 2010 and 2014
- Initial focus will be memory stacks and interposers





TSV (cont.)

- TSV is rarely justified by just miniaturization alone
  - More cost-effective to thin, stack and wire bond
  - Cost can be 2X-4X price of flip chip ($200/wafer is the goal) and 5X-10X the price of wire bonding

- TSV will be justified by performance
  - Increase in inter-die I/O
  - Increase in bandwidth
  - Decrease in interconnect length

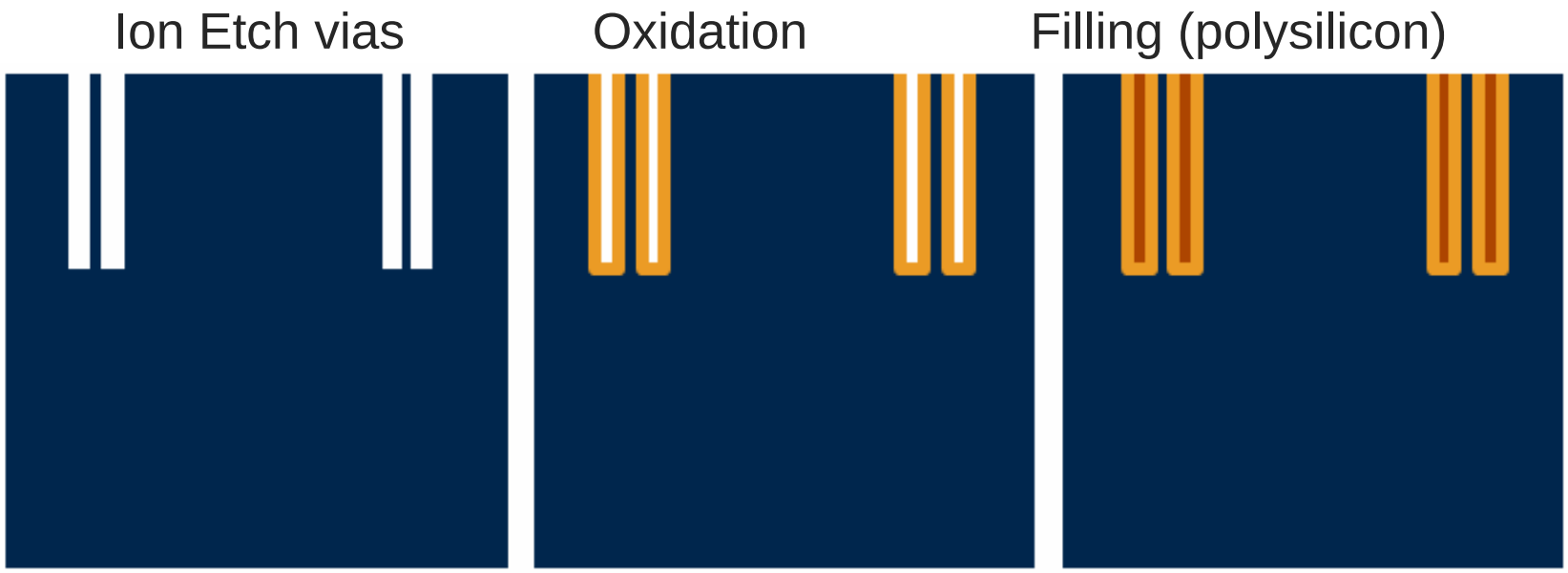
	On-Die	On-Package			Off-Pkg
		2D Planar MCP	Substrate Embedded Die MCP	3D Stacked Die MCP	
	CPU	CPU Memory	CPU Memory	Memory CPU	CPU Memory
I/O Speed		4–7Gb/s	4-10Gb/s	10+Gb/s	4Gb/s
# of Connections		200-400	400-10,000	10,000+	~4–6 channels DDR
Bandwidth		100-200 GB/s	200 GB/s – 1 TB/s	> 1 TB/s	< 100 GB/s
Capacity	< 50 MB	512+ MB	< 512 MB	< 512 MB	> 1 GB
Interconnect Length	< 1 mm	~7 mm	1-3 mm	1 mm	> 100 mm

http://www.intel.com/technology/itj/2007/v11i3/3-bandwidth/6-architectures.htm (August 22, 2007)

TSV Processes

- Via First, before Front End of Line (FEOL)
  - Vias etched in bare wafer prior to fab
  - Not likely
- Back End of Line (BEOL)
  - Via First, before BEOL
  - Via Last, after BEOL
- Vias can be created at various stages of the process
  - By the wafer provider, IC manufacturer, or packaging house

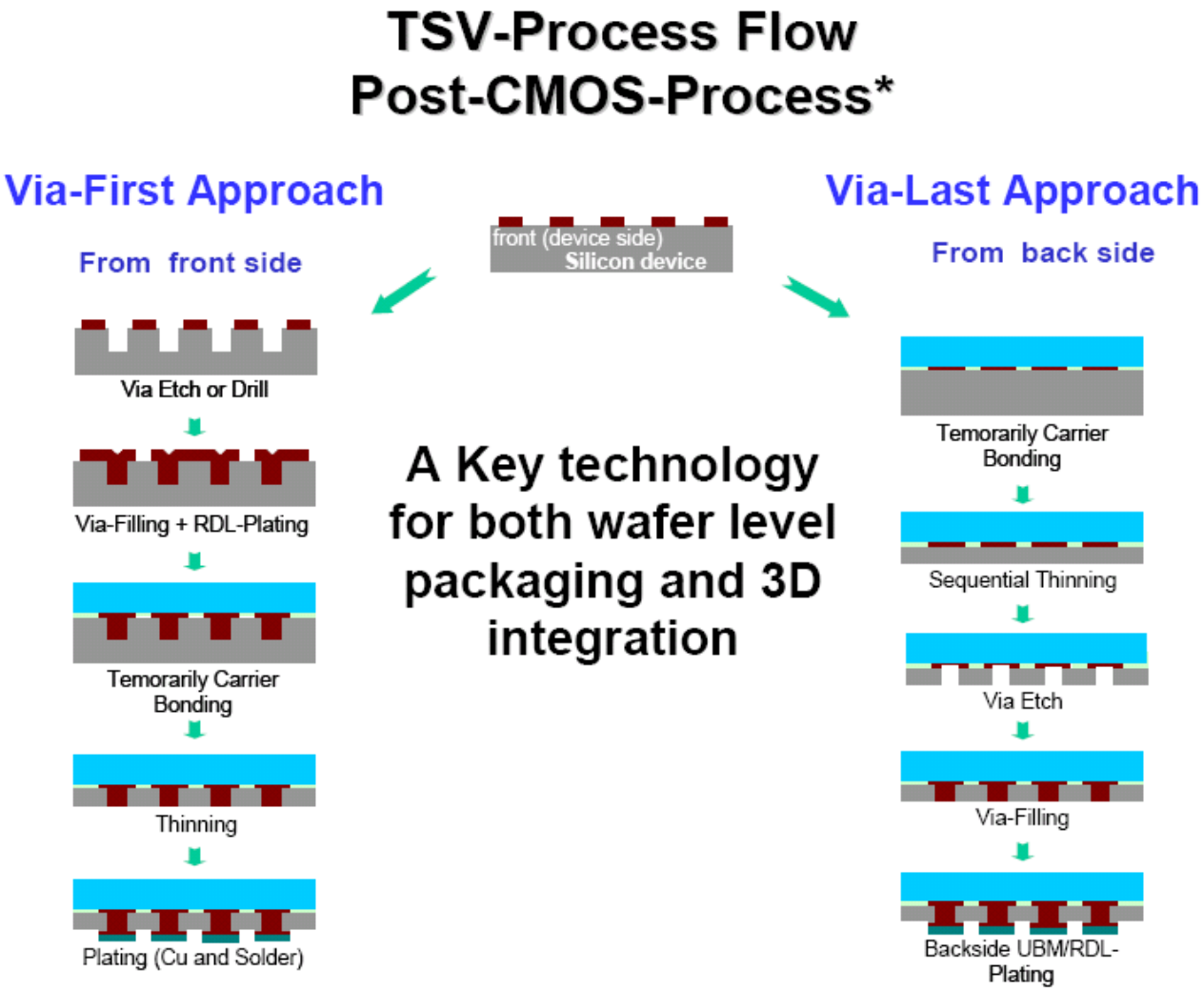
TSV Process (FEOL)



Polysilicon is used for conductor because it can survive high temp wafer processing (up to 1000C).

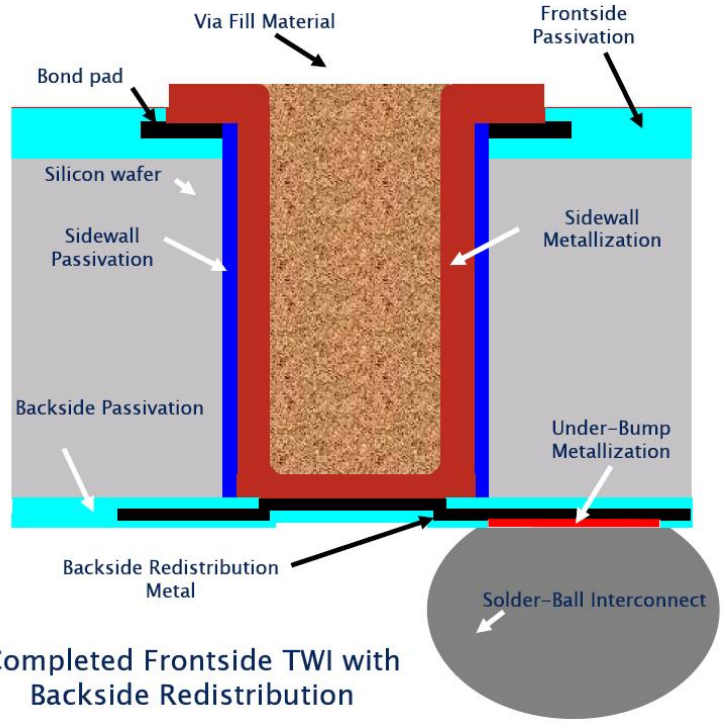
Easily integrated into the wafer process.

TSV Process – BEOL



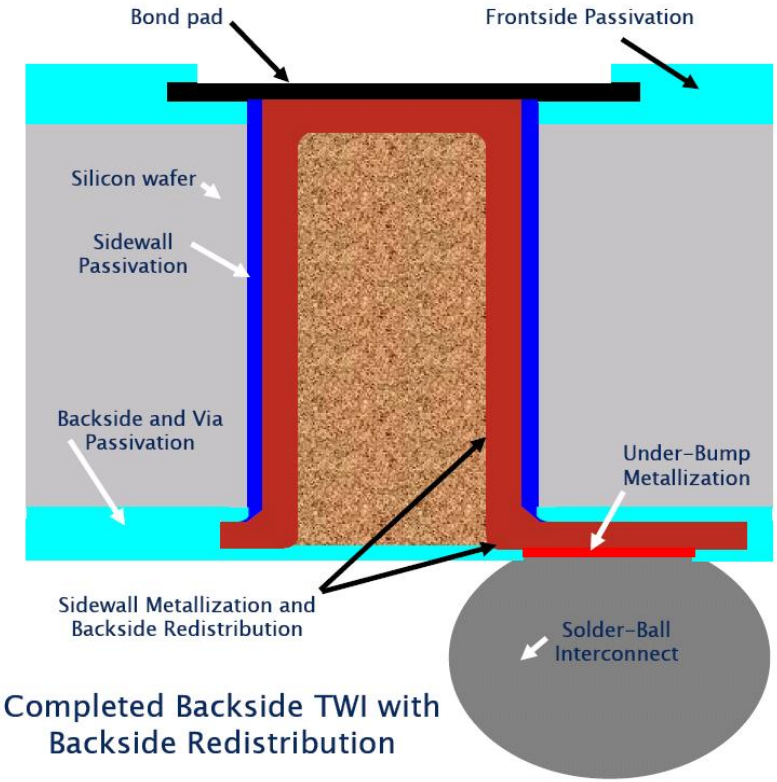
TSV – Via First, Before BEOL

Osmium™ Front side TWI Structure



Completed Frontside TWI with Backside Redistribution

Osmium™ Backside TWI Structure



Completed Backside TWI with Backside Redistribution

Via Formation

- Two main technologies for “drilling” TSVs
  - Dry etching or Bosch etching
  - Laser

Via Formation (Etching)

- Developed more than a decade ago for the MEMS industry
- Bosch process alternates between short isotropic SF6 plasma etches for the removal of silicon and short C4F8 plasma deposition steps for sidewall passivation
- Current etch rates are approximately 50 um/min
  - For next generation thinned die, this could allow via formation in under one minute.
- This technology is capable of creating very high aspect ratio vias with no limit on minimum diameter.

Via Formation – Laser drill

- Being maskless, the laser process eliminates PR coat, expose, develop and strip processing.

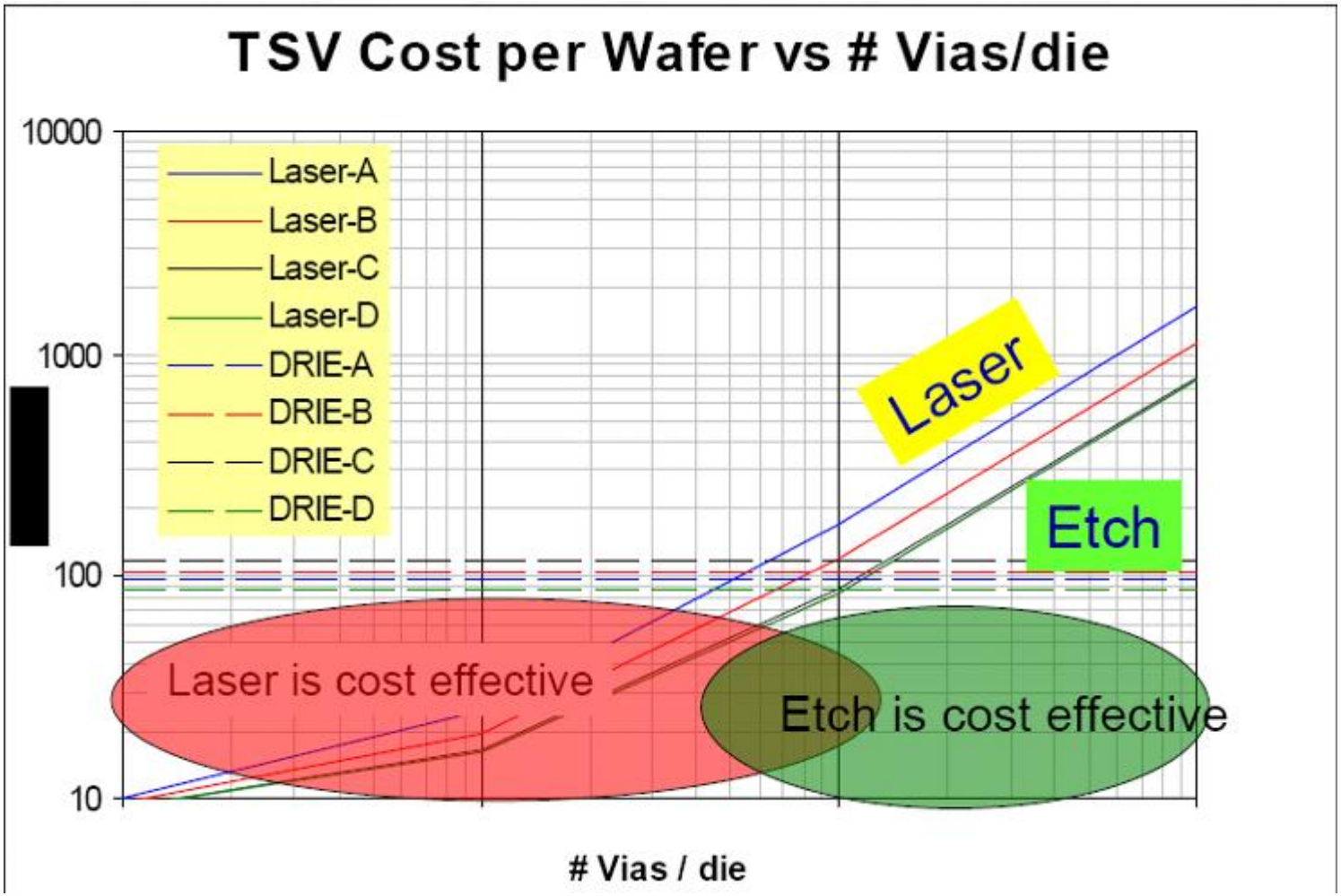
- The laser process produces sloped sidewalls which are more conducive to barrier and seed layer deposition and can "drill" through oxide and nitride layers as well as Al, Cu, Ni and Ti metallizations.

TSV Process (Drilling)

- Currently, laser drilling will likely dominate
  - Initial adoption technology will be memory stacks (see Micron-IBM press release) and interposers
  - Neither require large numbers (10K+) of small diameter connections.
  - Under this configuration, laser drilling is more cost effective and easier to implement

- CPUs will likely not utilize TSV until 10K+ connections can be made between die.
  - At which point reactive etching may become the technology of choice.

TSV Drilling Cost



TSV Process – Insulating

- After via formation, oxide (SiO2) insulation layers are typically deposited by CVD using silane (SiH4) or TEOS.
  - If the TSVs are being insulated and filled after chip fabrication, care has to be taken with the deposition temperature.
  - Typical TEOS deposition processes are in the 275-350°C range.

- To reduce the deposition temp, one option is the use of Parylene precursor, which can be deposited at room temperature, as a conformal organic insulator for TSVs.

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TSV Process – Filling

- The final step is the filling of the via
  - It is important to know what aspect ratios will be required for various via diameters both in terms of creating the vias and filling them.

- Most cost of ownership (CoO) models show that via formation and via filling are the major cost barriers for 3-D, but this depends on size, pitch and aspect ratio.

How Can Through Silicon Vias (TSV) Fail?

- Three primary failure mechanisms
  - Cracking of the Copper Plating
  - Cracking of the Silicon /Change in Resistance of Silicon
  - Interfacial Delamination of Via Wall from Silicon

- Challenges
  - The exact process and architecture (materials, design) for TSV has yet to be finalized
  - Can lead to large changes in stress state

TSV Design

- Via walls can be straight (etch) or tapered (laser)

- Vias can be filled (likely) or not filled (aka, annular)

TSV Design

- Depending on Via First or Via Last design layout, TSV can have a 'floor' of copper
  - Also known as Carpeted or Nailheading

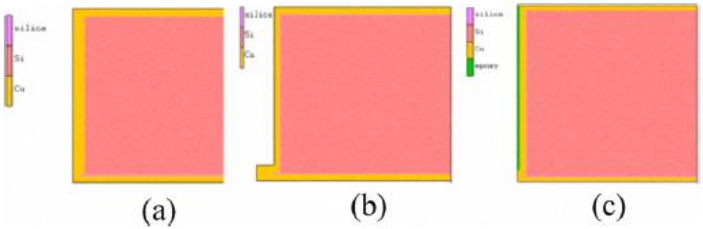
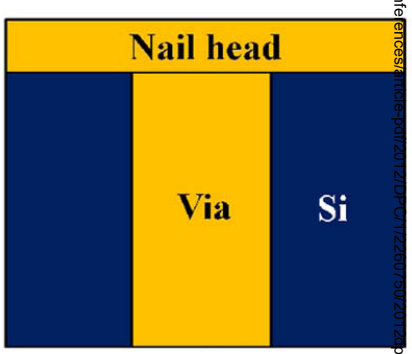


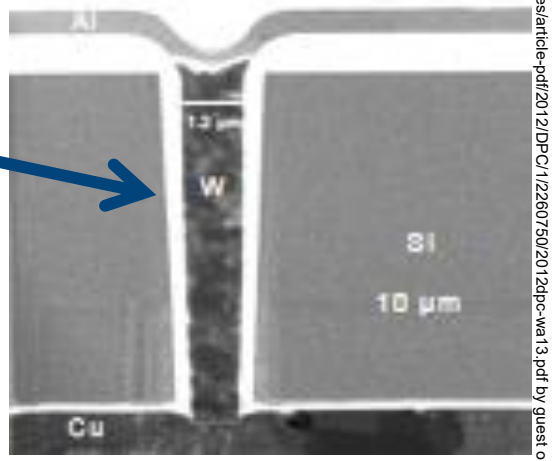
Fig.2: a) Filled copper via, b) Carpeted via
c) Filled epoxy

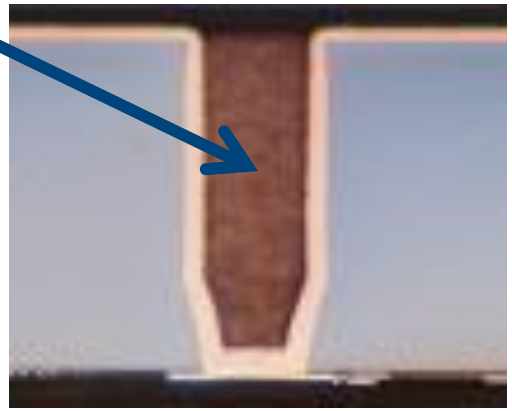
S. Barnat et. al., EuroSIME 2010



TSV Materials

- Will the via be filled?
- If yes, with what material?
  - Copper
  - Tungsten
  - Conductive polymer

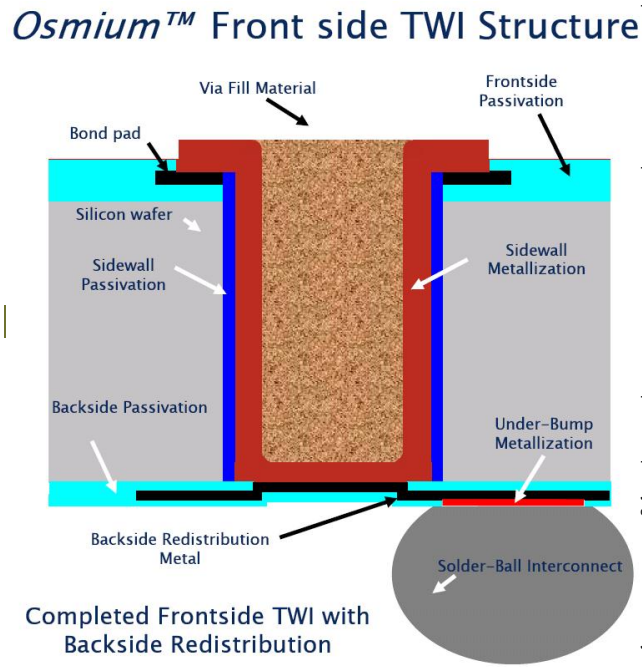




Why Tungsten?
Low CTE mismatch with Silicon

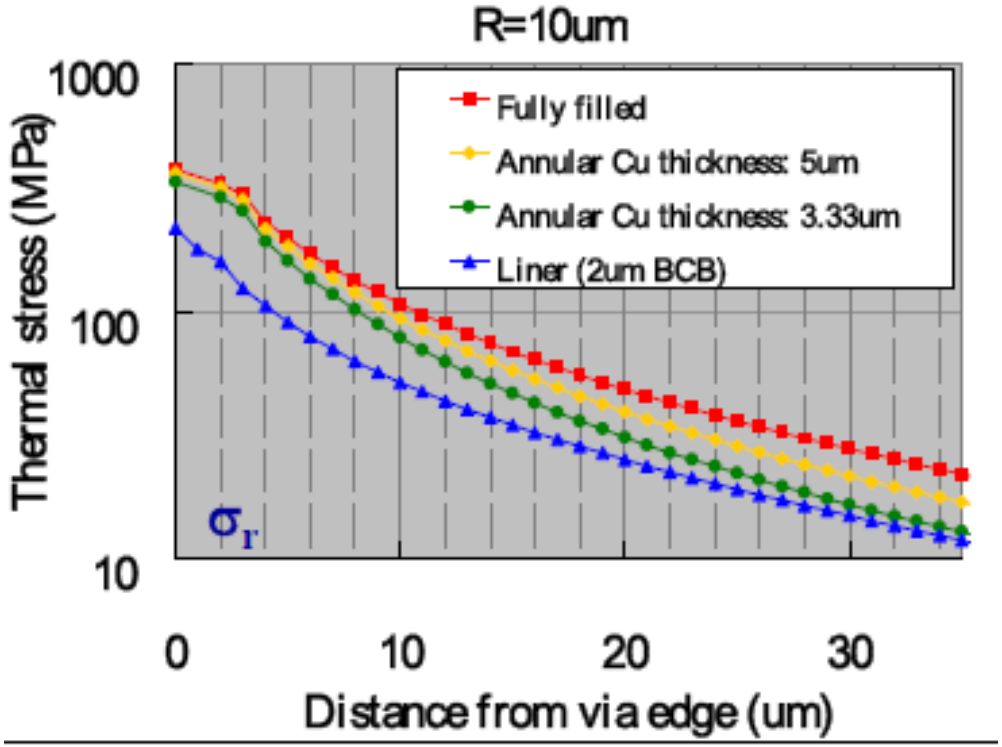
Via Fill (Tradeoffs)

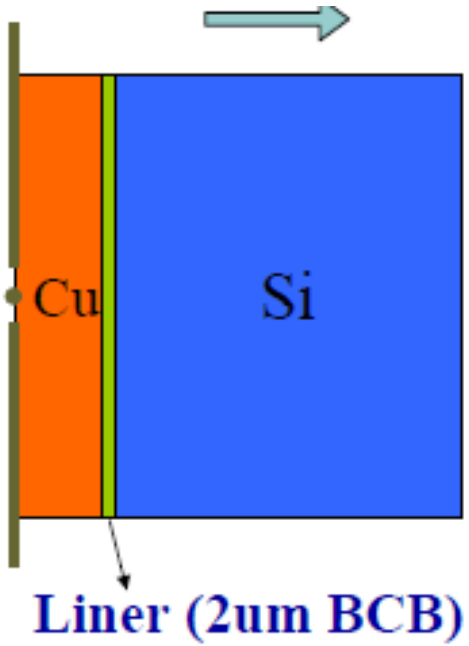
- Solid Fill (copper, nickel, tungsten, aluminum, etc.)
  - Most robust (fatigue)
  - High stress in silicon
  - Longest process
  - Enhanced thermal performance
  - Greater density (think filled microvias)
- Polymer Fill
  - Still robust
  - Reduced stress in silicon
  - Shorter process, more expensive material
- No Fill (annular)
  - Least robust
  - Lowest stress in silicon
  - Fastest process, lowest cost



TSV Materials (cont.)

- The TSV can have a polymer liner
  - Significant reduction in radial stress





K. Lu et. al., SEMATECH 2008

TSV Process

- Is the copper deposited through electroplating or chemical vapor deposition (CVD)?
  - CVD primarily for small holes (<3um dia.), high aspect ratio
  - EP for larger holes (>5um dia.)
- Will there be an anneal after plating?
- Stress free temperatures can be completely different
  - Electroplated copper is stress free near room temperature (25 – 50C)
  - CVD can occur at 400C
  - Annealing can occur around 200C
  - Lu measured 125C (Via First, before BEOL, no fill)

Cracking of Copper TSV

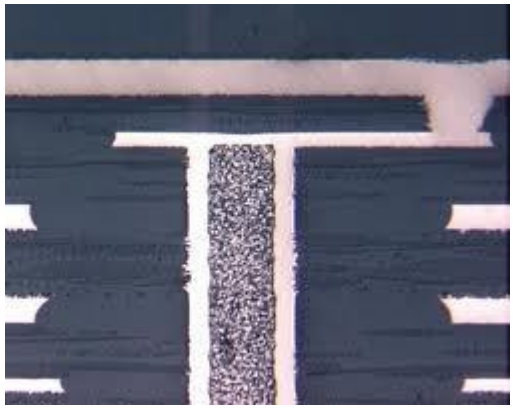
- Will copper in TSV experience fatigue cracking?
  - Classic circumferential fatigue cracking of copper plating is currently unlikely for two reasons

- Reason #1: Hole Fill
  - Most TSV concepts seem to be moving to a solid plug design (fully filled)
  - A partial fill or plated barrel likely a process defect (pinch off due to non-optimized leveler)

Example: Filled PCB Vias

- Filled PCB vias (copper, solder, or conductive fill) do not fail when subjected to temperature cycling

- KEY EXCEPTION
  - Partially filled PCB vias fail **faster** due to the presence of a stress concentration

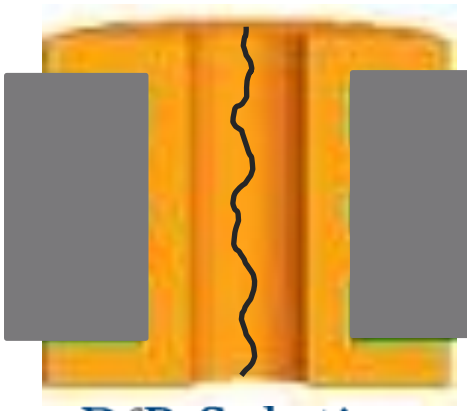


Cracking of Copper TSV (cont.)

- Reason #2: Unfilled Via and Compressive Stress
  - Unlike in PCB, the 'matrix' (i.e., silicon) has a lower coefficient of thermal expansion (CTE) than the barrel
  - There is also a lower CTE mismatch
    - PCB: 50ppm vs. 17ppm (33) / TSV: 2ppm vs. 17ppm (-15)

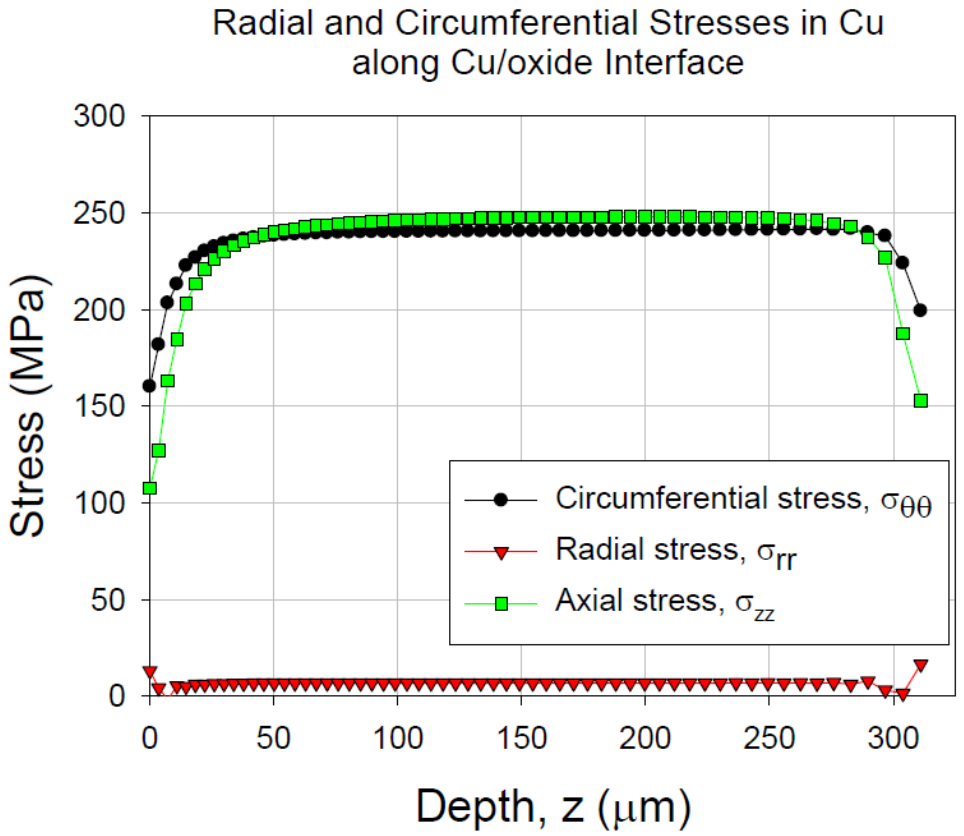
- If electroplated, stress free state should be at room temperature
  - Any increase in temperature, due to hot spots or change in ambient conditions, will place the copper plating under an axial compressive stress

- The tensile stress then arises circumferentially
  - Could induce cracking along the length of the via, but will not cause electrical failure



Cracking of Copper TSV – Possible Exceptions

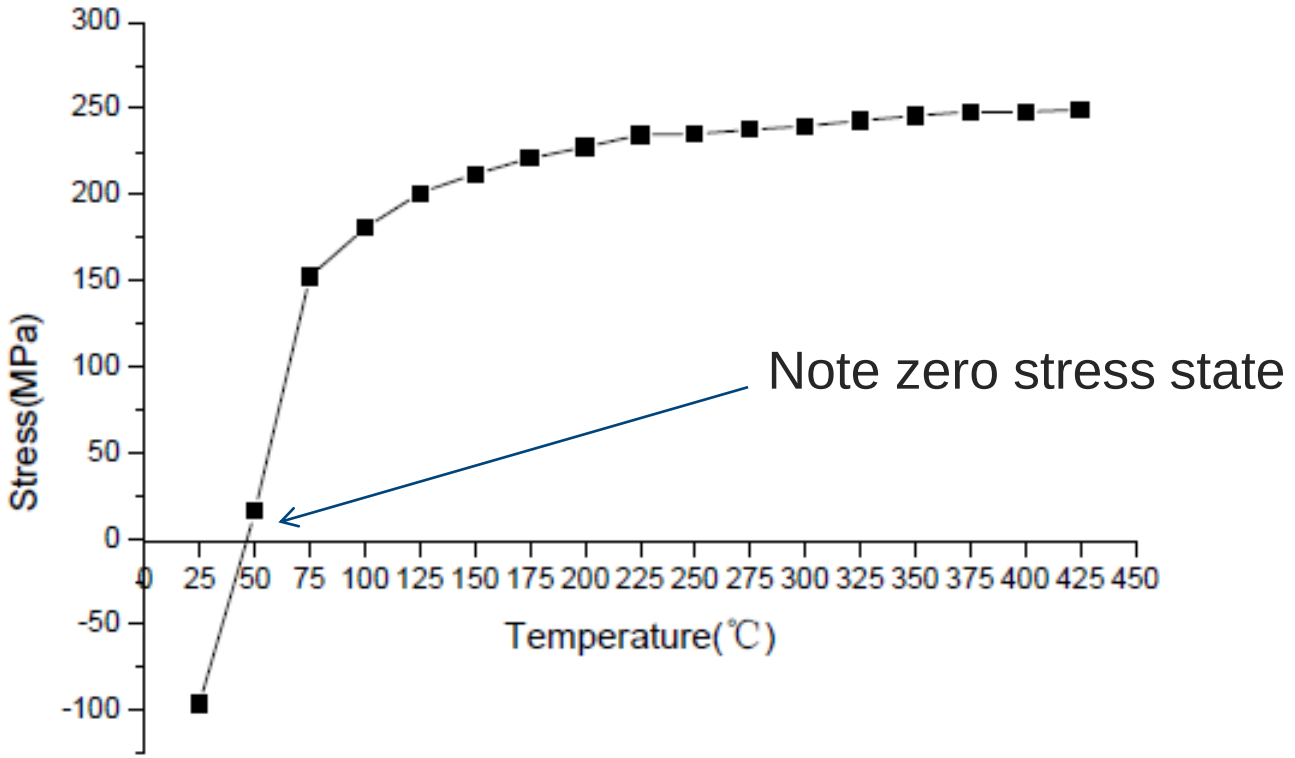
- Lu claimed very large stresses in the copper plating for annular TSV



Lu, Dissertation, UTexas, 2010

Cracking of Copper TSV – Possible Exceptions

- Liu measured (XRD) similar stress levels in filled TSV



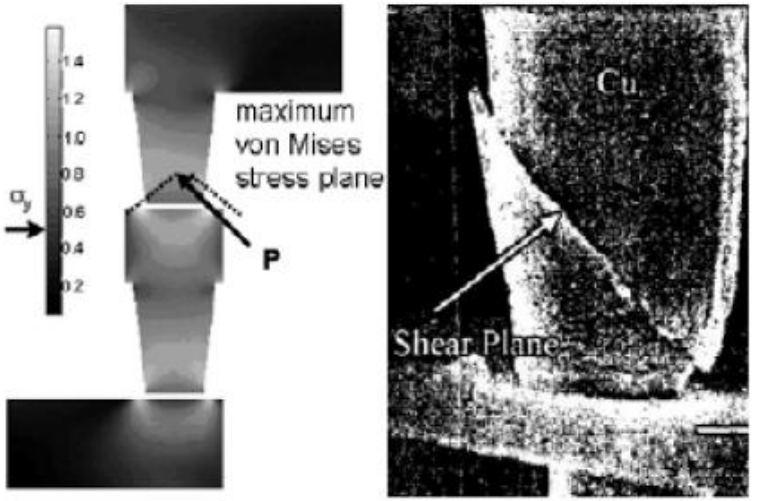
Liu, ECTC, 2009

Cracking of Copper TSV – Possible Exceptions (cont.)

- One publication seems to show stress-driven cracking of TSV, but little additional information is provided

Shear stress for plated Cu is dangerously close to yield for ~250°C TSV processing temperatures and CTE differences. What happens if we place an additional time or spatial gradient driven stress from power up and power down cycles or hot spots of 30-60°C?

J. McDonald, Thermal and Stress Analysis Modeling for 3D Memory over Processor Stacks, SEMATECH Workshop on Manufacturing and Reliability Challenges for 3D IC's using TSV's, 2008



Cracking of Silicon – Single TSV

- Stresses within the silicon can be computed using plane-strain analytical solution known as Lamé stress solution

Cylindrical

- σ_r and σ_θ are radial and circumferential stresses
- E is modulus, $\varepsilon_T = (\alpha f - \alpha m)\Delta T$ (thermal mismatch strain), D_f is TSV diameter, υ is Poisson's ratio

$$\sigma_r^{Si} = -\sigma_\theta^{Si} = \frac{-E\ \varepsilon_T}{2(1-\nu)}\left(\frac{D_f}{2r}\right)^2$$

Lu, Dissertation, UTexas, 2010

Cartesian

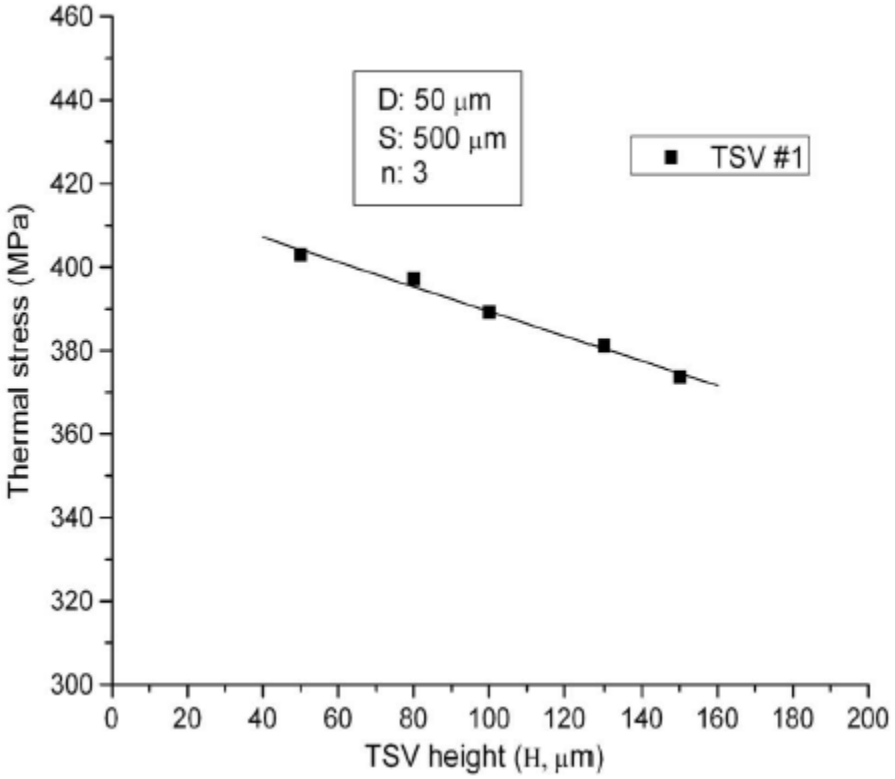
- σ_{xx} and σ_{yy} are inplane stresses
- B is modulus, $\Delta\alpha\Delta T$ is thermal mismatch strain, r is TSV radius

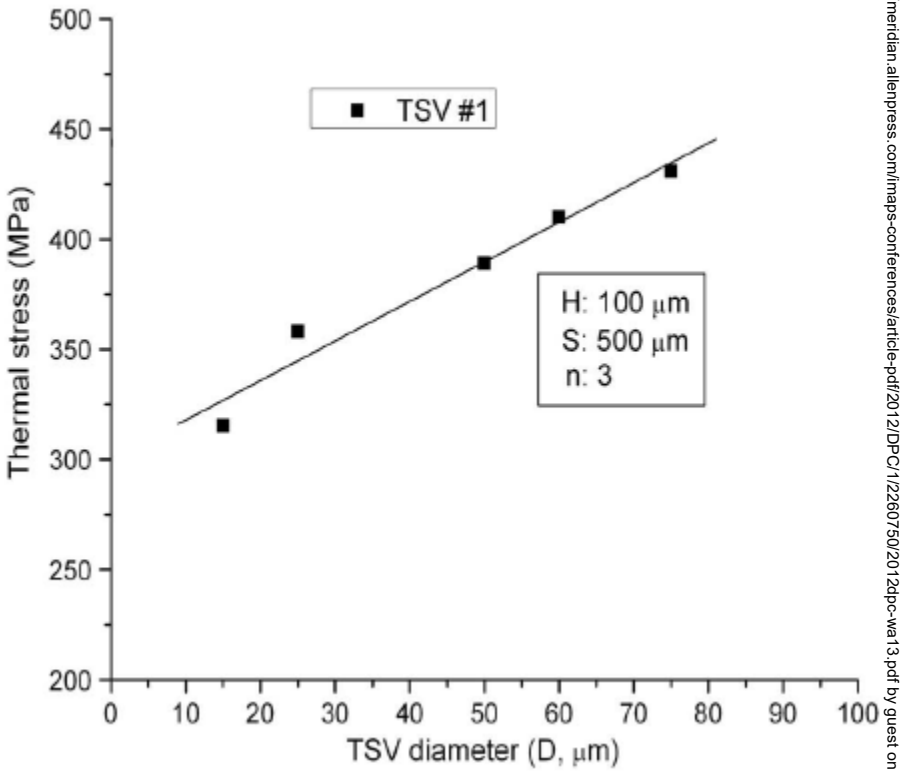
Zhang, IEEE Trans. ED, 2011

$$\sigma_{xx}^m = -\sigma_{yy}^m = -\frac{r^2 B \Delta\alpha \Delta T (x^2 - y^2)}{2(x^2+y^2)^2}$$

Ignores elastic mismatch

Stresses in Silicon (cont.)





Zhang, IEEE Trans. ED, 2011

Stresses in Silicon (cont.)

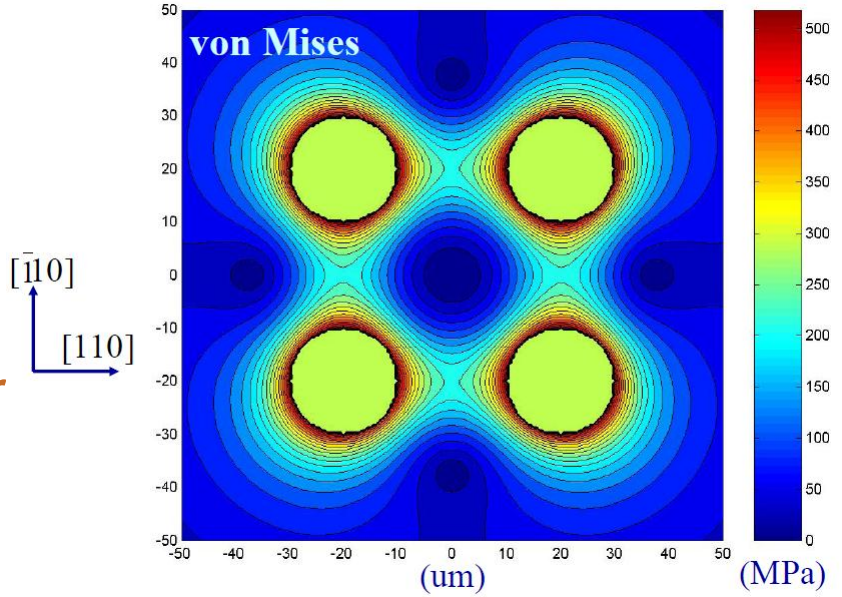
- Are these stresses high enough to cracking semiconductor-grade silicon?
  - Unlikely
- Fracture strengths of silicon wafers have been reported between 1 – 20 GPa Ritchie, Failure of Silicon, 2003
- Some debate about silicon and fatigue
  - Dauskardt reports no fatigue behavior
  - Ritchie reports fatigue behavior up to 0.5 fracture strength

Cracking of Silicon – TSV Array

- These stresses can be adjusted for a TSV array

$$\theta_2^* = \theta_1^* \cdot \frac{1}{1 - R_{VS}^*} = \frac{D^{*2}}{H^*} \cdot \frac{1}{1 - \frac{\pi}{4} \cdot \frac{1}{(S^*+1)^2}}.$$

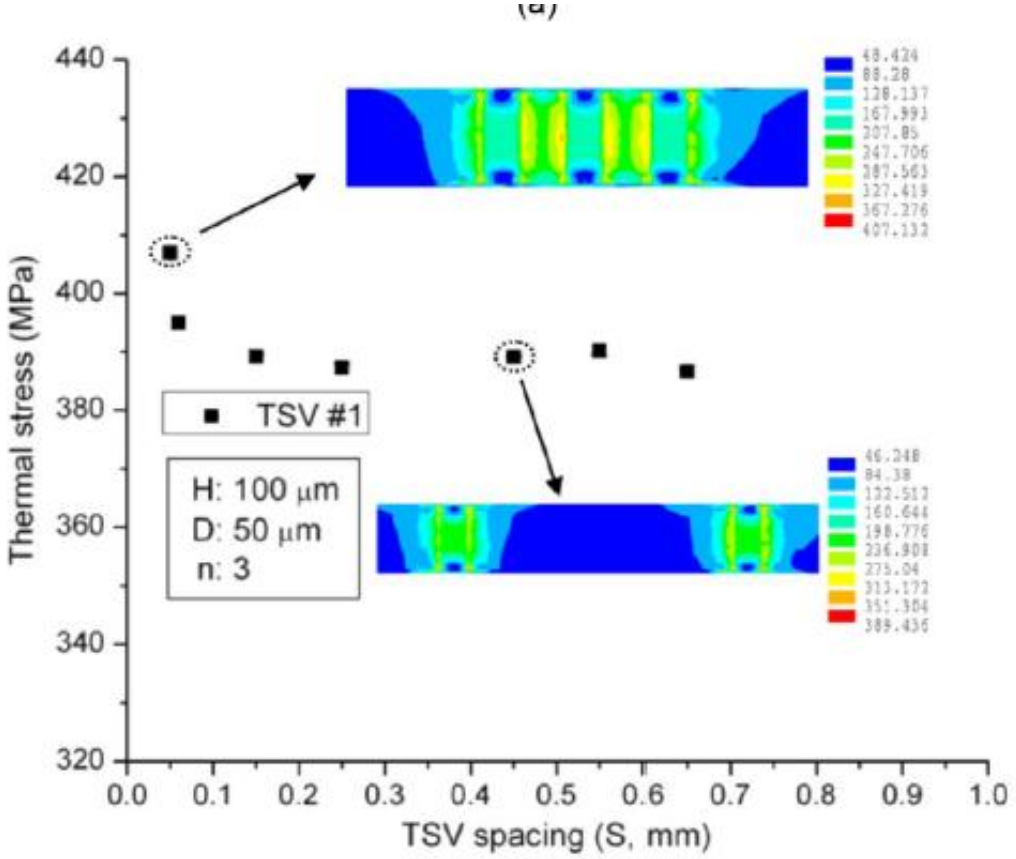
- where D is the TSV diameter, H is the TSV height, and S is the spacing of the TSV arr



Lu, Dissertation, UTexas, 2010

Cracking of Silicon – TSV Array (cont.)

- Array does not create a substantial rise in stress
- Maximum stress is theoretically 4.66 times that of a single TSV, but requires very close spacing



Zhang, IEEE Trans. ED, 2011

Resistance of Silicon

- The electrical properties of silicon (piezoresistance) will change before it cracks
  - Could require a keep out zone (or could improve performance!)

Cooling

- **Piezoresistance effects in sillicon**

$$\Delta\mu / \mu \approx \left|\pi_{//}\sigma_{//} + \pi_{\perp}\sigma_{\perp}\right|$$

S. Thompson et al., *IEEE Trans. Electron Devices*, vol.53, no.5, May 2006

(001) wafer; [110] channel	Piezoresistance coefficients (unit: Pa^{-1})	
Polarity	$\pi_{//}$	$\pi_{\perp}$
n-MOSFET	-3.16×10^{-10}	-1.76×10^{-10}
p-MOSFET	7.18×10^{-10}	-6.63×10^{-10}

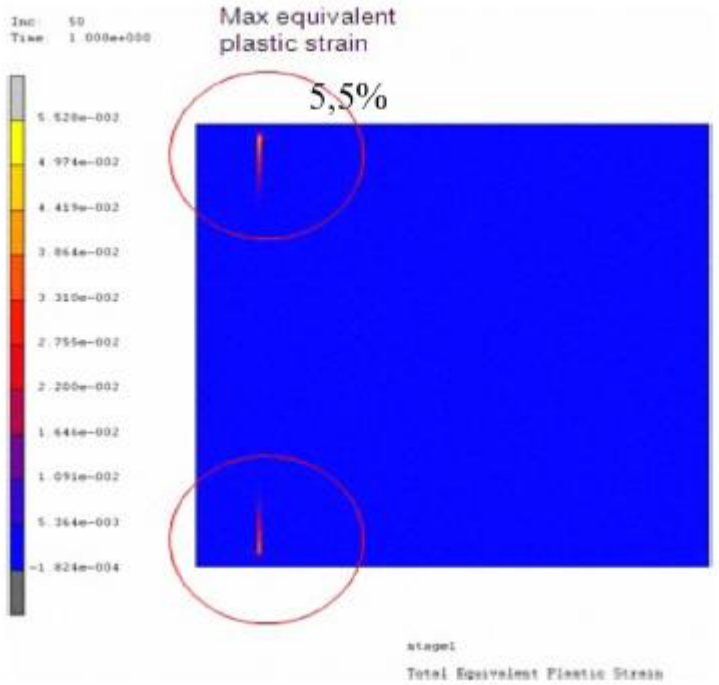
Ex: 100 MPa → up to 7.2% mobility change!

THE UNIVERSITY OF TEXAS AT AUSTIN

Lu, Dissertation, UTexas, 2010

Interfacial Failure of TSV

- This failure mechanism is the most likely failure mode of TSVs
  - Very high stresses
  - Very complex stresses
  - Difficult to measure material properties
  - Key material properties not controlled (i.e., fracture strength)



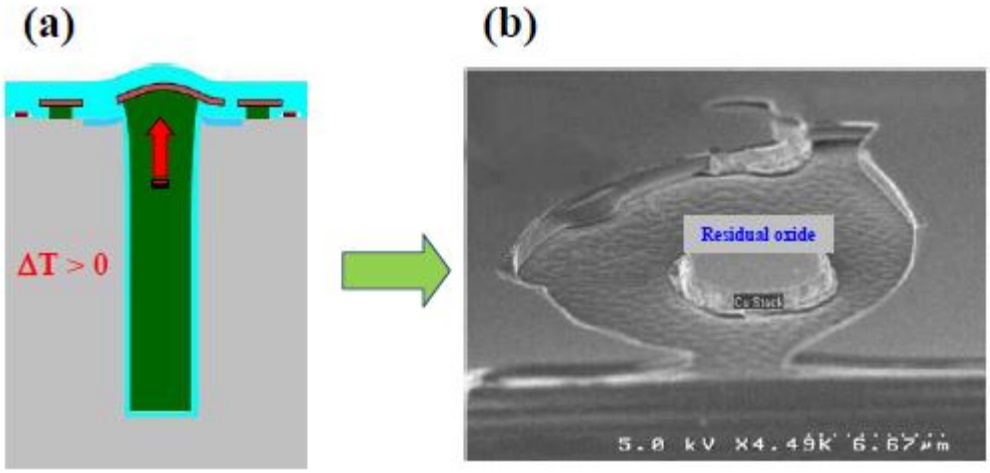
Interfacial Delamination (cont.)

- Analysis by Dudek identified risk of micro cracking and delamination problems at the upper via pad in a local model.
  - R. Dudek, et. al., Thermo-Mechanical Reliability Assessment for 3D Through-Si Stacking, EuroSimE, 2009

- Liu found that Cu/SiO2 interfacial cracks and SiO2 cohesive cracks are likely to initiate and propagate at the corners of electroplated Cu pads, where large stress gradients and plastic deformation exist
  - X. Liu, et. al., Failure Mechanisms and Optimum Design for Electroplated Copper TSV, ECTC, 2009

Interfacial Delamination

- Interfacial delamination of TSVs was found to be mainly driven by a shear stress concentration at the TSV/Si interface
- Can result in TSV extrusion, fracturing the overlaying dielectric material



P. Garrou, "Researchers Strive for Copper TSV Reliability," Semi Int, 03-Dec-2009.

TSV Failures (Summary)

- Ability to predict TSV reliability still in its infancy
  - Hampered by little published test data (primarily simulation)
- Any prediction must taken into account changes in interfacial material
  - Don't simulate/test nominal; investigate realistic worst-case
- However, there is no need to reinvent the wheel
  - A significant amount of relevant material, especially in regards to interfacial reliability can be found in studies on fiber-reinforced ceramic composites