Material Requirements for Power and High Temperature Multilayer Ceramic Capacitors (MLCC)

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Abstract: Recent trends and progresses in power electronics rely on fast, miniaturized, high current and high temperature switching semiconductors. However, in electronics system design, passive components technologies, in particular capacitors, limit their full exploitation. The goal of the present paper is, firstly, to analyse the capacitor technologies, in particular ceramic technologies for the limits set by high current, high voltages, high temperatures, high frequencies, and by cost items. Secondly, for each of the identified limits, to define the tools and technologies that are capable to overcome it. The new technologies include a new PLZT based antiferroelectric ceramic material with high switching field, copper inner electrode for the multilayer construction, firing in reducing atmosphere, applying a sputter method for the outer connecting electrode combined with silver sintering of a flexible termination or of a pressfit connector. The third goal is to show how the new technologies are applied such that the cost forecast in production scale is giving a good economic perspective for future use in power electronic systems. Finally, specific applications in power electronics are selected and described, where the benefits resulting from the new technologies are made evident.

Keywords: Multilayer Ceramic Capacitors, Anti-ferroelectric Ceramic Material, DC-Link, Power / High Temperature Electronic Design.

1. Introduction

The main components of power electronic systems are the switching semiconductors, the control electronics, the inductive and capacitive passive components, sensors, chassis, cooling, control electronics, and connector elements. All these need to be robust, highly efficient, and have a good relation of cost to performance. For optimum and low system size, low losses, and for lowest possible cost, a careful balancing of the semiconductor switching speed, frequency of switching, current density, and ripple and turn-off overshoot voltage is necessary. The recent trend of the development of switching semiconductors is towards higher switching frequencies, steeper switching slopes, higher junction temperatures, higher current density, and less size while keeping high robustness. The progresses in the semiconductor technology, there are interactions with the supporting passive components, in particular the DC-link capacitors.

Apart from resistors, the multilayer ceramic capacitor (MLCC) is the most widely used passive component in modern electronics. Hundreds of MLCCs are used in typical electronic devices such as cell phones, computers and in multimedia. More than 2 trillion pieces of MLCCs were manufactured in 2012.

In addition, there any many other applications in comparison to the above mentioned devices, where special requirements exist to in order to comply with e.g. functionality, size, and reliability. In order to achieve miniaturization and efficiency improvements on the system level also the involved capacitors must be able to follow these trends. In most of the applications of MLCC, the low cost for the components is resulting to a large extent from the large-scale economy manufacturing of standard products resulting in very good performance/price ratio. The mayor trend is the miniaturization, which is partly due to the continuous lowering of the voltage rating, and the lowering of power consumption of the application. For the use in power electronics however, with the high voltage rating exeeding e.g. 250 Volt, other optimization parameters are often required, especially the need for high capacitance at high voltage and high currents.

In the present paper these shortcomings of the classical MLCC with respect to their application in power electronics will be dealt. At first, the relation between the MLCC specifications and the basic material properties for ferroelectric and for antiferroelectric ceramics are discussed. From the power electronics requirements, it is shown, that the ferroelectric MLCC cannot comply with the needs of high currents at high temperaures simultaneously. A change in development trend direction is needed, and it is recommended to develope and improve anti-ferroelectric dielectrics in the future, which are able to be processed with base metal electrodes. These materials can comply with the high current / high temperature needs, because of their material properties [1,2].

Then, the main recipe and the potential recipe road maps are compared.

Further requirements in power electronics which are different from comsumer and mobile communication electronics are the temperature cycling requirements, and enhanced robustness and lifetime issues. Further material requirements result, and the implications for the design features of the multilayer construction are discussed.
A recommendation is given for the design of the outer termination connecting the component with the system in order to improve reliability and functionality at high temperatures.
Differences in multilayer processing for ferro -and antiferroelectric ceramics are explained, and an analysis is made for the cost drivers that will be decisive for future acceptance of any new ceramic power capacitor solution in the marketplace.
Finally, arguments are presented for a technology road map, which take into account these cost drivers. A conclusion is made for a cost road map. In case that the development progress for base metal anti-ferroelectrics is similar to that of ferroelectrics in the last decade, a good economic perspective for anti-ferrolelectric ceramics with copper inner electrodes for use in power electronics is concluded.

2. Requirements and trends of Capacitors for Power Electronics

The following criteria of the capacitors are important to be considered in any application:
High capacitance density, voltage range, current capability, ESR (Equivalent series resistance), loss DF (dissipation factor), high frequency capability, capacitance stability, temperature capability, energy density, very low leakage and cost.
Further criteria are e.g. easy use in the electronics manufacturing processing (e.g. in a standard SMD manufacturing line), high mechanical stability, and reliability (life expectation, robustness with respect to humidity).
In marketplace, there is common understanding that MLCC specification is such that the capacitance is measured at 25°C, 10kHz, Vrms = 1 Volt, no bias voltage applied and the same holds for the dissipation factor, and comparisions are made on the basis of this condition. However, in power electronics, e.g. when using the capacitor as a DC - link, or a snubber there is the need for specification at high link - voltage (e.g. 400 Volt DC- link voltage for 650 Volt semiconductors), at higher ripple voltages, and at much higher frequencies according the switching features of the semiconductors.

The trend of the semiconductor switches is driving the overall trend in power electronics. Faster slopes, higher current densities less size and higher temperatures are commonly accepted as the present trend items. Recent silicon semiconductors, an also wide-bandgap semiconductors like SiC and GaN are fully supporting these trends. The passive components trend has to follow this main driver.

Based on a of datasheets, reports on capacitor usage, company news and own experience of the author, there are limits and trends for capacitors in power electronics as shown inTable 1.

	Present limits	Trend (emerging or required)
ESR related	< 1 A/µF	>> 1 A/µF
Temperature	≤ 70 °C mean 90 °C peak	> 90 °C mean > 150 °C peak w/o cooling
ESL	~ 15 nH	< 2 ~ 5 nH
Size	DC–link caps determine size, e.g. 5cm³ for 1Amp	DC – link caps are / can be highly integrated, << 1cm³ / Amp
Frequency	10 ~ 30kHz	> ~ 30kHz up to 1 GHz
Cost	Component as low a.p.	System cost down capability

Table 1: Present limits and trend for capacitors in high efficient power electronics

Presently, the dominant capacitor technology for high power electronics (e.g. P > 1 kW), is the film capacitor technology. Exceptions are some special application areas, where size, high frequency, and high efficiency are important requirements. In fact, film capacitor technology combines relatively low cost with stable capacitance over bias. The reasons why MLCCs have not yet entered the market segment may become clearer with the analysis of the present paper.

3. Ceramic dielectric materials and properties

Today´s commercial ceramic dielectrics have a zero field dielectric constant (K) that has a range from 5 to greater than 20,000, while temperature dependence ranges from few ppm/°C to several %/°C.
In general, they are categorized into three classes :
1) Class I dielectrics are low K (5 to a few hundred) ceramics with low dissipation factor (<<0.01). They have a linear temperature coefficient of permittivity from zero to several thousand ppm/°C with a prescribed tolerance, and no dependence of dielectric constant on bias.
2) Class II dielectrics are high K materials (1,000 to >20,000 at zero field), mostly based on ferroelectric ceramics. One important feature in this class of dielectrics is the moderate-to-high temperature dependence of dielectric constant ; the second important feature is the decrease of the dielectric constant with increasing bias.
3) Class III dielectrics are the basis for barrier layer capacitors. Due to the low operating voltage (usually <25V), this class of materials will not be discussed further.

Class II is the category considered in the context with power electronics, because of their relatively high zero field permittivity, and the relatively low temperature coefficient when applied in high voltage MLCC.
For the class II MLCC designed for standard applications, ferroelectric barium titanate is the major basis material of choice for ceramic dielectrics.
The ferroelectric behaviour of the electronic polarisation, is schematically depicted in Fig.1 (a), together with the dielectric constant K. Due to saturation of D with E, there is a decrease of K (the differential dD/dE) with bias field E, which is a systematic effect for all ferroelectrics. The shaded area is the integral of DxE, which is the *energy* contained in the dielectric when voltage is applied.

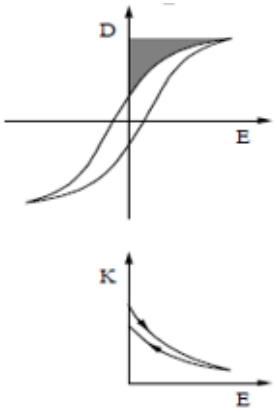


Figure 1(a): Ferroelectric, polarization curve (after [3])

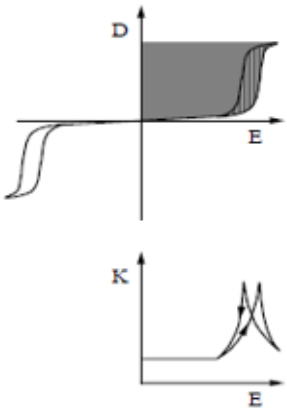


Figure 1(b): Anti-ferroelectric

Commercial class II MLCC mostly have Barium titanate ($BaTiO_3$) as the mayor constituent and have base metal (Ni) inner electrodes. $BaTiO_3$ has a perovskite crystal structure that exhibits three phase transitions when cooled down from high temperature, namely cubic to tetragonal at ~120°C, tetragonal to orthorhombic at 0°C, and orthorhombic to rhombohedral at −90°C. Each phase transition is associated with a dielectric peak, which is not at all an ideal behavior for a capacitor dielectric, but on the other hand it is the source for the high K at zero field. The usual way to smoothen the temperature dependencies, is to generate the so-called core-shell grain structure effect (see e.g. [4]). The ceramic grains consist of low doping BaTiO3 core and an outer region with compensating temperature characteristics that is created by adding small amounts of dopants (donor, acceptor or indifferent) to the dielectric powder. The thickness of the shell is determined by the diffusion of dopants during sintering. The combined dielectric behavior of the core and the shell results in relatively little temperature dependence of the dielectric constant (e.g., the X7R characteristics, acc. EIA nomenclature). For achieving high reliability, rare earth dopants (e.g. Dy or Ho) are used to prohibit functional deterioration when high thermal and electrical load are applied.
It is important to realize, that *all* ferroelectrics show a decrease of dielectric constant with bias voltage, with no exception. The high K values noted above always go down to 400 ~ 500, when the voltage has induced full ferroelectric polarization. The corresponding anti-ferroelectric behaviour of the electronic polarisation, is schematically depicted in Fig.1 (b), in contrast to the ferroelectric case the dielectric constant i slow for low field, and increases then. Fig. 2 shows examples. The field dependence of K is shown for an antiferroelectric capacitor (with Cu inner electrodes, commercially available as « CeraLink » from EPCOS), in comparision with a commercial $BaTiO_3$ - based MLCC. For the latter it is important to emphasize, that the zero field value of K does not matter, the high field value of K will go down to 400 to 500 anyway. A further note is, that in ($BaTiO_3$) - based MLCCs designed for power electronics use the field strength at reated voltage reaches values >20 Volt/µm, otherwise the capacitance density will go down considerably.

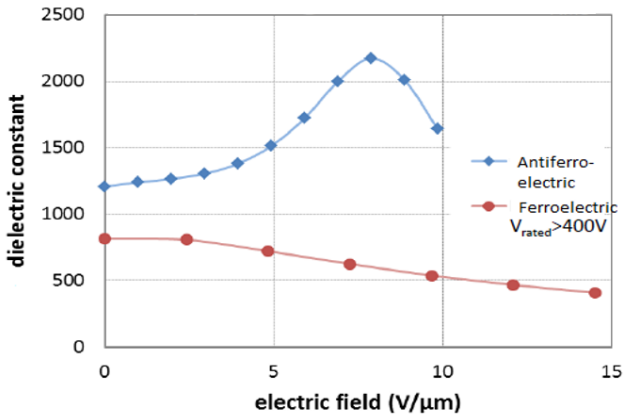


Figure 2: Dielectric constant (for 25°C, 1 kHz, measurement with 1 V_{rms}) as a function of the electric field strength. The anti-ferroelectric is the CeraLink™ from TDK EPCOS, the ferroelectric is a commercial ($BaTiO_3$) - based MLCC. The picture is from [5].

The relation of the field strength in the anti-ferroelectric material, and the voltage is via the dielectric thickness. The maximum in the dielectric constant from Fig. 2 is at ~8 V/µm, using a dielectric thickness of 50µm then results in a voltage of 400 Volt. This shows how, e.g., a DC-link voltage of ~400 Volt can be favorably matched with the maximum of a dielectric curve. Since higher dielectric constant means higher current capability, anti-ferroelectric curve turns out as a material requirement for ceramic power capacitors.

There are only few material systems, which do not only show anti-ferroelectric behavior, but also fulfill the necessary other requirements, e.g. process ability in a multilayer process. The most important material system is the PLZT system. By now, there is still only

one commercial system, where a base metal electrode (Cu) is in the multilayer, namely the CeraLink™.

From XRD analysis, the chemical formula of the CeraLink™ capacitor is

(1) $Pb_{0,87}La_{0,07}(Na,K)_{0,05}Zr_{0,86}Ti_{0,14}O_3$

to a good approximation.

The material used is an anti-ferroelectric zirconia -rich PLZT ceramic material (lead-lanthanum-zirconate-titanate) with sintering aid dopants (Natrium and Potassium, see Ref. [6]). It has a rather smooth bias dependence.

There is a further effect of the Na - addition on the anti-ferroelectric effect, since adding Na to the recipe transforms the polarization curve of the material to higher values (Fig. 3, see Ref. [6]).

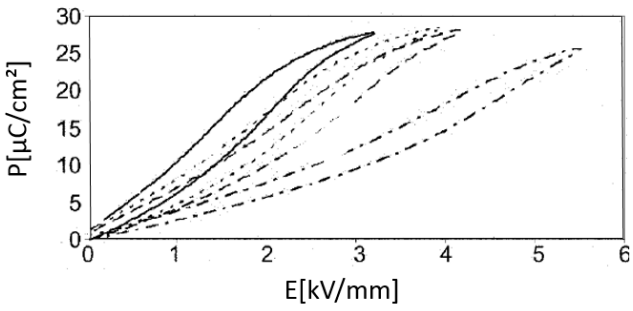


Figure 3: $Pb_{0,88-0.5x}La_{0,07}Na_xZr_{0,8}Ti_{0,2}O_3$ sintered at 1250°C for x=0, x=0,005, x=0,01 and x= 0,03 (from left to right). After Ref. [6].

When a bias is applied below the so-called switching field, the alignment of the dipoles along the direction of the external field results. This in turn causes an increase of the electric permittivity. At higher bias fields an anti-ferroelectric to ferroelectric phase transition is induced and the capacitance drops with increasing voltage in exactly same way as intrinsic ferroelectrics from zero field onwards.

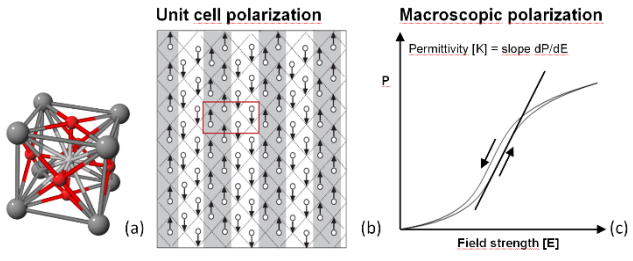


Figure 4: (a) Titanium octahedral that are linked in opposite polarity forming doubled unit cells (b), and (c) the resulting total polarization (picture from Ref. [2]).

There is a further effect ("large signal" - capacitance), for quasi-static conditions, when a slow change of voltage is superimposed onto the bias voltage. The "large signal" capacitance reaches values more than double that of the "small signal" capacitance [see data sheet].

As already stated, low leakage - currents are important criteria for efficient and reliable power electronic systems. Thus, the capacitors used in the DC-link must have a very high isolation resistance at high bias fields and elevated temperatures. Defining

$$\tau = R_{ins} \cdot C = \rho.\varepsilon \ \text{[sec]} \qquad (2)$$

a comparison of different capacitor technologies is possible, which is independent of geometrical factors like dielectric thickness and area (ρ is the specific resistance, ε the dielectric permittivity). Figure 5 shows the time constant for the new PLZT capacitor material compared with those of standard MLCC and film capacitors. At room temperature, all technologies show very high time constants.

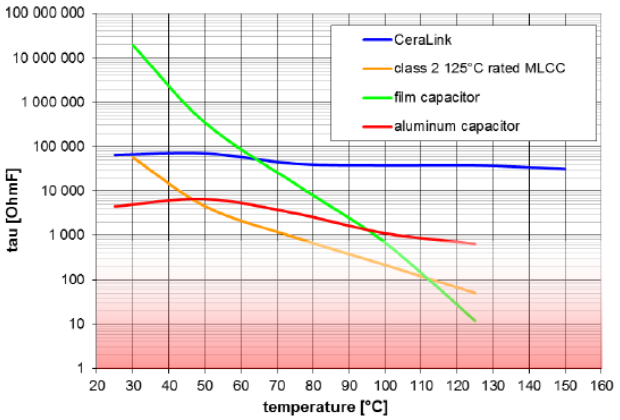


Figure 5: Temperature dependent insulation time constants for PLZT, Bariumtitanate and film based capacitor technologies (after [5])

The decrease of τau with increasing temperature, however, is critical for barium - titanates and film technology when values below the critical τau-value of ~ 500 or even ~ 100 [sec] are effective. In contrast, the PLZT material remains with high isolation resistance up to much higher temperatures (up to 150°C and even more).

Together with the reversed bias effect, high capacitance density, and considerably higher current density, this is the strongest argument for increasing use of the new anti-ferroelectric MLCC in power electronics in the future.

4. Device constructions

The standard MLCC construction in the case of Ni inner electrodes is a monolithic SMD with an outer termination consisting of a fired Cu termination paste covered with plated Ni/Sn layers.

For high quality applications however (with "Zero-defect requirement"), where high capacitance at high voltage is required, e.g. in automotive industry, lead frame construction have higher robustness with respect to mechanical stresses, and are thus often preferred.

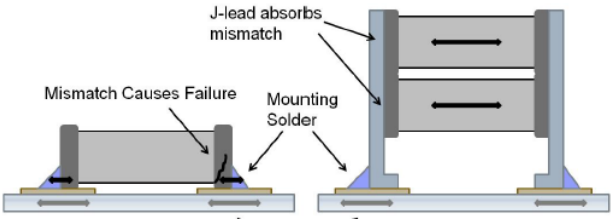


Figure **6**: Effect of J-lead to reduce mechanical stress resulting from mismatch of PCB (e.g. FR4: 12-15 ppm/°C versus X7R MLCC: 7 ~ 10ppm/°C), see Ref [7].

A similar construction is also realized for the anti-ferroelectric MLCC (Fig. 7), but with the difference that there is no fired termination paste with plated layers. Instead, a sputter layer (e.g. Au) is applied to the lapped ceramic surface.

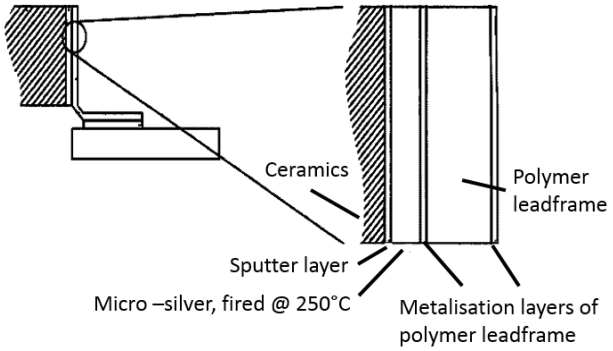


Figure **7**: Polymer leads (e.g. polyether-ether-keton, PEEK) attached by high temperature silver lead fired at ~ 250°C (Ref [8])

Then, a low temperature µ-silver sintering technique is applied to connect the sputtered ceramic with a metallized (Cu) polymer lead. It has been shown that connections based on this new sintering technique are stable up to several hundred thousand power cycles, which cannot be achieved by other lead-free soldering methods, where micro cracks form along alloy phase boundaries which in turn alter the current distributions and may lead to function failure at high current.
This construction according Fig. 7 however is well suited for fulfilling the requirement of high currents and temperatures in inverters, together with short time current overload from low to high temperatures, as this usually causes massive self-heating of the involved components.
Together with the other high temperature features of the anti- ferroelectric MLCC (low leakage, low ESL, etc.), the mounting of such a capacitor even within a module is possible.

For the connection of the semiconductor module to PCB or ceramic plate, the press-fit connection technique is used for high reliability connection.

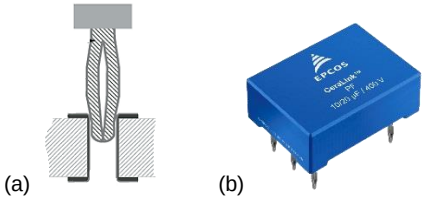


Figure 8: (a) Press-fit connector, (b) Ceramic antiferroelectric capacitor with press-fit connectors.

For achieving high robustness, there are also helpful tools for the inner multilayer construction. A quite simple and very effective method is to apply inner series connection of two capacitors, see Fig.9.

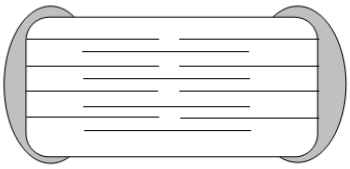


Figure **9**: Schematic view of inner serial design.

In case of a weakness within the multilayer structure, there is a high probability that any increase of failure current is prohibited by the "second" capacitor.
This is illustrated for the case of a crack, which is one of the most severe damages occurring after mechanical overstress in Fig. 10.

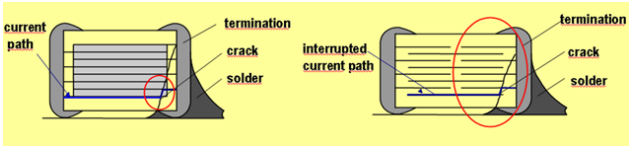


Figure 1**0**: Current path comparison in case of failure between standard MLCC vs. MLCC with internal series. Left: leakage run – away is possible and in case of low ohmic application leading to more and more destructions along the current path. Right: the current is not increasing beyond the isolation of the dielectric irrespective of the voltage source impedance (see Ref. [9])

For less severe cases, the overall robustness increases markedly (see e.g. Ref. [9]). This method is standard for the design of high voltage capacitors.
An important further design tool is to relieve the mechanical stress in the ceramic. For this purpose, a soft/ porous layer is introduced, as shown in the example of Fig. 11.

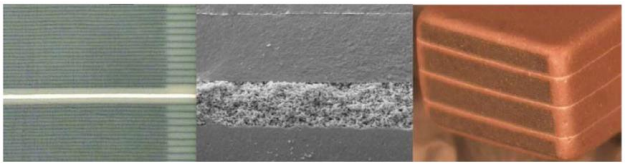


Figure 11: Porous stress relieving layer in the multilayer structure, SEM picture, and macroscopic view. (After: [M. Ellis, Bodos Power systems, November 2013, www.bodospower.com]).

Also, in the CeraLink™, such a relieving layer is present (consisting of a simple slit) and described in Lit[..] to improve the robustness (see Fig. 12 for the combined effect of series connection and the stress relieving layer). In comparison, a device without such means of enhancing robustness, would have much lower breakdown figures (estimated factor of 2)

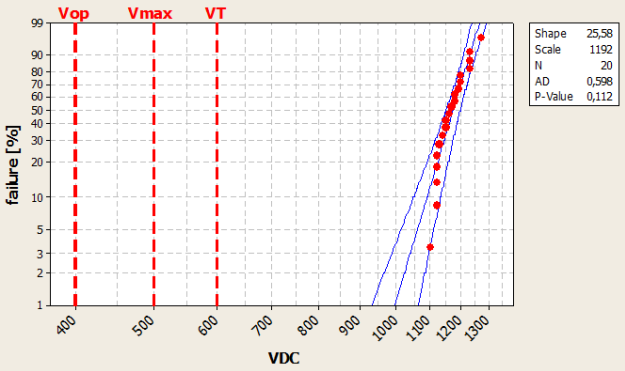


Figure 12: Improved breakdown voltage by serial inner design and inner relieve construction compared to operating voltage Vop, maximum application voltage Vmax, and factory testing voltage. (After [2]).

It is evident, that all the described design tools are of utmost importance for the application in power electronics, with high currents at high temperatures.

4. Processing

The MLCC Production process is similar for both ferro- and antiferroelectric devices. The major difference is the copper inner electrode versus nickel Inner electrode.
The production process steps overview and the major differences between the Ni inner electrode BTO systems and the Cu inner electrode PLZT system is summarized in table 2.

Process step	Anti-ferroelectric MLCC	Ferroelectric MLCC	Difference in function(s)
Powder	PLZT	BTO	Antiferro- vs. ferroelectric
Slurry, tape casting			No difference
Electrode printing	Cu inner electrode	Ni inner electrode	Lower contribution of Cu to total ESR, higher thermal conductivity
Laminating			No difference
Binder burnout	In reducing atmosphere	In N2 atmosphere	None
Sintering	~ 1000°C, in reducing atmosphere	~1350°C, in reducing atmosphere	None
Surface treatment	Lapping	Tumbling	No difference
Termination	Sputtering	Paste and paste firing in reducing atmosphere, galvanic plating	Anti-ferro: no exposure to glass frit diffusion and to plating bath(s)
Lead attach	Microbond silver	Soldering	cycling robustness improvement
Measurement and test			No difference

Table 2: Comparison and differences of MLCC production steps of BTO and PLZT.

The powder production equipment does not differ in principle. Milling equipment is needed for destruction of agglomerates in the slurry. A “degassing” of the slurry follows.
Foil casting the sheet thickness is to tight thickness tolerance, for soft drying long drying zones are used.

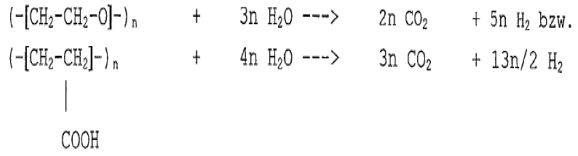


Figure 13: Principle of the steam - cracking method (Ref. [10])

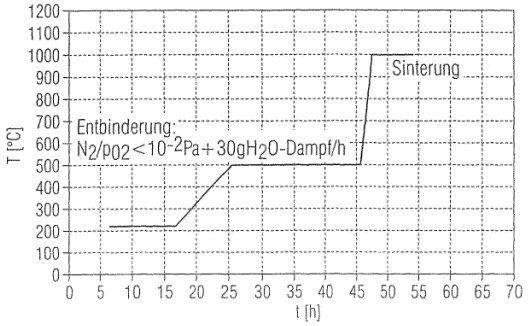


Figure 14: Example of a temperature profile using the steam - cracking method, and firing at 1000°C for densification of PZT copper multilayers (Ref. [11])

Binder burnout and sintering kilns for big production volumes of single types are usually “pusher kilns”, for small scale production “batch kiln” are common.
There is a difference in the binder burnout and firing for Cu inner electrode. For binder burn out, the principle of the “steam-cracking” see Fig. 13. This is a soft way for the debindering.
The method is e.g. used the production of Class 1 MLCC (Cu inner electrode is necessary to achieve very high Q values, see e.g. Ref. [11].
An example of the corresponding temperature and atmosphere profile of burn out and of firing for a Cu

inner electrode PZT material system is schematically depicted in Fig. 14 (Ref. [11]).

5. Endurance test requirements

Endurance test requirements depend on the application. Usually, e.g. consumer electronics specifications are less severe than automotive, avionics, or other industry. For power electronics, the lifetime, humidity and temperature cycling requirements demand very robust material system, design, and stable processes. Fig. 15 shows the standardized evaluation scheme of the lifetime of MLCC.

$$\left(\frac{\lambda_T}{\lambda_B}\right) = \left(\left(\frac{U_B}{U_T}\right)^N \exp\left(-\frac{E_a}{K}\left(\frac{1}{T_B}-\frac{1}{T_T}\right)\right)\right)^{-1}$$

λ_B = Failure rate at reference conditions (T_B = 40°C, U_B = 0,5*U_N)
λ_T = Failure rate at test conditions
U_B = Reference voltage (0.5 U_N)
U_T = Test voltage
N = Voltage exponent (N = ~3,5)
E_a = Aktivation energy (E_a = ~ 1.3 eV)
T_B = Reference temperature [K] (313 K)
T_T = Test temperature [K]
K = Boltzmann´s constant (1.38×10^{-23} J/K = $0{,}86 \times 10^{-5}$ eV/K)

Figure 15: Calculation of the fit rates of standard MLCC from the results of accelerated tests. Note that the quoted reference conditions are not suitable for power electronics, where higher mean temperatures prevail and the mean voltage is near the rated voltage.

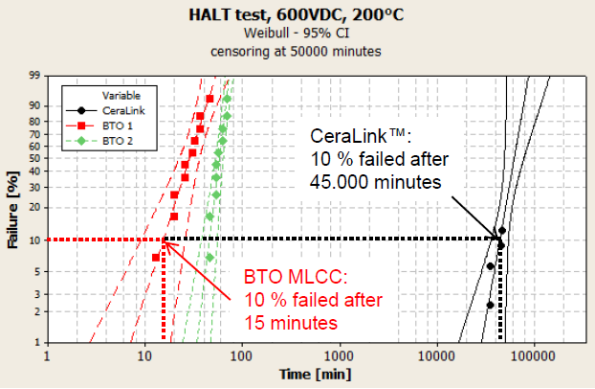


Figure 16: High accelerated life test statistics (failure% over time) for anti-ferroelectric (CeraLink™) and for ferroelectric MLCCs (Barium - titanates). The results are from Ref. [5].

The PLZT system with Cu inner electrode has exceptional high intrinsic lifetime performance, a recently published high accelerated life result for the material in Eq. (1), $Pb_{0,87}La_{0,07}(Na,K)_{0,05}Zr_{0,86}Ti_{0,14}O_3$ is shown in Fig.16.
It is to note, that the design of the BTO - MLCCs is for much higher field strength, so there is no direct 1 to 1 comparison of the technologies. However, taking the design field strength of the anti-ferroelectric as ~ 8 V/µm, and that of the BTO as 24 V/µm, then a factor of 3^N ~10 in the failure rate should be applied. Despite this, the result of PLZT is very promising for high temperature applications, and the use of such capacitors within semiconductor switching modules, even with high junction temperature operation, is feasible for the first time.

5. Applications

Due to the properties described above, there are emerging applications, which were not in reach for the film cap technology, but also not feasible for the classical ferroelectric MLCC. Table 3 shows a summary of the expanded limits for the important parameters in power electronic circuits.

Capacitor function and parameter:	para-/ ferroelectric MLCC/Ni	antiferroelectric MLCC
• Energy capability	< 0,5 J/cm³	>1 J up to ~3J/cm³
• Current capability	< 1 A/µF @ 100kHz	up to 8 A/µF@100kHz
• Temperature / current capability	< 90°C @ < 1A/µF	>=150°C @ >1A/µF
• Diel. constant at high op. voltage	~ Max. K <400 @ H.V.	>2000 @ H.V.
• Low leakage at high temperatures	<10 OhmF @ 150°C	>1000 OhmF@150°C

Table 3: Comparisons of parameters that are decisive in power electronics trend towards faster switching semiconductors.

An important basic application aspect of any capacitor in power electronics is the behavior of voltage and current in a simple switching situation. See Fig. 17 for the typical differences of ceramic vs. film capacitor.

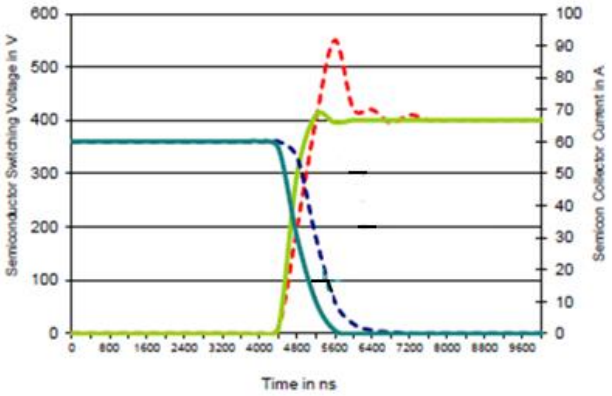
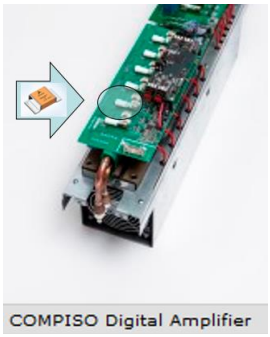
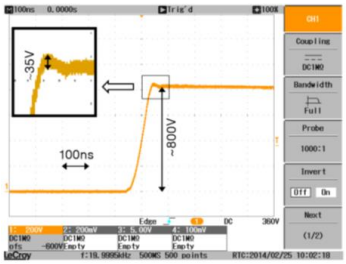


Figure 17: Comparison of the typical switching behavior of standard IGBT of film cap with anti-ferroelectric MLCC with copper inner electrode, showing the differences in onset, switching time elapsed, and voltage overshoot [5].

The anti-ferroelectric MLCC with copper inner electrode thus exhibits very low overshoot voltage, resulting in low EMI as a side effect. In the first commercial application in the marketplace for such a capacitor (application “COMPISO”), shown in Fig. 18 (see www.egston.com), the low overshoot leads to an expansion of the voltage range without the need for expanding the semiconductor voltage rating.
Another notable application is the use of the anti-ferroelectric capacitor with Cu inner electrodes in the motor integrated power electronics within the “Motorbrain” project (www.motorbrain.eu). In Fig.19, the capacitors (pressfit pins) are mounted directly at





DC-LINK Voltage Overshoot

Figure 18: Commercial use of anti-ferroelectric capacitor with Cu inner electrodes ("COMPISO" from the Austrian company Egston, www.egston.com), and picture of voltage overshoot (two 500V capacitors are in series to achieve the range to 1000Volt.

the backside of the semiconductor modules, thus the inductance of the connecting wires and their contribution to voltage overshoot is reduced further.

Figure 19: Integration of power electronic circuit into motor assembly requires very high capacitor densities and high current capabilities, shown are the anti-ferroelectric capacitors with Cu inner electrodes mounted at the backside of IGBT modules (www.motorbrain.eu).

6. Technology trend

The technology trend for capacitors over the past decades was following "Moore´s law" in analogy to that for semiconductors, by reducing dielectric sheet thicknesses. The capacitance density is simply

(3) $$C := \frac{\varepsilon_o \times \varepsilon_r \times A}{d} \quad \left[n := \frac{H}{d} \right] \quad \frac{C}{V} := \frac{\varepsilon_o \times \varepsilon_r}{d^2}$$

The capacitance density increases with quadratic exponent with the dielectric sheet thickness. There is good reason to expect the same trend that was achieved for ferroelectrics, will become reality for anti-ferroelectric material also. Thus, the trend is towards an increase of field strength to ~ 20V /µm, which means a miniaturization to 1/10 of the same capacitance. Since the cost trend follows the same law, a substantial cost reduction is the consequence. As there are no additional cost driver, the same cost structure that is known from MLCC can be used to estimate the resulting production cost (for large scale mass production) to be ~ double that of film caps. Due to the benefits in the technical parameters (see Fig. 20 for a radar-chart), the system cost decrease is an enabler for large-scale use of anti-ferroelectric MLCC in power electronics.

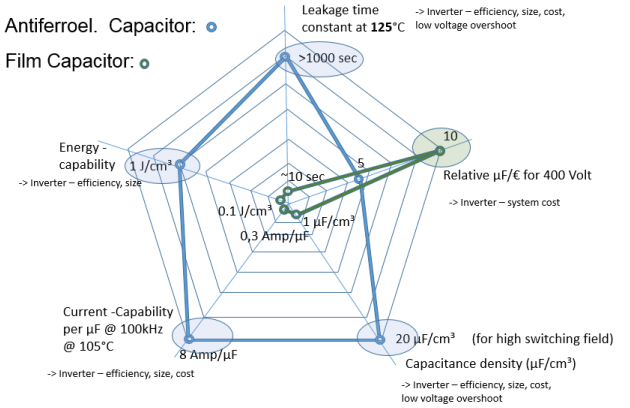


Figure 20: Comparisons of parameters: anti - ferroelectric MLCC with film capacitor depicted in radar - chart – diagram.

8. Summary

Material requirements for MLCC in power electronics are given. Based on the specific solutions for power electronics and high temperature environment, the MLCCs based on anti-ferroelectric ceramics and copper inner electrodes are recommended for use in power electronics. They combine small size, low ESR, low ESL, high current handling capability, high isolation resistance at elevated temperatures, and potentially low cost, even comparable to film cap.

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