Ultra-low Residue (ULR) Semiconductor-Grade Fluxes for Flip-Chip and MEMs Applications

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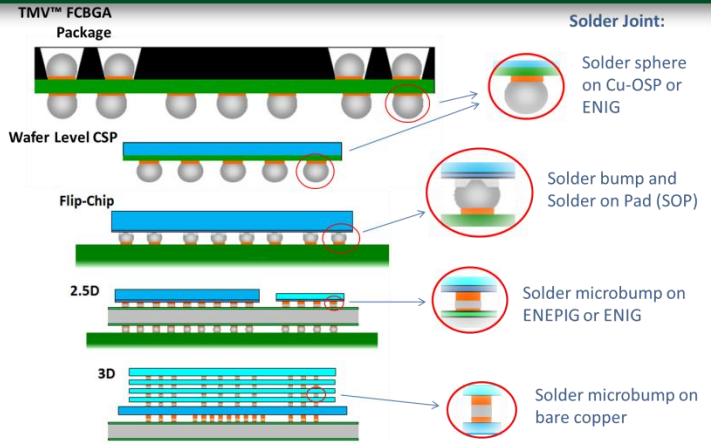
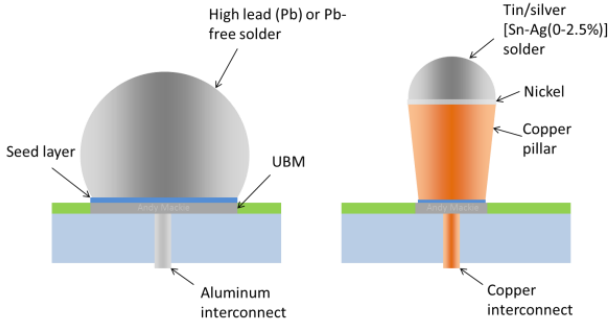
Outline of Presentation

- **Roadmaps and challenges for flip-chip assembly**
- **Characteristics of ultralow residue fluxes**
  - Rheology
    - Viscosity
  - Residue level
    - Thermogravimetric analysis (TGA)
  - Solderability
    - Wetting
  - Holding die in place
    - Movement during reflow (MDR)
  - Compatibility with MUF/CUF

Roadmap Challenges: Mobile Devices



Old and current solder bump technology



Single Chip Package Technology Requirements for Mobile Devices

	Year of Mass production =	2014	2016	2018	2020	Units
Transistor (T1)	MPU 1/2 Physical Gate Length after etch	18	15	13	11	nm
Wafer	Die thickness - Extremely thin packages (minimum)	10	5	5	5	microns
Mobile Device Packages	Cost per I/O for OSAT production (minimum cost)	0.36	0.34	0.32	0.3	(USD$/pin/100)
	Chip Area	100	100	100	100	mm^2
	Package pin count (maximum)	207 - 1100	218 - 1150	252 - 1150	278-1150	number of I/O
	Package profile or thickness (minimum)	0.22 - 0.40	0.20 - 0.35	0.19 - 0.35	0.19 - 0.35	mm
	Junction temperature - Tj (maximum)	105	105	105	105	degC
	Operating temperature - ambient (maximum)	45	45	45	45	degC

Critical points:
- **Thinner substrates**
- **Thinner die**
- **Finer pitch**
- **Lower cost**

More delicate packages and worse yield loss in assembly

Table data from: International Technology Roadmap for Semiconductors (ITRS) 2012/13 http://www.itrs.net/.reports.html

The End of Flip-Chip Flux Cleaning?

- **Package Design Changes…**
  - Pitch shrinking to 100microns and below
  - Die-substrate clearance down to 60microns and below
  - Substrates thinner and subject to warping
- **…Causing Flux Cleaning Challenges:**
  - Finer pitch makes it difficult to completely remove flux residues:
    - Conductive residues may lead to ECM
    - Can block flow of CUF and MUF leading to voiding
    - Can interfere with CUF and MUF adhesion causing delamination
  - Cleaning process:
    - Increases substrate warpage after reflow and before underfill, leading to cracked solder joints
    - Adds significant costs

Dendrites caused by electrochemical migration (ECM) of poorly-cleaned flux

→ **Move to ultralow residue no-clean flux**

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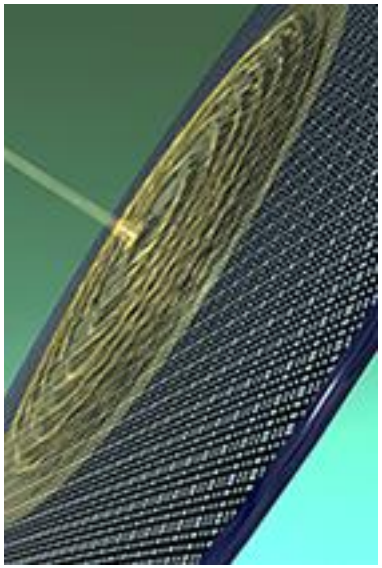
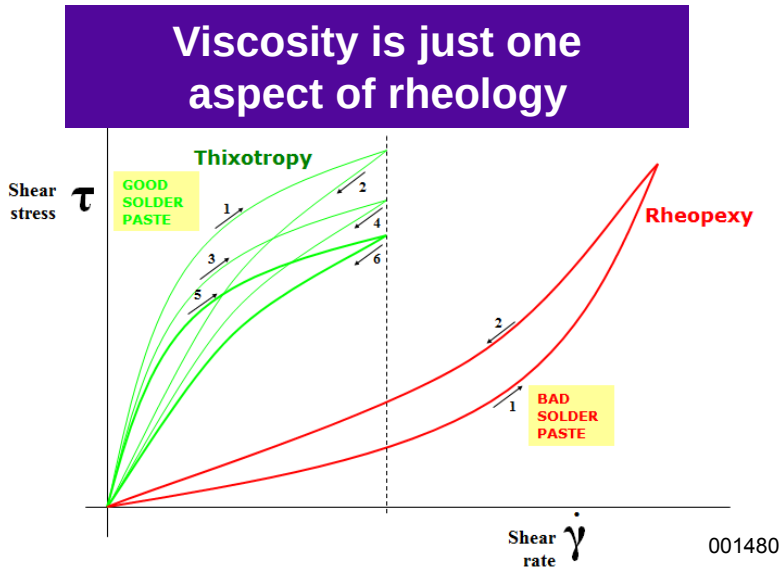
Ultralow Residue (ULR) Flip-Chip Flux Characteristics

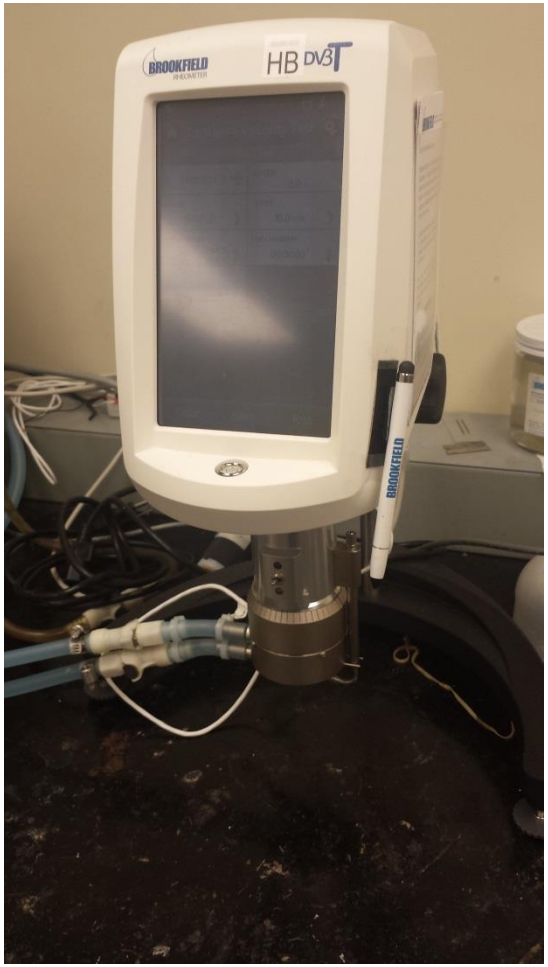
- **Rheology**
  - Viscosity
- **Residue level**
  - Thermogravimetric analysis (TGA)
- **Solderability**
  - Wetting
- **Holding die in place**
  - Movement during reflow (MDR)
- **Compatibility with MUF/CUF**



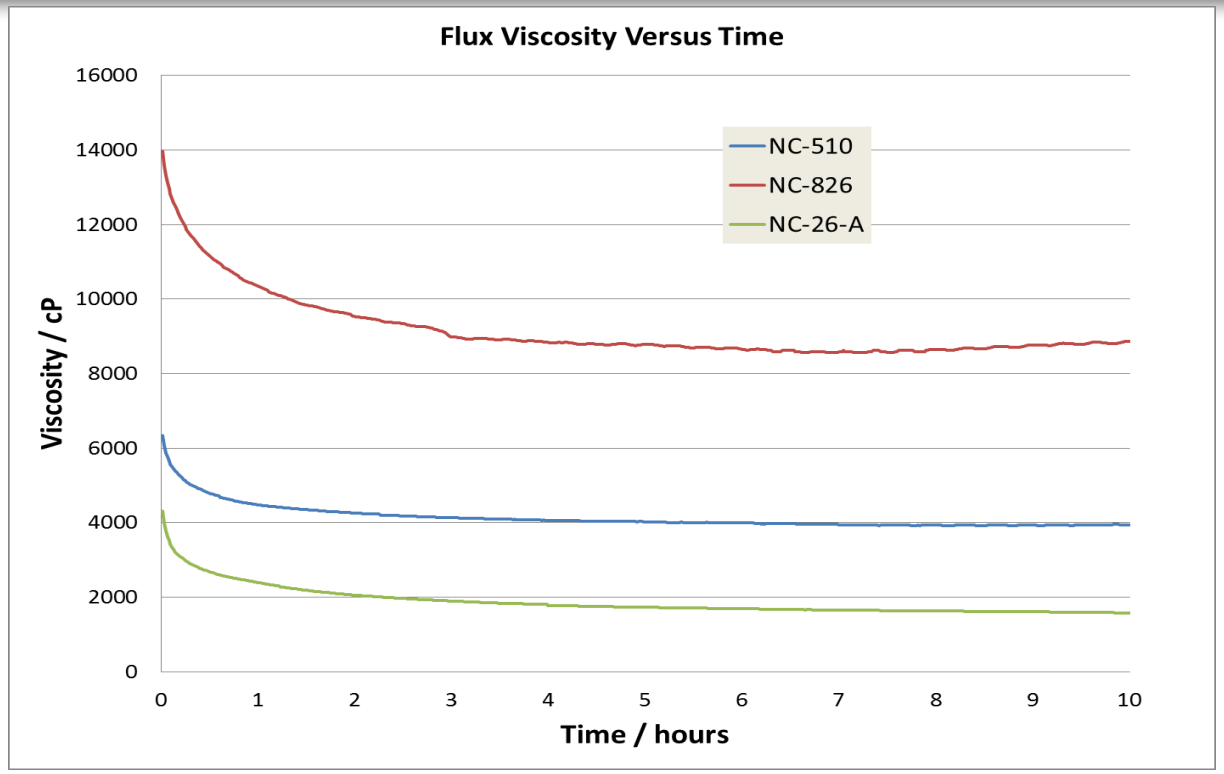
Viscosity Test Method

- **Equipment:**
  - Brookfield Cone and Plate
  - Model: DV3THBCB
- **Parameters:**
  - Spindle: CP-51
  - Temperature: 25°C
  - RPM's: 20 RPM

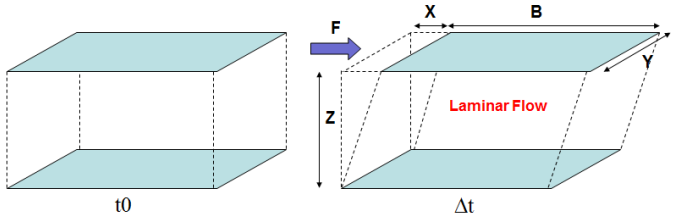




Comparative Viscosities as a Function of Time



Viscosity controls dipping and die-holding during reflow

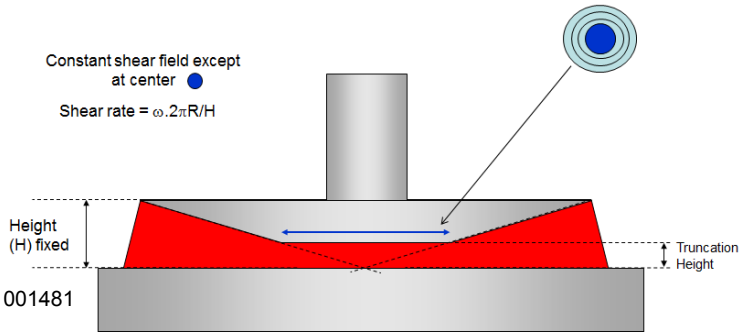


Shear stress $\tau = F / (B.Y)$

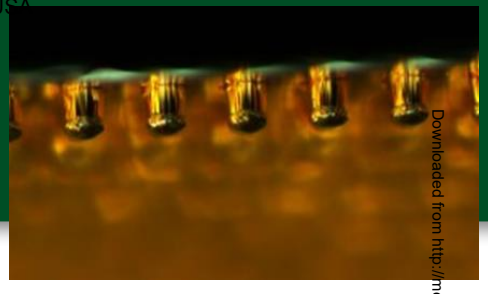
Shear $\gamma = X / Z$

Shear rate $\dot{\gamma} = \Delta\gamma / \Delta t$

Viscosity $\eta = \tau / \dot{\gamma}$ (Shear stress / Shear rate)

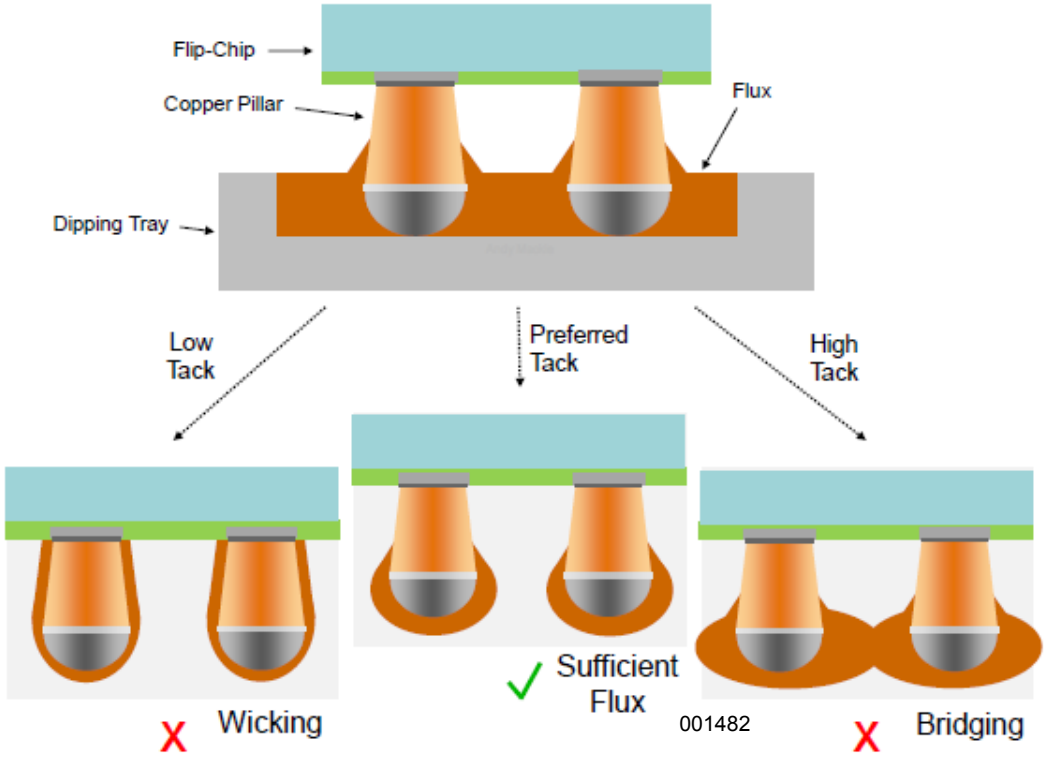


Importance of Rheology for Fine-Pitch Dipping Process



Rheology (viscosity / tack) must be tuned to the process needs, especially for fine pitch, without sacrificing the ability to hold die in place:

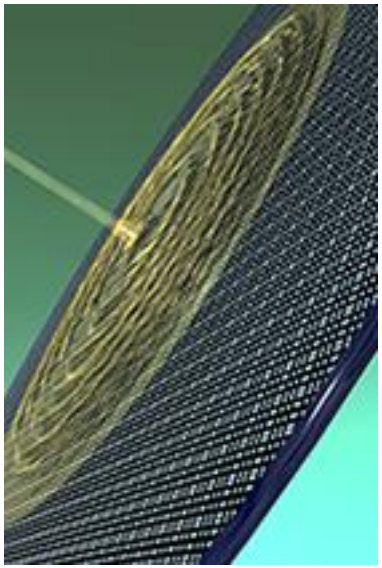
- High viscosity can lead to bridging
- Low viscosity can lead to flux wicking and die-surface contamination



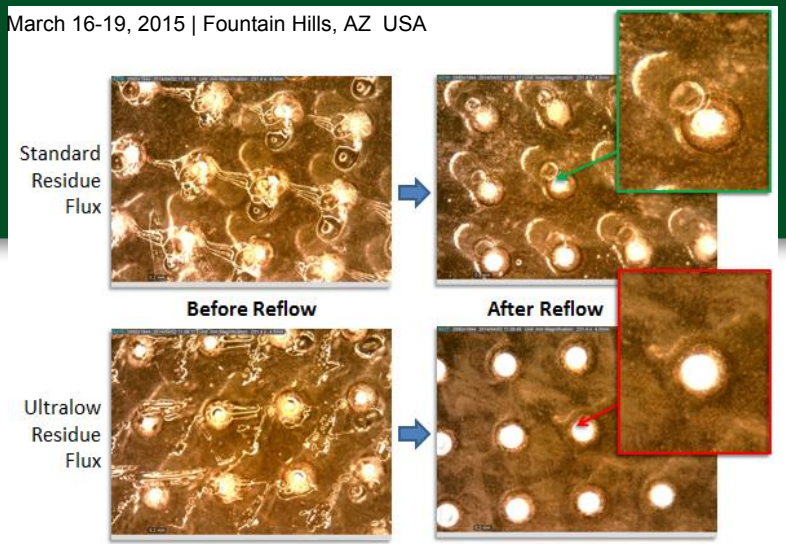
Flux rheology and exact needs will vary with the flip-chip design

Ultralow Residue (ULR) Flip-Chip Flux Characteristics

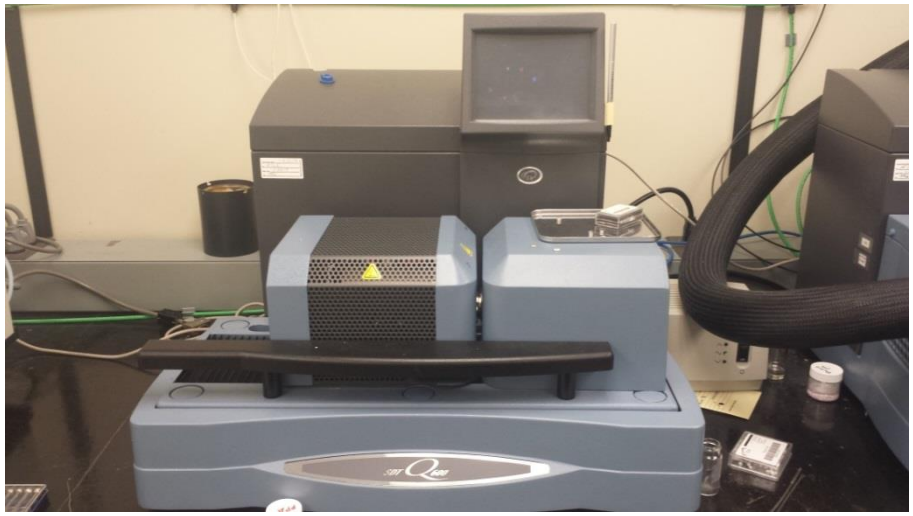
- Rheology
  - Viscosity
- **Residue level**
  - Thermogravimetric analysis (TGA)
- Solderability
  - Wetting
- Holding die in place
  - Movement during reflow (MDR)
- Compatibility with MUF/CUF



TGA Test Method



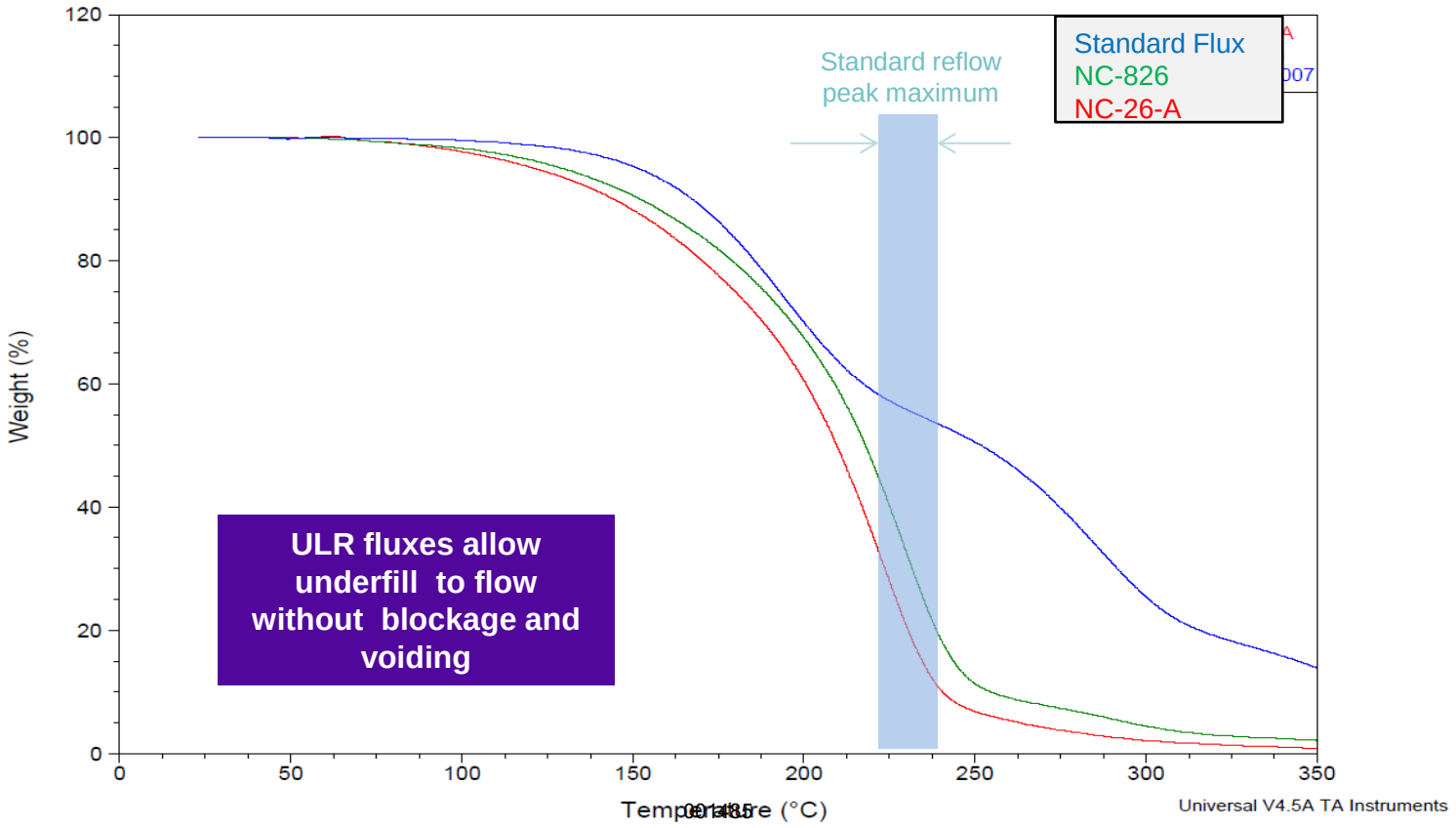
- **Equipment:**
  - TA Instruments SDT Q600
- **Parameters:**
  - Method:
    Ramp 10°C/min
  - Sample size:
    10mg ± 1mg
  - Nitrogen gas:
    100ml/min



TGA is an indicator of relative flux residue levels

TGA: Ultralow Residue (ULR) and Standard Residue Flux Types

TGA is unrepresentative of real situations for flux. The exposed surface area is much smaller in TGA is smaller than for real flip-chip applications. In reality, flip-chip fluxes will have lower residue levels than shown here.



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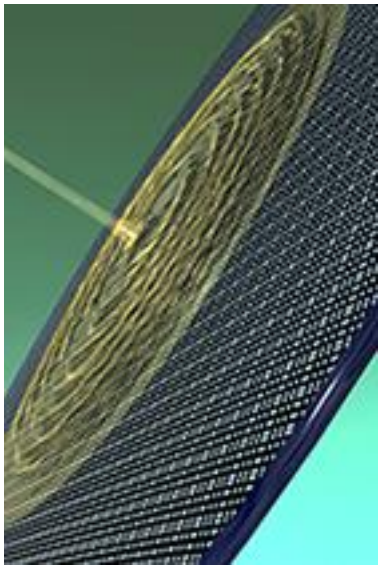
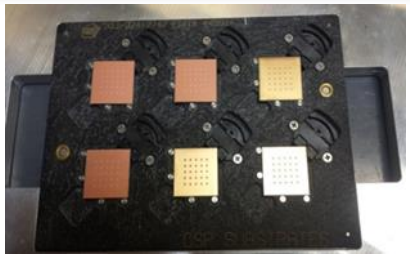
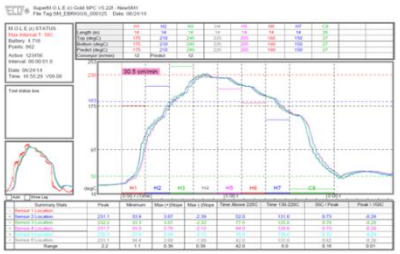


Wetting Test Method

1. Print flux onto metallized surface
2. Place spheres onto flux deposit
3. Reflow in nitrogen
4. Measure reflowed height deposit
5. Calculate percent spread





$$S_R = \frac{D-H}{D} \times 100 \quad \text{(16)}$$

where, S_R : spreading ratio (%)

H : height of the spread solder (mm)

D : diameter of the solder, when it is assumed to be a sphere (mm)

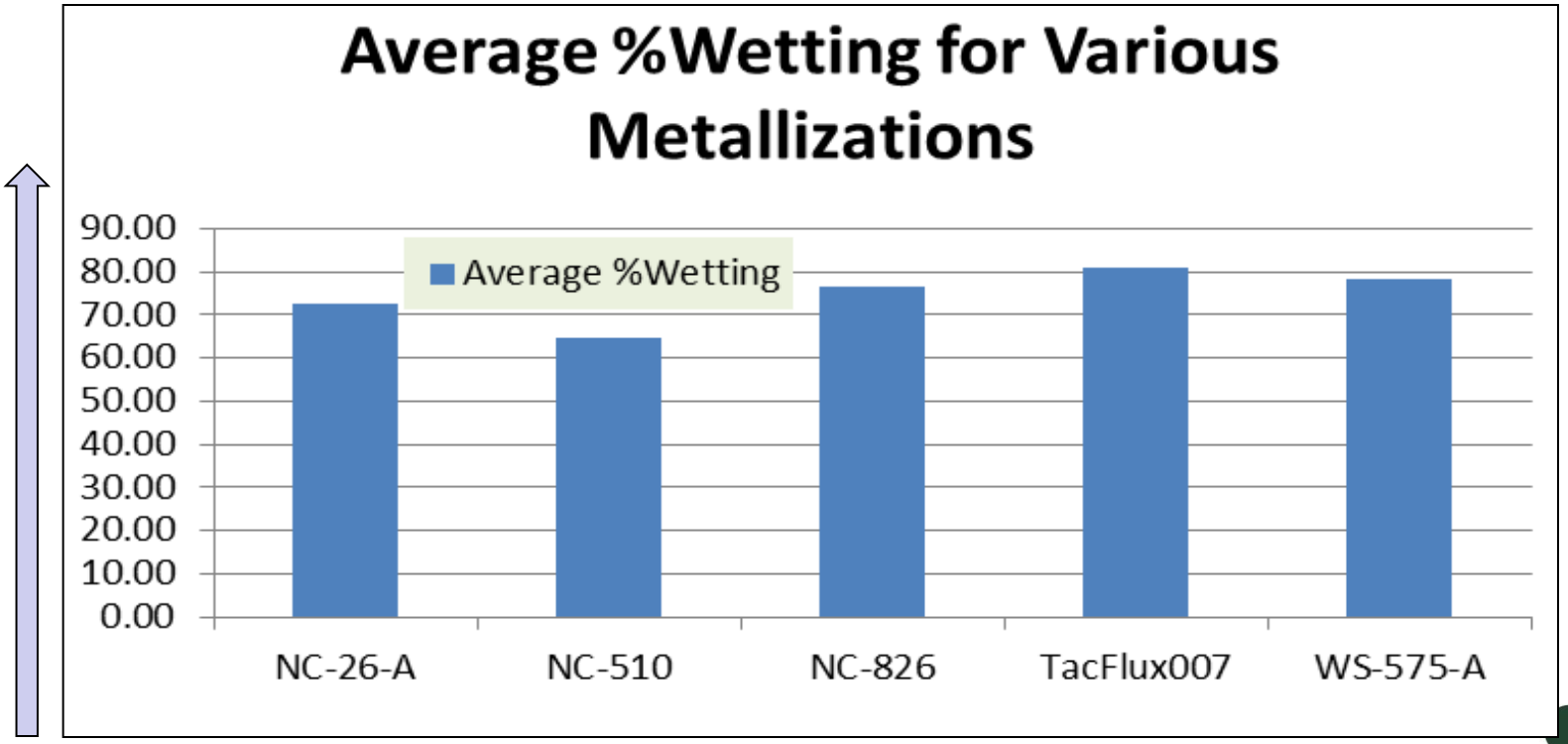
$D = 1.24V^{1/3}$

V : mass[12]/density of tested solder

Wetting Test Comparison

Wetting must be controlled, and balance between

- Excessive: leading to bridging
- Poor: leading to non-wetting or weak solder joints with voids



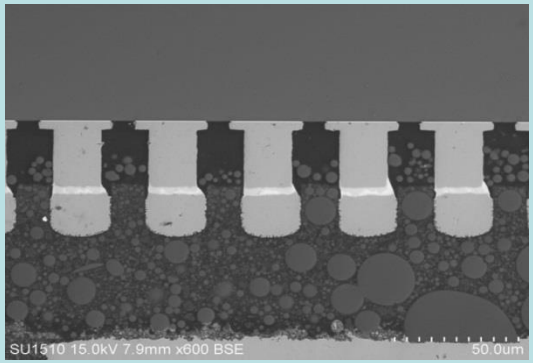
GOOD

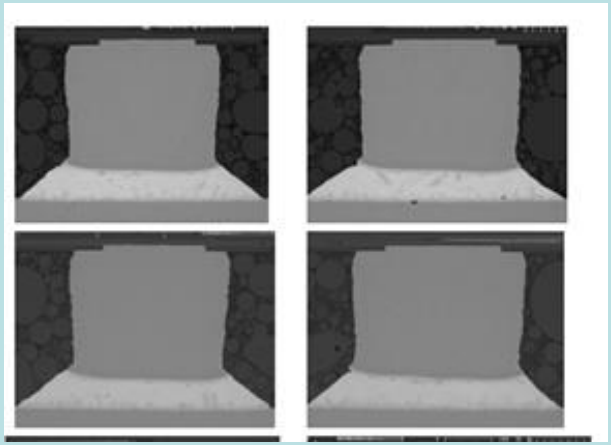
NC-26-A and NC-826 balance wetting onto OSP

INDIUM CORPORATION®

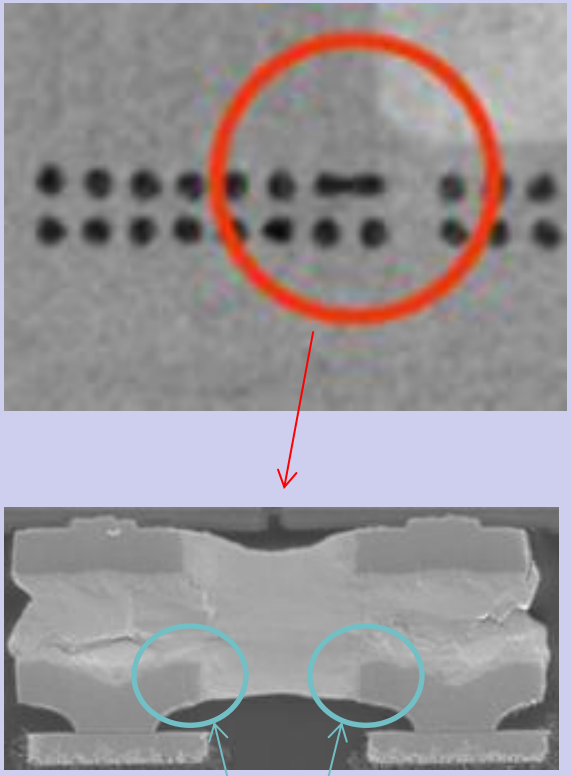
Wetting: Ultralow Residue Fluxes

NC-26-A





Competitor water-soluble (WS) flux



Excessive solderability

NC-26-A shows zero voiding and zero bridging on OSP

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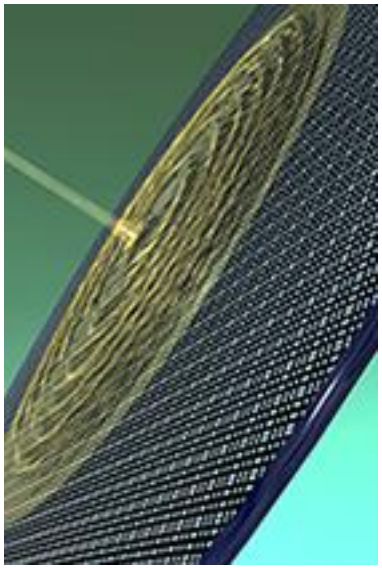
- **Holding die in place**
  - Movement during reflow (MDR)
- Compatibility with MUF/CUF



MDR Test Method

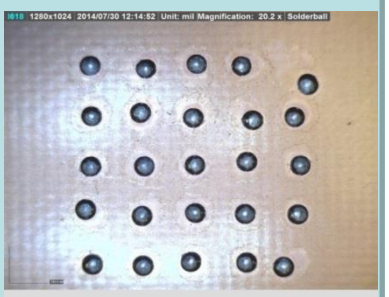
- Correlates with die-skew
- Measure movement of reflowed deposit from original position of sphere
- Calculate amount of movement during reflow
- *For more details, contact Indium Corporation's Technical group*

Good wetting

Good (Low) MDR

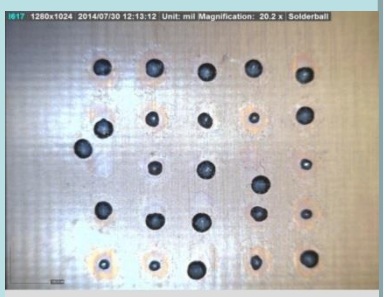
Moderate wetting

Moderate MDR

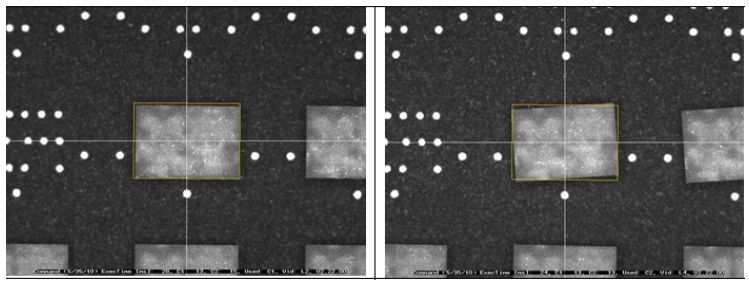


Uneven wetting

Poor (High) MDR



Die skew



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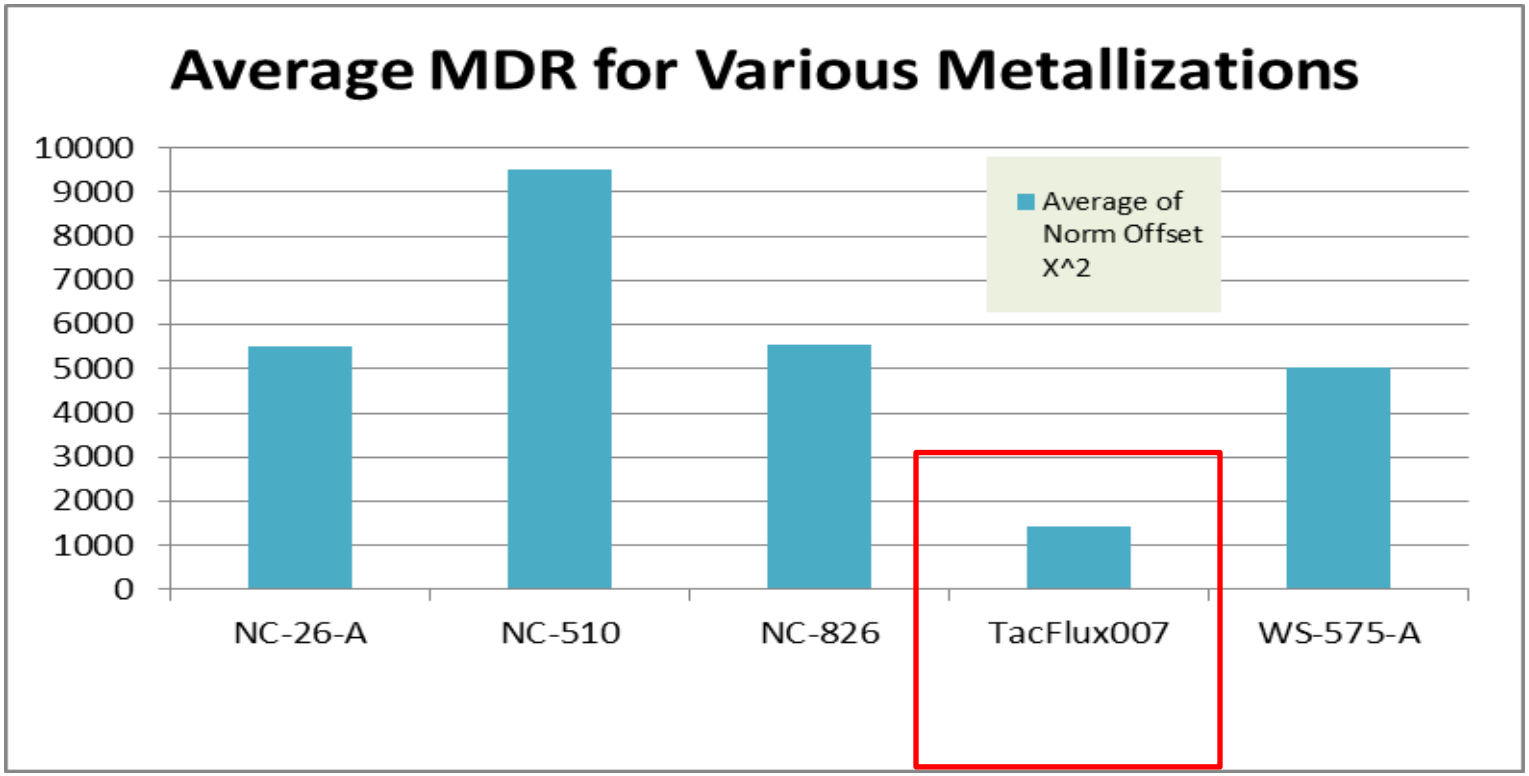
Good Bad

Movement During Reflow (MDR)

GOOD



NC-26-A and NC-826 are comparable to WS flux for die holding

Ultralow Residue (ULR) Flip-Chip Flux Characteristics

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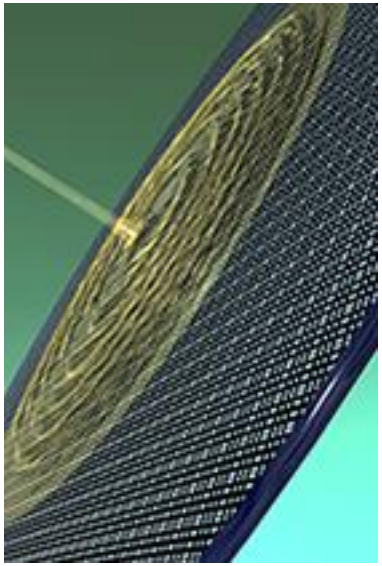
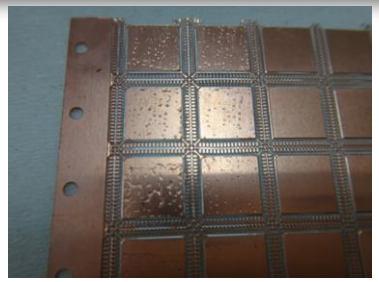
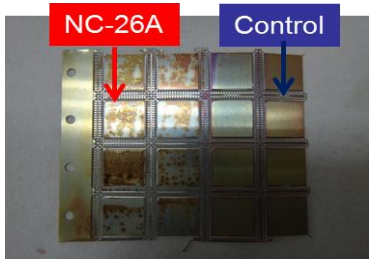
- **Compatibility with MUF/CUF**

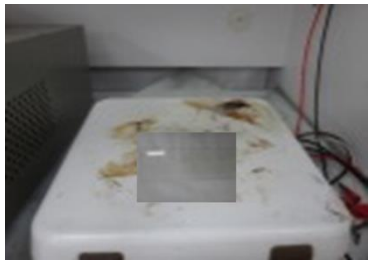


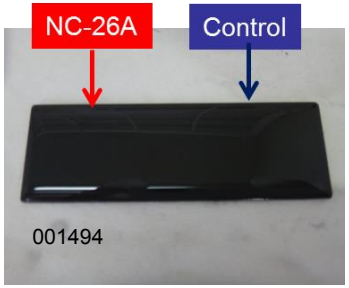
CUF Compatibility: Test Method A

- **Deposit flux on substrate**
  1. Using FC to dip transfer flux onto Cu leadframe
  2. Spread a thin film of flux on glass slide
- **Heat on hot plate @240°C for 10-15sec**
- **Deposit underfill**
- **Cure underfill at recommended condition**
- **Post reflow treatment**
  - Control (no baking)
  - Baking at 180°C for 1hr
  - Baking at 180°C for 3hr
  - 10 temp cycle at 125°C/65°C (dwell time 1.5min)
- **Delamination evaluation**
  1. Visual and Scotch tape for samples on Cu leadframe
  2. Cross-section SEM for sample on glass slide







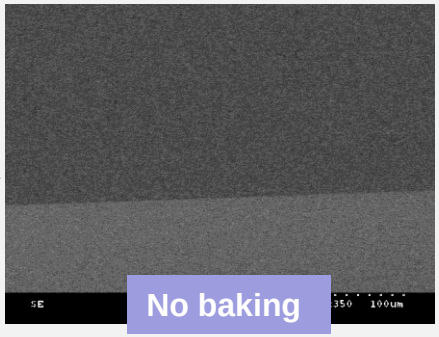


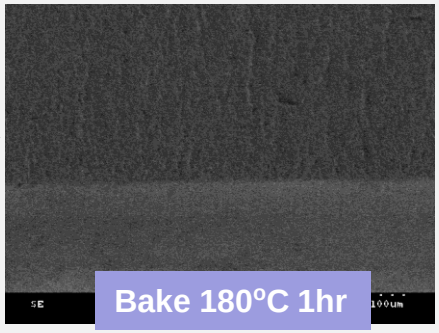
SEM X-section Check on Flux Thin-Film

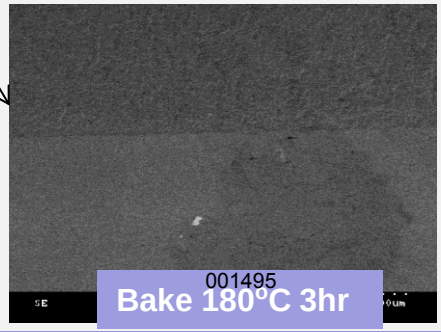
Cut here

NC-26-A has good compatibility and no delamination

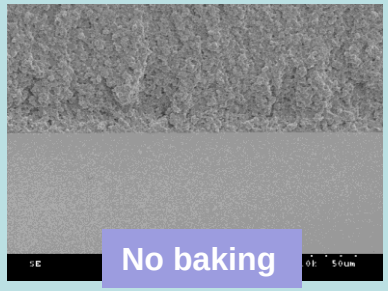
Before thermal cycle

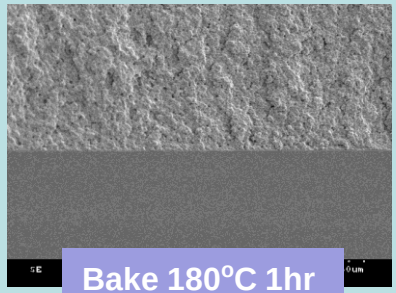


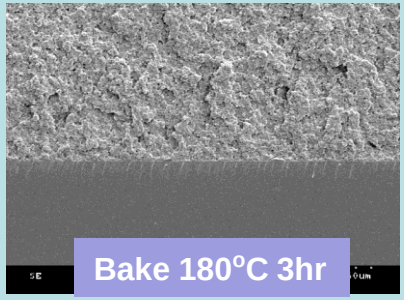




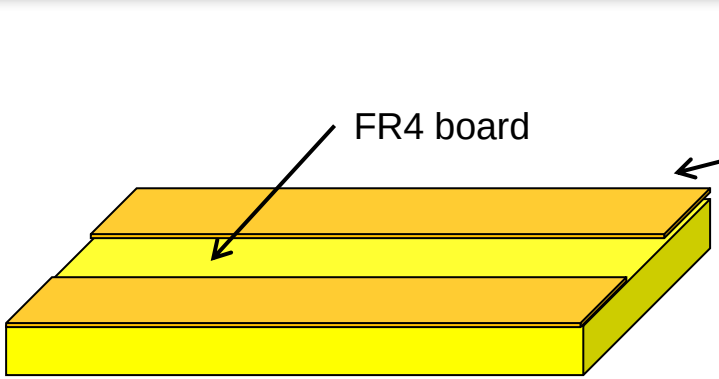
After thermal cycle



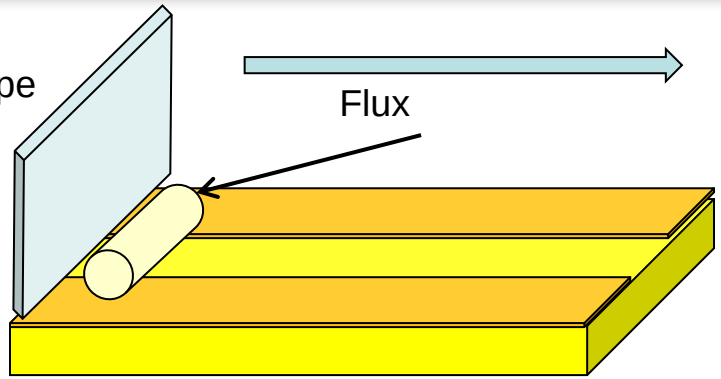




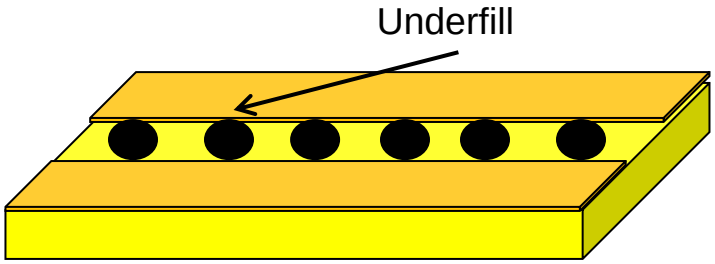
CUF Compatibility: Test Method B



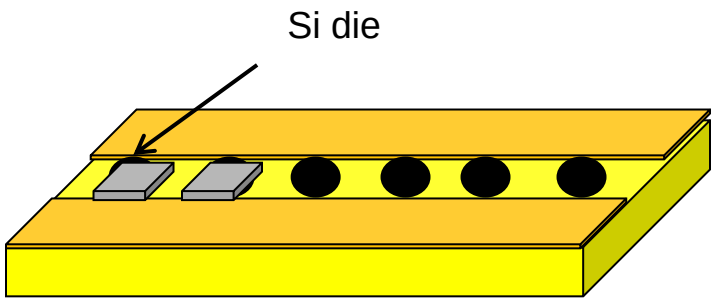
Place Kapton tape on FR4 board



Apply flux and spread it evenly onto the FR4 board then reflow



Apply underfill and spread over reflowed flux



Apply die, cure and then measure shear strength

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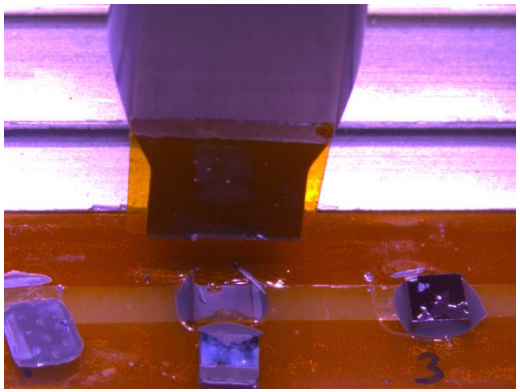
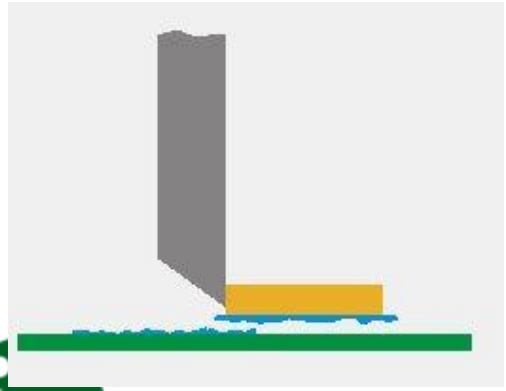
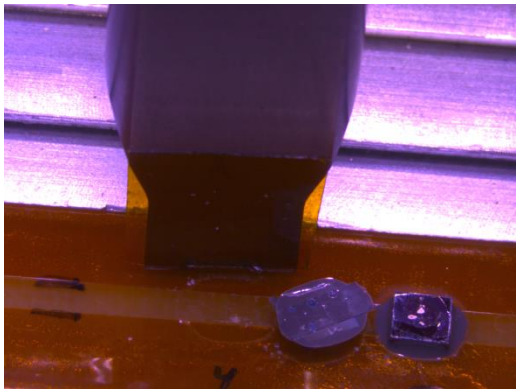
Test Failure Types

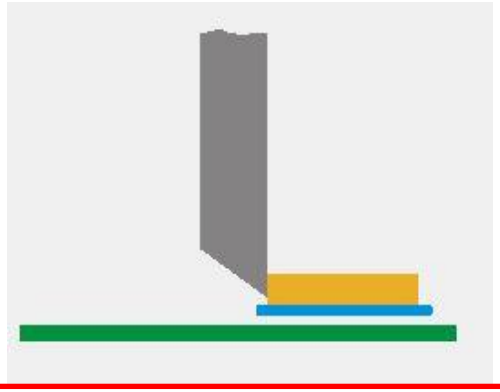


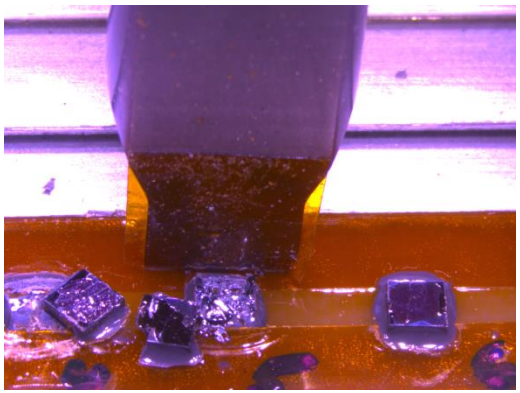
Combination Failure



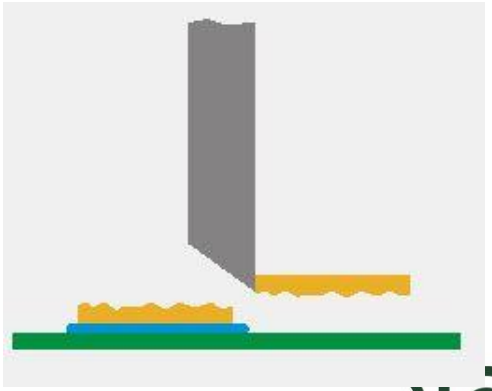


Adhesive Failure

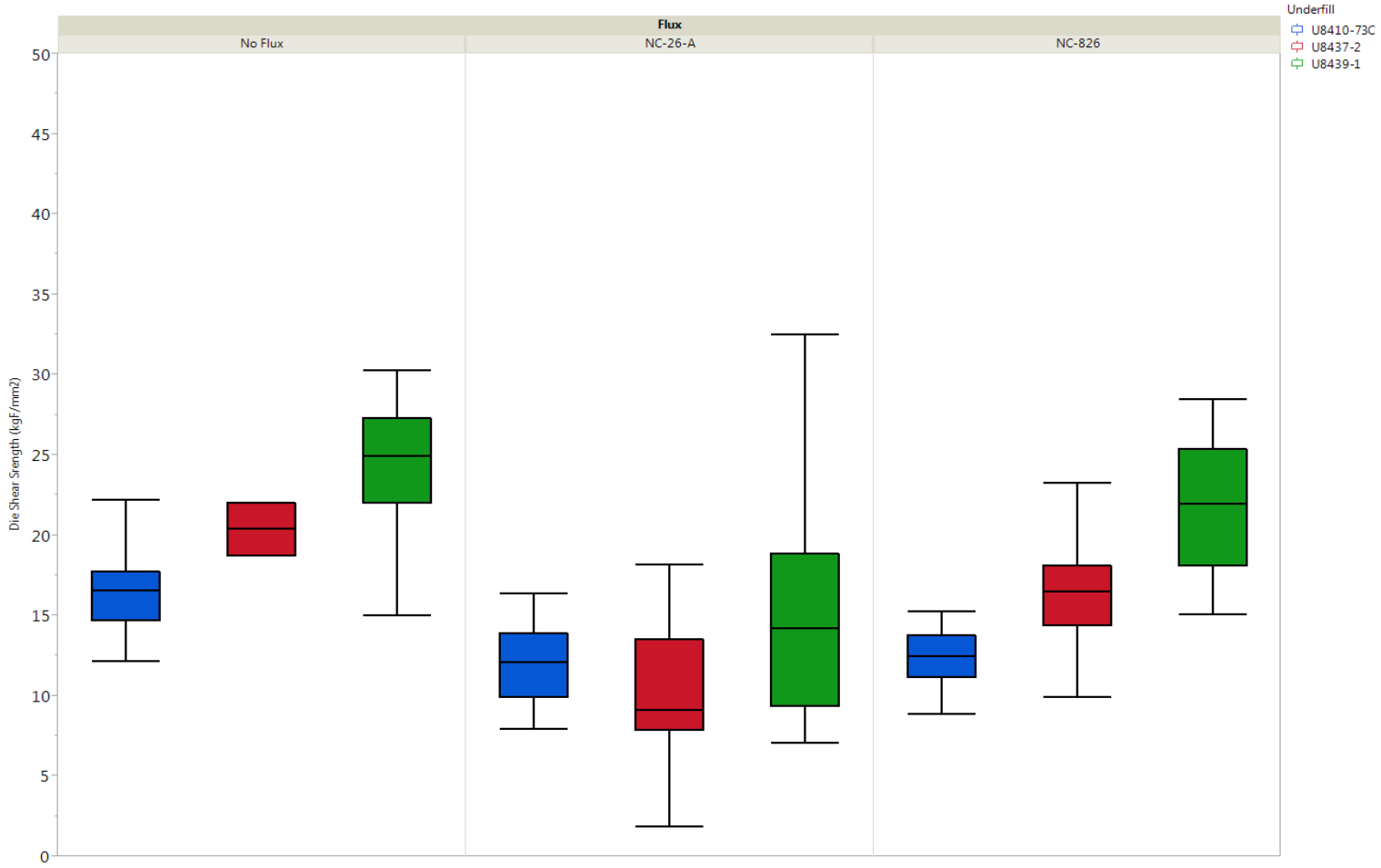




Die Failure



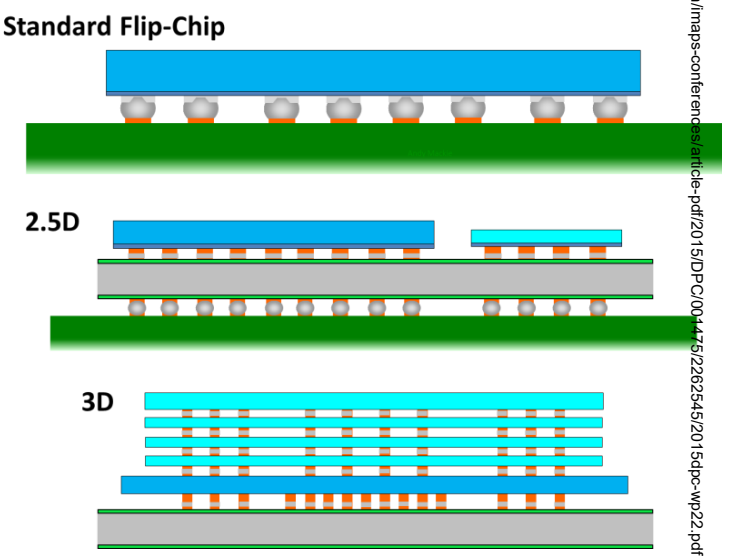
Test Data



*Adhesive failure data only

ULR Flip-Chip Flux Product-Specific Attributes

- High-yield soldering to copper OSP
- Designed for copper-pillar
- Dipping with minimal bridging
- No wetting onto die surface
- Holds large die in place during reflow
- Customer-proven residue compatibility with CUF and MUF without delamination



Indium ultralow residue fluxes are customer-proven in copper pillar flip-chip processes

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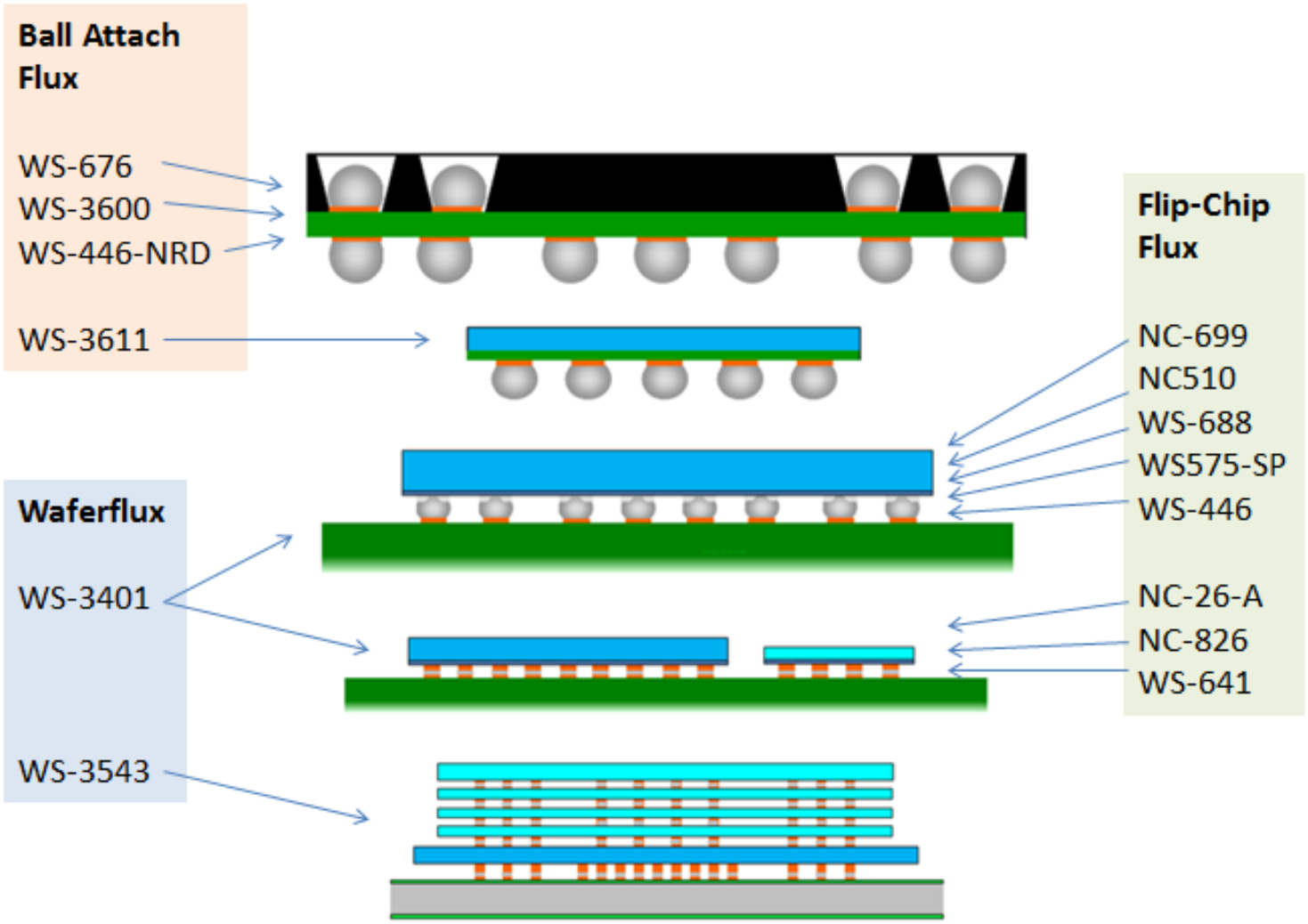
Semiconductor Fluxes: Major Commercial Usage Q3 2014



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Thank you!

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