

CORNING

Advancements in Through Glass Via (TGV) Technology

IMAPS DPC 2015

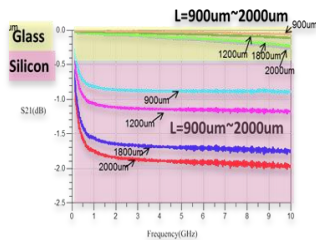
Aric Shorey
Commercial Technology Manager
18 March 2015

Overview

- Advantages provided by glass
 - Provides opportunities for numerous applications
- Current capabilities for via formation
- Update on recent progress in downstream processing of glass interposers – wafers and panels
 - Via fill
 - Reliability/Thermal Cycle Tests
- Summary

Why Glass?

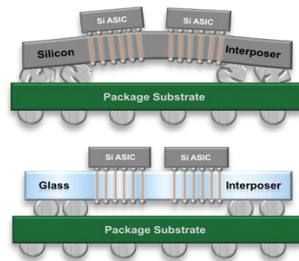
Electrical Properties



Low Electrical Loss

- Improved signal isolation
- Lower power requirement

CTE Adjustability



Capability to deliver multiple CTEs

- Improves reliability
- Si-Match
- Also important in Carrier applications

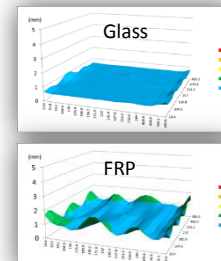
Surface Quality



Enables fine line spacing

- Smaller package size
- Fewer metal layers, resulting in cost savings

Stiffness



Glass is stiffer compared to organics

- Better flatness enables fine line spacing

Form Factor

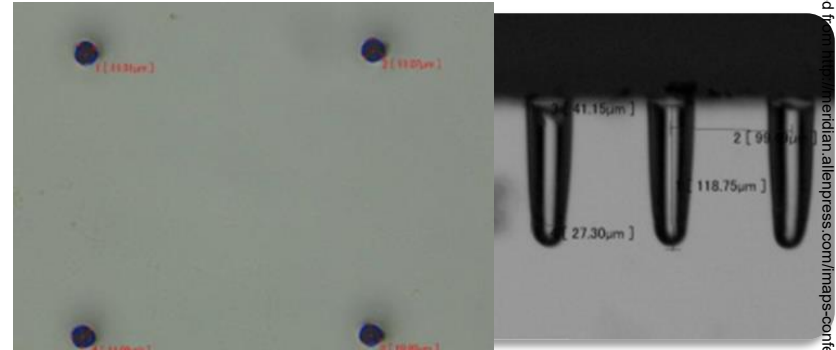


Forming at thickness

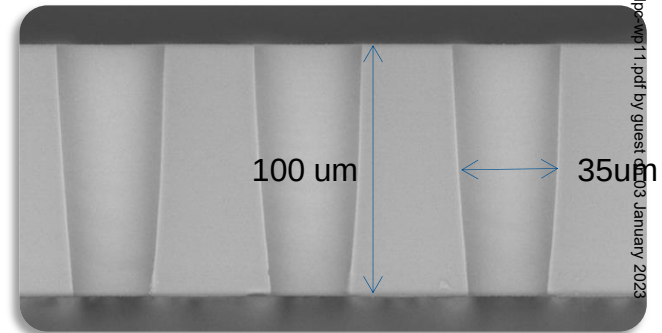
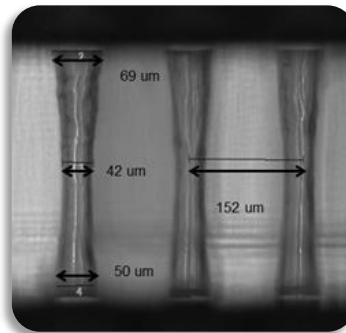
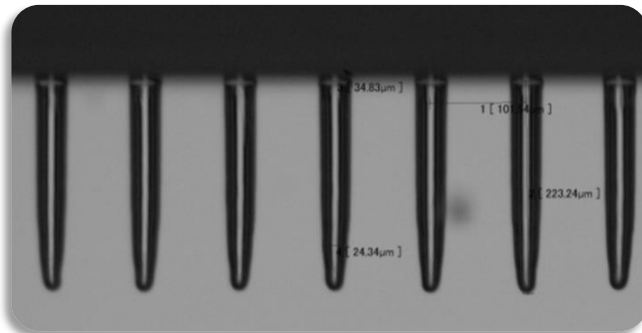
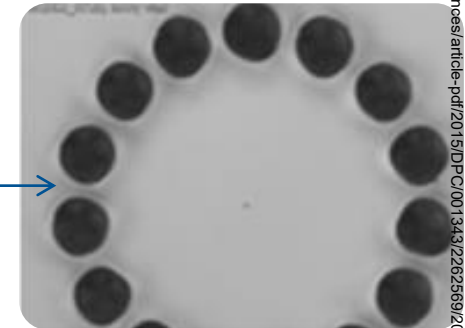
- Better yield/cost (no grind and polish)
- Better quality and efficiency in panels

Corning TGV Current Design Rules

- OD – 25 μ m to 100 μ m $\longrightarrow$ 10 μ m
- Minimum Pitch – 2X OD
- Through and blind holes
- Glass size
 - Wafers 100mm $\longrightarrow$ 300mm wafers
 - Panels > 500mm square
- Thickness
 - 100 μ m $\longrightarrow$ 700 μ m
- Pattern – Flexible – customer x/y locations

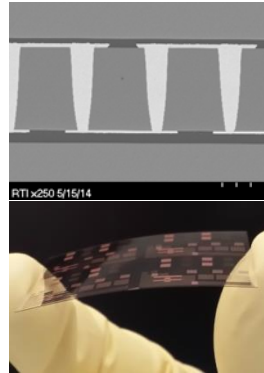


Space
edge to
edge
24um

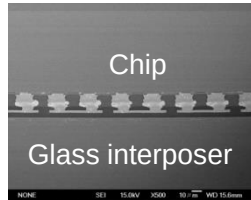


Progress in Metallization and Reliability Testing

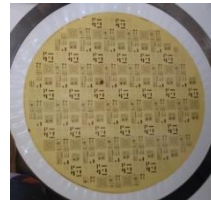
Filled TGV (Electrolytic Plating)



RTI completed glass interposer test die



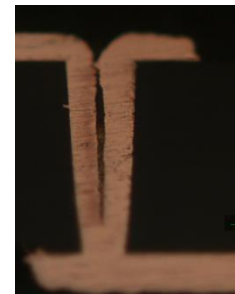
Chip
Glass interposer
ITRI solder μ bump to Cu pillar structures



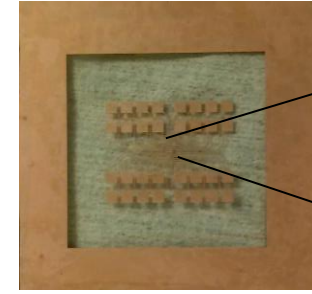
ITRI 300mm glass interposer



Filled TGV (Conformal Plate)



TPV after 1000 thermal cycles

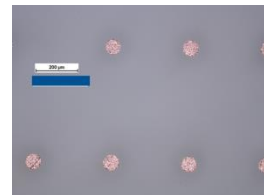


2" Final fabricated test vehicle

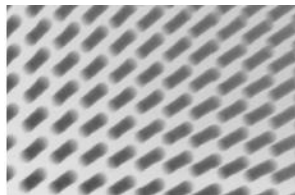
From: Demir et al, "First demonstration of reliable copper-plated 30 μ m diameter through-package-vias in ultra-thin bare glass interposers", ECTC 2014



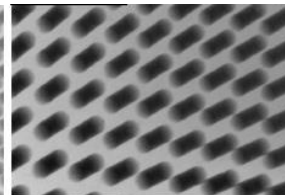
Filled TGV (Paste Filling)



Paste filled TGV
30 μ m via
100 μ m thick



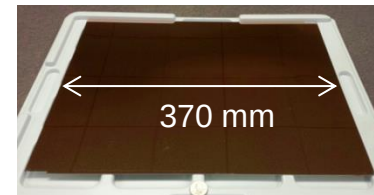
60 μ m via
void free
300 μ m thick glass



80 μ m via
void free
300 μ m thick glass



Fully Filled TGV (Electrolytic Plating)



Sputter coated 370x470mm
(130 μ m thick) with
~100,000 holes



Atotech's double side plating process can fill through holes in panel format with low overburden



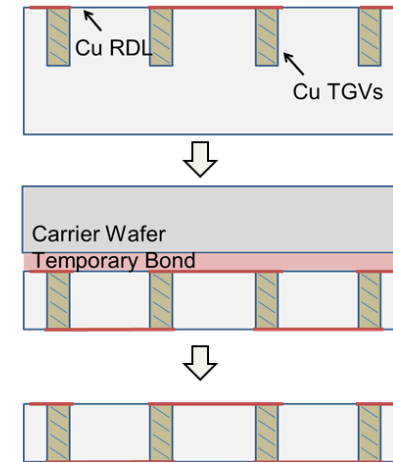
Demonstration and Testing

Blind Vias – Test and Reliability

Glass Interposer Test Lot



- A glass interposer test lot was used to demonstrate Cu via filling in 150 mm glass wafers
- Lot included:
 - SWG3 wafers with CTE of 3 ppm/°C
 - SWG8.5 wafers with CTE of 8.5 ppm/°C
- Fabrication process
 - 35 x 125 μm Cu via filling by electroplating
 - Frontside routing metal
 - Temporary carrier and wafer thinning
 - Backside routing metal
- Testing
 - DC continuity testing of arrays of 400 daisy chained TGVs on glass wafers of each CTE type
 - Thermal cycling wafers of each CTE type

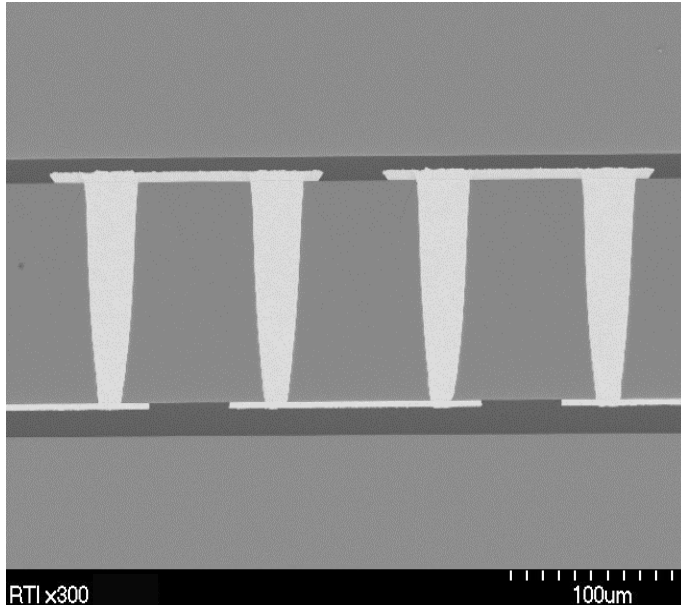


Glass interposer fabrication process

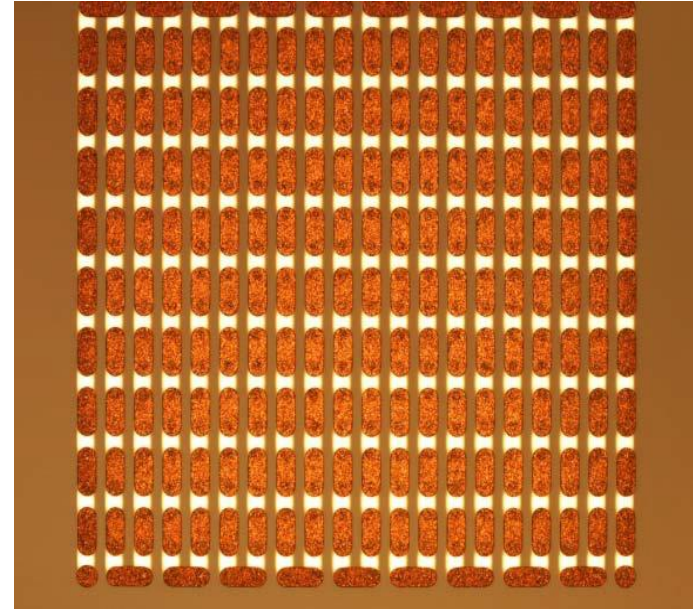


A 125 μm thick glass interposer test die

Thermal cycle testing

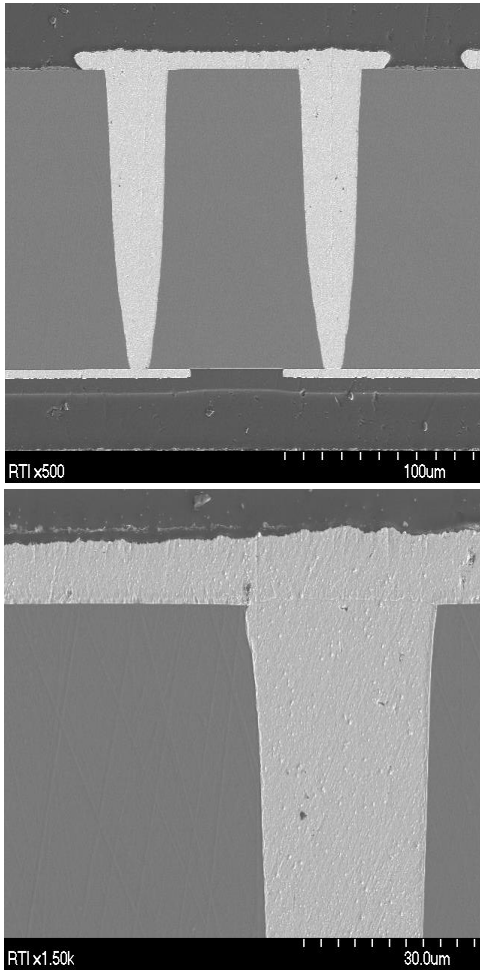


Cross section SEM image from a glass interposer test wafer, SGW3, before thermal cycle testing

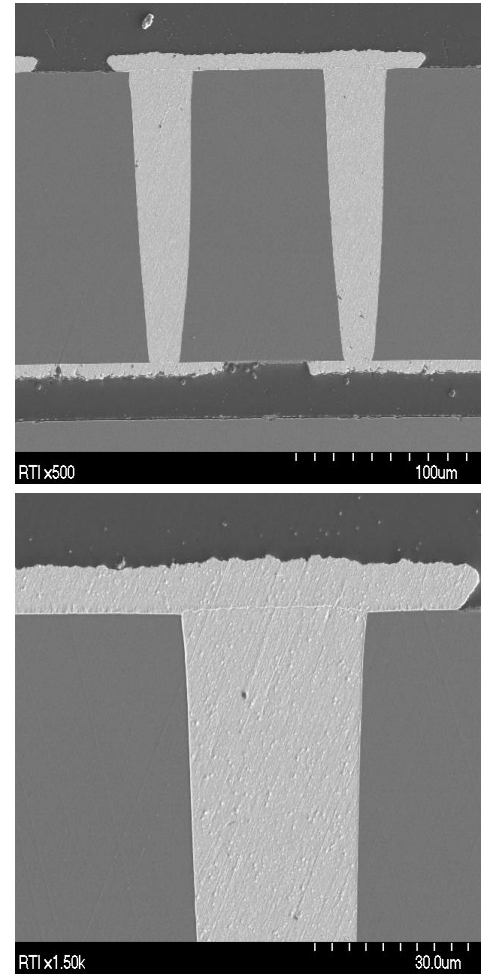


Optical microscope image of a 20 x 20 TGV daisy chain from a glass interposer test wafer, SGW3, before thermal cycle testing

1000 thermal cycles



SGW3



SGW8

Electrical Testing

1000 thermal cycles



Electrical test results taken from two SGW3 and two SGW8.5 wafers after completion of glass interposer test lot

Wafer	CTE (ppm/°C)	No. of 20x20 arrays tested	Yield of TGVs & routing metal (%)
SGW3 - Wafer 1	3	8	99.97
SGW3 - Wafer 2	3	8	99.97
SGW8 - Wafer 1	8.5	8	99.72
SGW8 - Wafer 2	8.5	8	100.00

Electrical test results taken from one SGW3 wafer and one SGW8.5 wafer before and after 500 and 1000 thermal cycles from -40 to 125 C

No. of thermal cycles	Wafer	CTE (ppm/°C)	Yield of TGVs & routing metal (%)	Median chain resistance (Ω)
0 cycles	SGW3-Wafer 1	3.2	100.00	10.4
	SGW8.5-Wafer 2	8.5	100.00	6.7
500 cycles	SGW3-Wafer 1	3.2	100.00	15.4
	SGW8.5-Wafer 2	8.5	100.00	13.5
1000 cycles	SGW3-Wafer 1	3.2	100.00	16.6
	SGW8.5-Wafer 2	8.5	100.00	15.9

Biased HAST Testing

Substrate types for HAST

SGW3

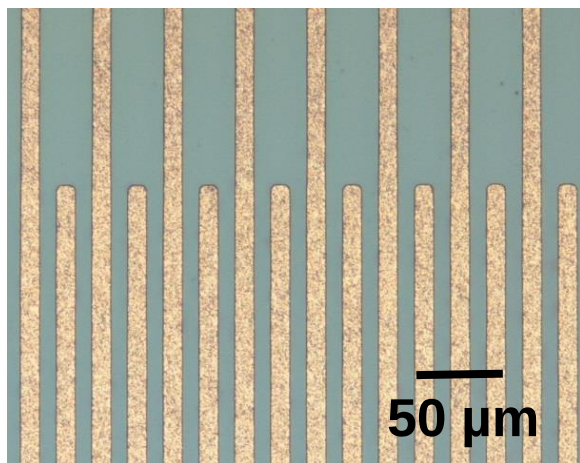
SGW8.5

SGW8.5 with 1 μm PECVD Si_3N_4

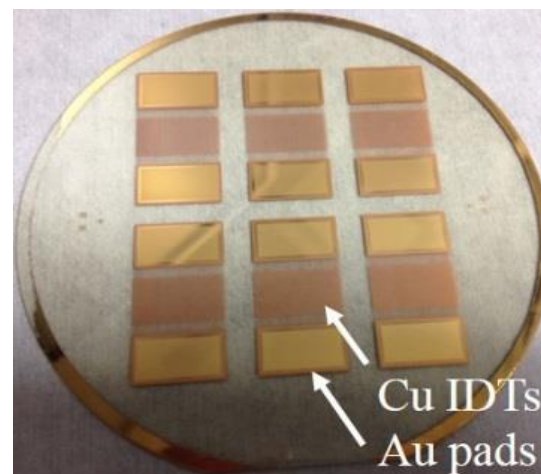
Fused silica

Si / 3kÅ thermal SiO_2

- 400 fingers on 10 μm L/S
 - Ti seed layer, plated Cu
- +/- 5V
- 130 C, 85% Humidity, 96 hours

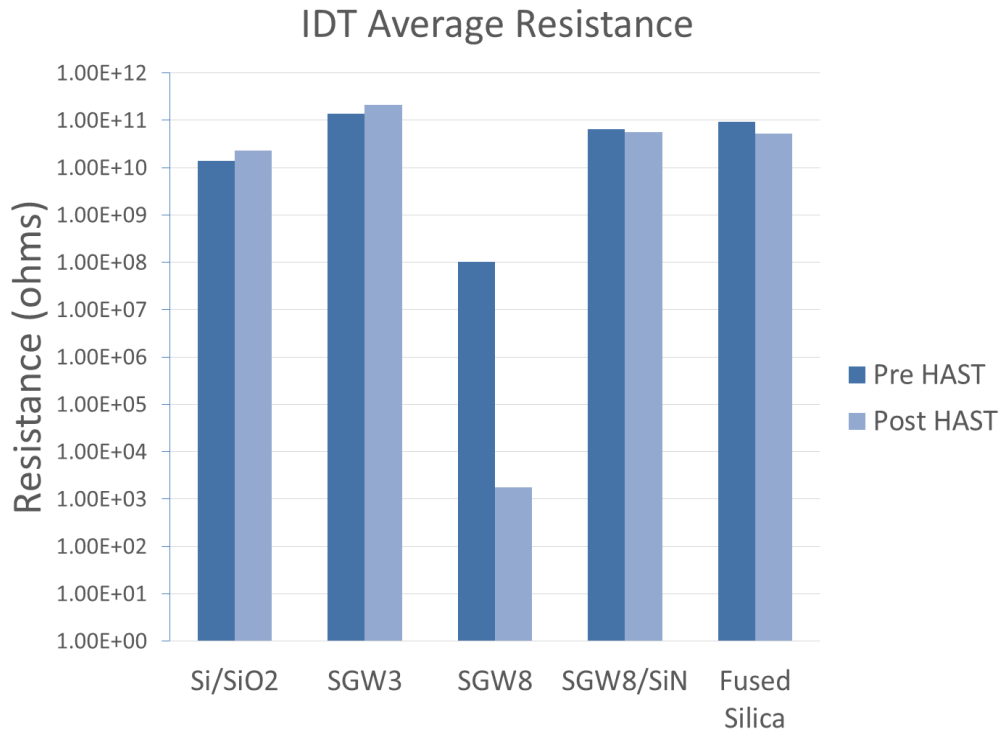


Design



Wafer

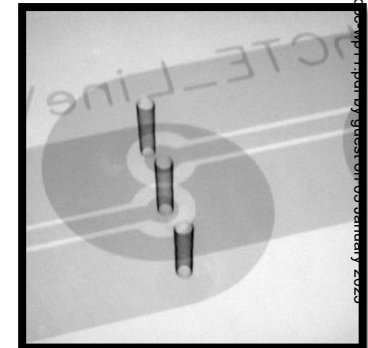
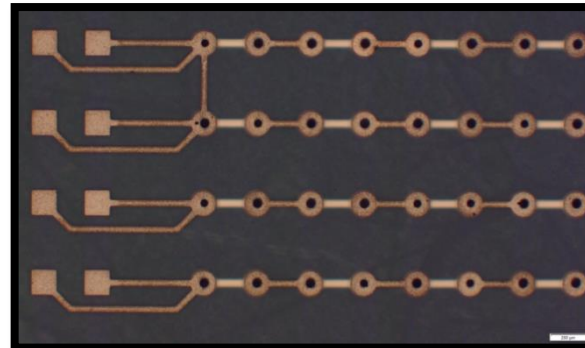
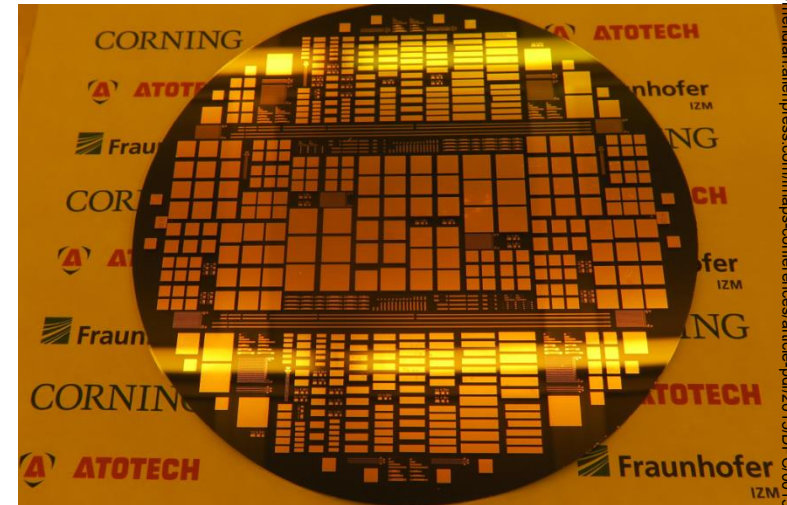
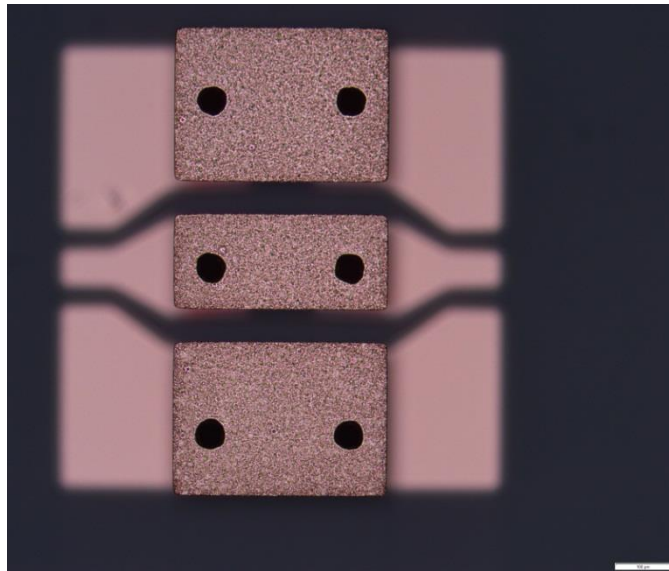
Biased HAST Testing



- SGW3 performed very well
- High CTE glass showed reduction in resistance
- SEMs show migration of Cu under conductor
- Si₃N₄ provided effective barrier layer eliminating migration
- SGW8.5 + Si₃N₄ performed very well

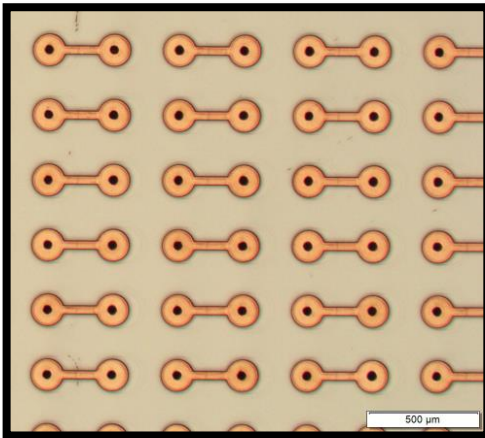
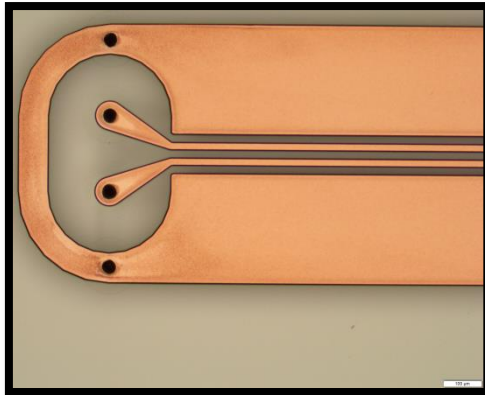
Metallization and Electrical Characterization

- Collaboration with both Atotech and Fraunhofer IZM to metallize glass with TGV
- Both SGW3 and SGW8.5
- Used Atotech's new adhesion promoter Vitrocoat GI
- 7 μm L/S Cu on both sides



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Characterization of Glass Parameters to 70 GHz



Frequency (GHz)	Relative Permittivity	Loss Tangent
0.1GHz	5.28	2×10^{-3}
1GHz	5.30	2×10^{-3}
2.5GHz	5.18	4×10^{-3}
10GHz	5.14	8×10^{-3}
15GHz	5.14	8×10^{-3}
24GHz	5.14	9×10^{-3}
60GHz	5.11	11×10^{-3}
70GHz	5.11	13×10^{-3}

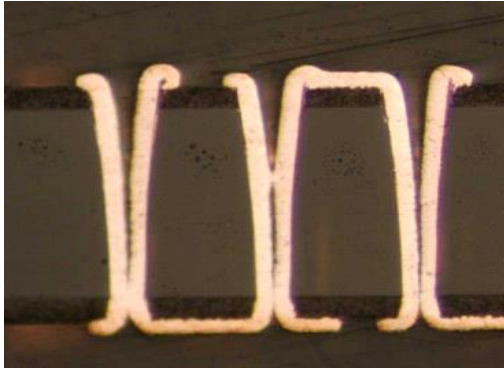
- Fraunhofer IZM has completed characterization of glass up to 70 GHz
- Results reported here are for SGW3
- Will have SGW8.5 soon

Failure Analysis

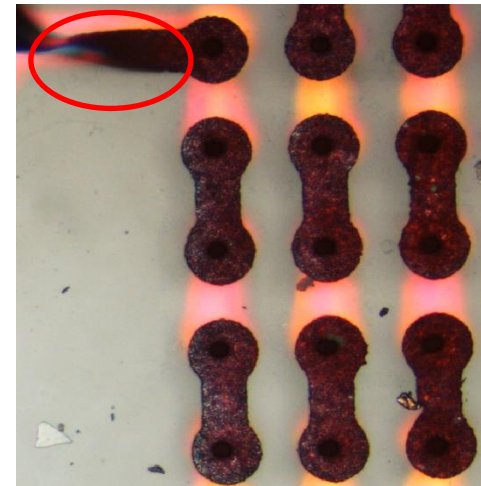
Survived 3000 thermal cycles



Georgia Institute
of Technology



TPV after 1000 thermal cycles



Delamination of copper line

- ❑ All of Daisy chains passed 1000 thermal cycles without any change in resistance
 - ❑ **Latest data up to 3000 cycles**
- ❑ 3 out of 20 TPV chains showed delamination of RDL line
 - No delamination of copper from TPV side wall was observed.
 - Adhesion of copper to bare glass surface is under investigation.

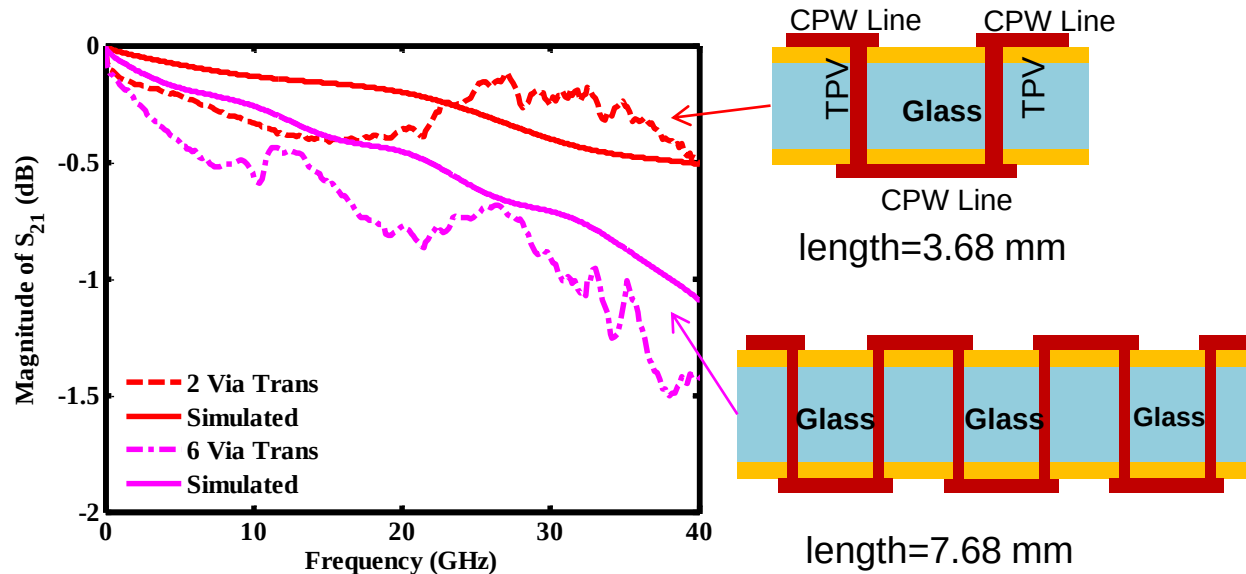
Interactive Presentation ECTC 2014: Adhesion and Reliability of Direct Metallization to Glass Interposers with TPVs -- Mr. Timothy Huang

From: Demir et al, "First demonstration of reliable copper-plated 30 μ m diameter through-package-vias in ultra-thin bare glass interposers", ECTC 2014

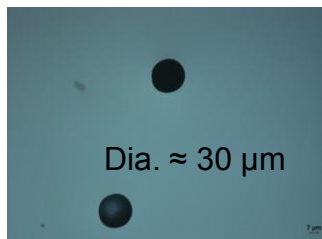
Highly Reliable Through Vias in Glass after Thermal Shock



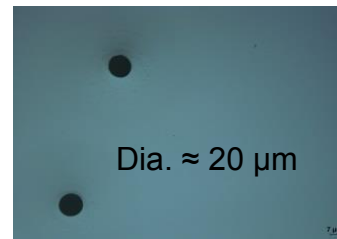
Georgia Institute of Technology



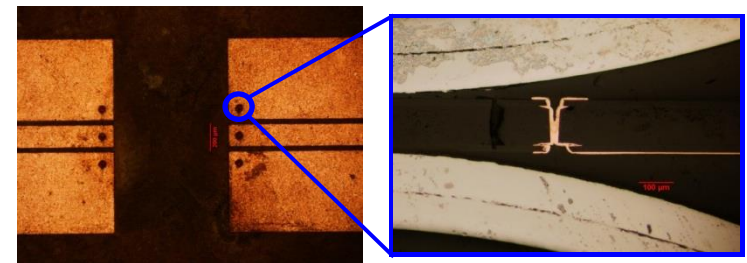
- Stable performance of TGVs up to 40 GHz
- Maximum spread in measurements about 5.6%
- No significant performance degeneration after 1000 thermal shock testing (-55C to 125C)



Entrance



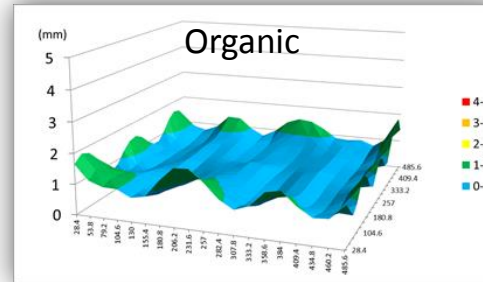
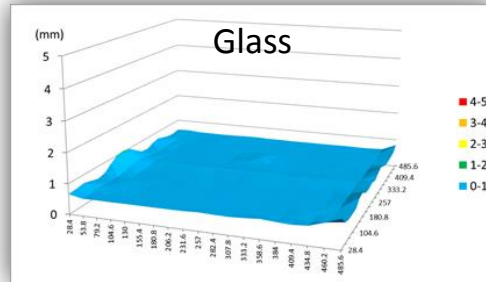
Exit



CPW-TGV Transitions

Advantages of Glass Core Substrate

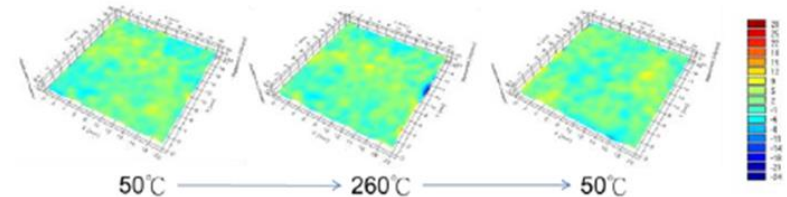
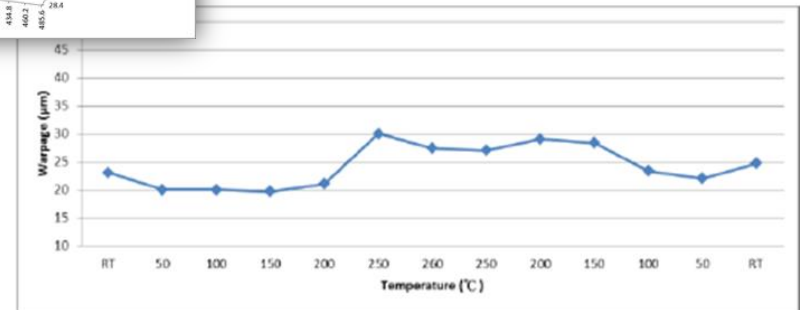
Increased stiffness and ability to adjust CTE



(left) Warpage measurement result of glass substrate after 2 layers build-up
(right) warpage measurement result of organic substrate after build-up layer 2



508 x 508mm glass panel

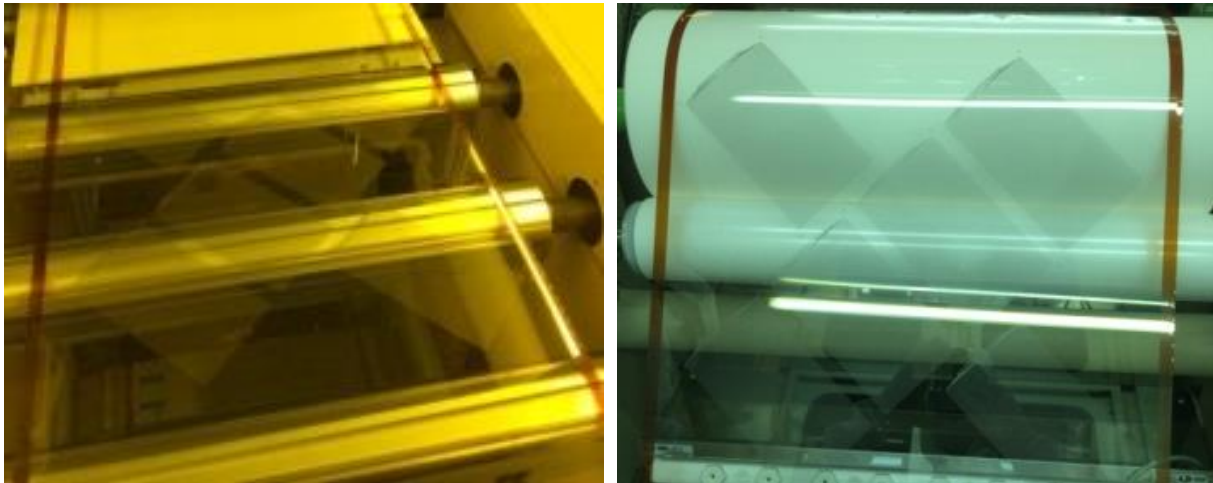


Targeted CTE of glass improves reliability of package (20x20mm)

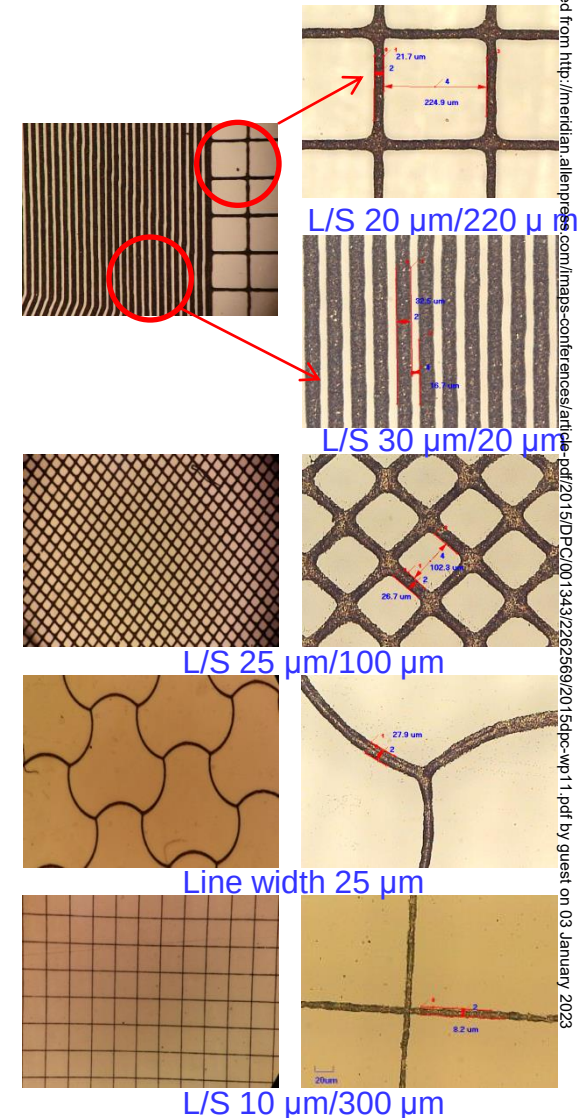
Source: YH Chen et al., Unimicron Technology Corp., Qualcomm Technologies, Inc., Corning Incorporated, "Low Cost Glass Interposer Development", 47th International Symposium on Microelectronics, San Diego 2014.

Corning® Willow® Glass and Roll to Roll (R2R) Processing R2R Electronics Patterning

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- Demonstrated R2R Gravure-Offset Printing on Flexible Glass
 - Ag-ink metal mesh structures printed on glass web and sheets
- R2R Photolithography



Summary and Next Steps

- Corning will continue to develop TGV process, enhanced quality and capacity
- See application in RF, interposer/substrate and others
- The value of glass and ability to leverage industry process and equipment to enable cost-effective, reliable glass solutions continues to be demonstrated
- Continue to mature supply chain and demonstrate reliable performance
 - Metallization
 - Handling (bare glass and carriers)
 - Performance – Electrical and mechanical
 - Reliability – Electrical, mechanical, thermal, chemistry

Acknowledgements

- Atotech Deutschland GmbH
- CAMM/Binghamton University
- DuPont Microelectronics
- Fraunhofer IZM
- Georgia Tech Packaging Research Center
- i3 Electronics
- Industrial Technology Research Institute (ITRI) Taiwan
- RTI International
- Rudolph Technologies

THANK YOU!

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