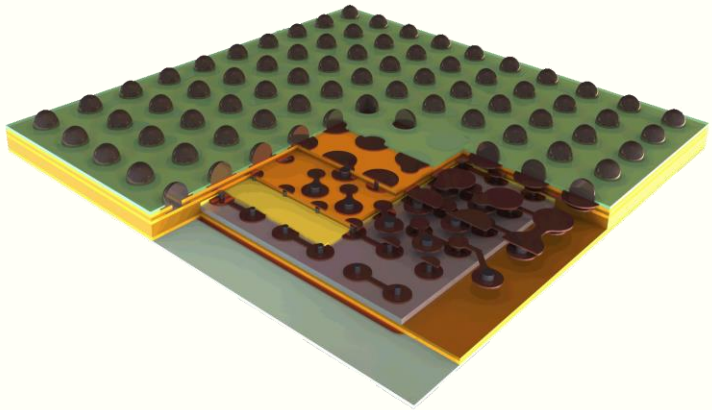
FlipChip International

Miniaturization through Innovation



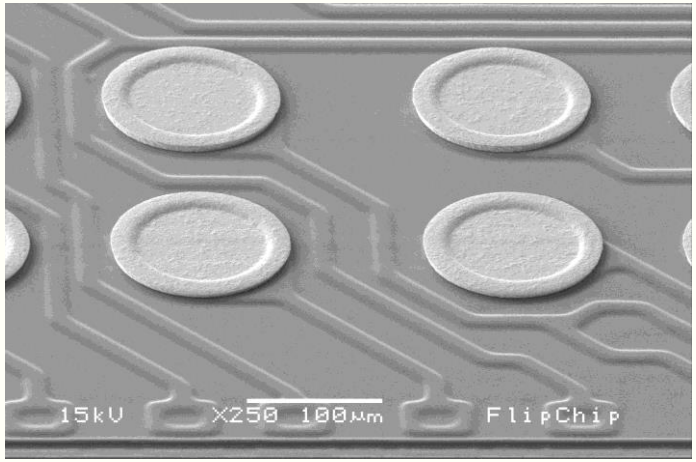
Electroplating with Dielectric Bridges

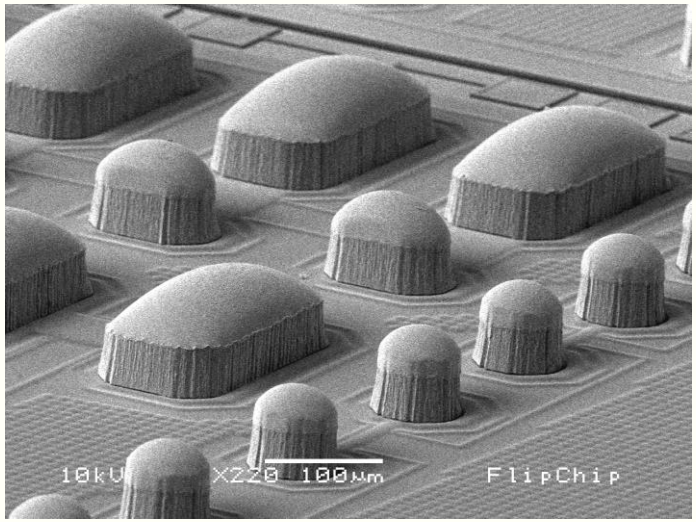
Gene Stout, Anthony Curtis, Guy Burgess, and Theodore G. Tessier

March 17, 2015

Overview

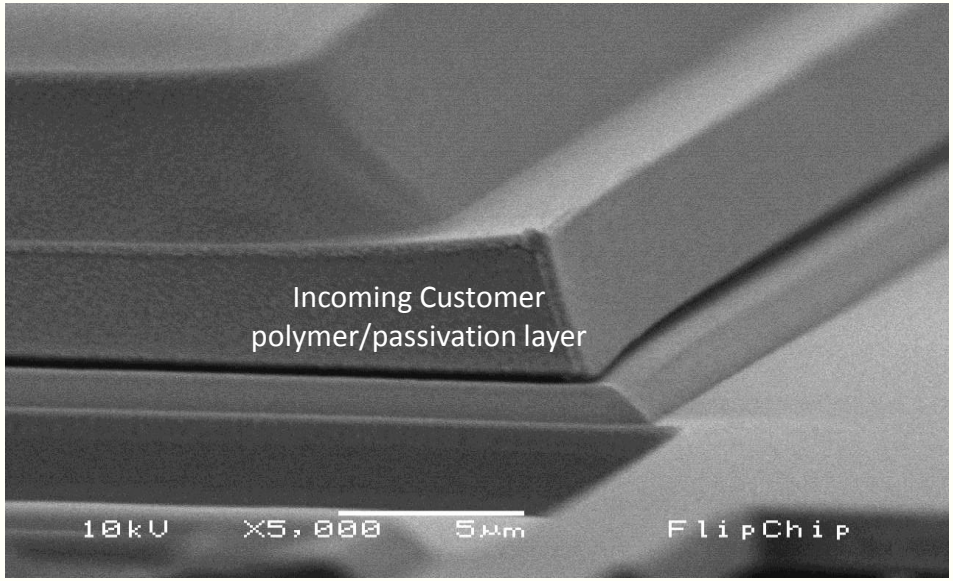
- **Electroplated Copper Bumping technologies are now standard and enable advanced packaging options:**
  - Copper Pillar
  - WLCSP/ WLCSP RDL
  - Flip chip/ Flip chip RDL
  - TSVs
- **Electroplated Copper facilitates:**
  - Enhanced Reliability
  - Smaller Pitches/Smaller Die area
  - Tighter lines and spaces
- **Electroplated copper relies on seed layer continuity for uniform plating across a wafer.**





Overview

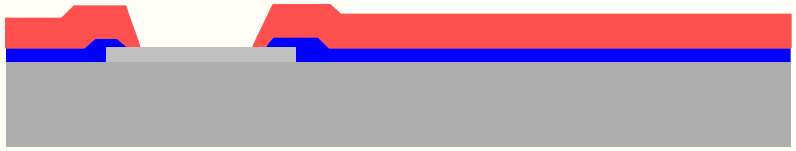
- **Integrating front end fab structures with topography for copper plated bumping can be challenging.**
  - Overhangs
  - Vertical Gaps
  - Trenches
  - Retrograde angles
  - Lifting Passivation layers



- **FCI has developed a patent-pending solution to incoming topography-related electroplating issues.**

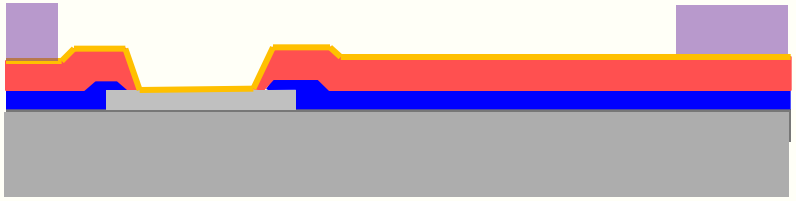
Electrodeposited Copper Processing

1. Incoming



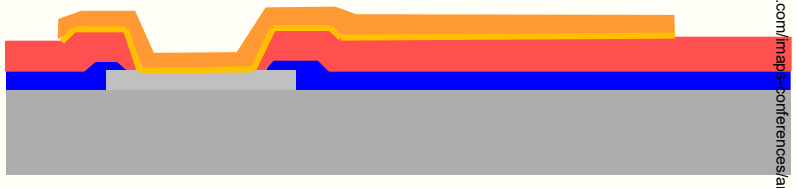
2. Dielectric-1 Coat & Patterning

3. Sputtered Seed Layer Deposition



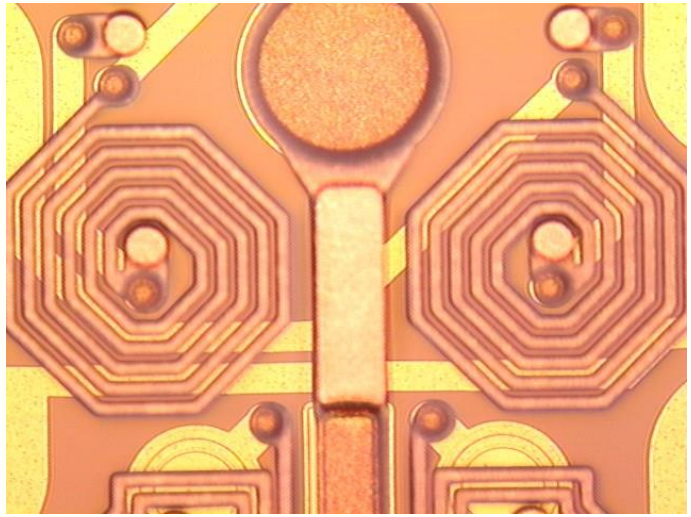
4. Plating Resist Deposition & Patterning

5. RDL Cu Electroplating



6. Resist Strip & Seed Layer Etch

Copper Plated RDL – Example of an Inductor:



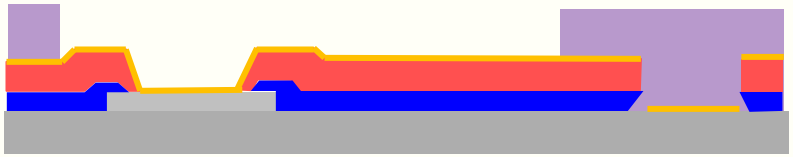
Copper Processing With a Die Edge Undercut

Without Dielectric Bridge

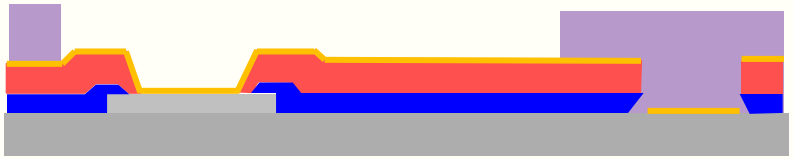
1. Incoming

2. Dielectric-1 Coat & Patterning

3. Sputtered Seed Layer Deposition



4. Plating Resist Deposition & Patterning



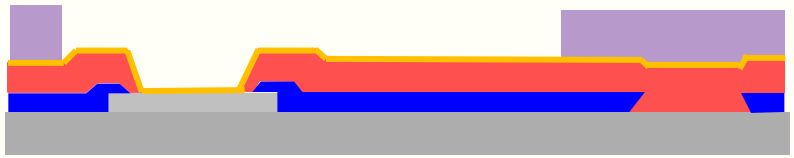
5. Failed Cu Electroplating

With Dielectric Bridge

1. Incoming

2. Dielectric-1 Coat & Patterning

3. Sputtered Seed Layer Deposition

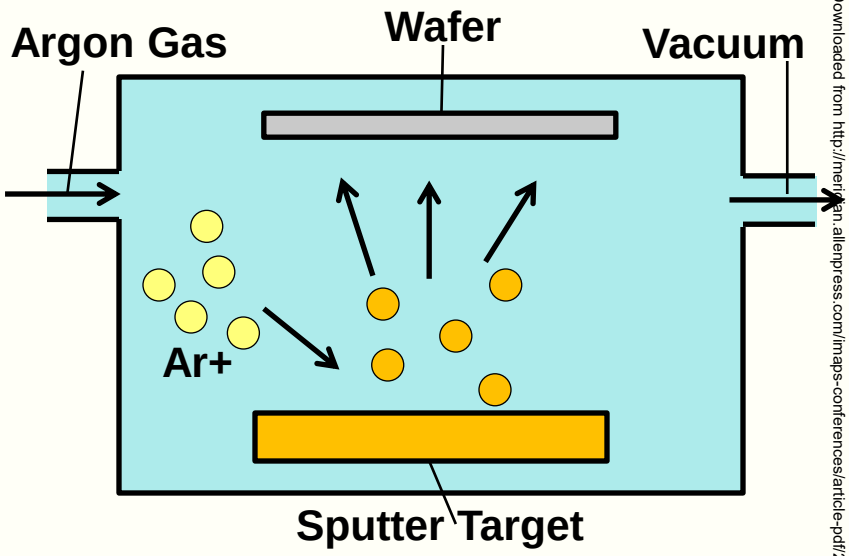


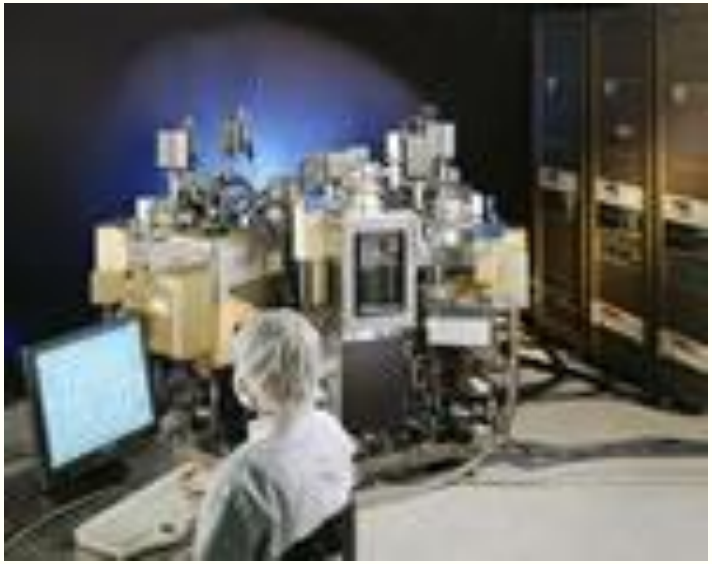
4. Plating Resist Deposition & Patterning

5. Successful Cu Electroplating

Seed Layer Sputter Process Details

- **Electrodeposited copper plating relies on a sputtered seed layer to conduct electricity during the plating process.**
- **Sputter Deposition is a Physical Vapor Deposition (PVD) technology:**
  - Under vacuum, Argon ions bombard the sputter target and target ions are deposited on the wafer.
  - Titanium is the adhesion layer to the wafer substrate.
  - Copper (deposited after Titanium) is the seed layer for Copper plating.

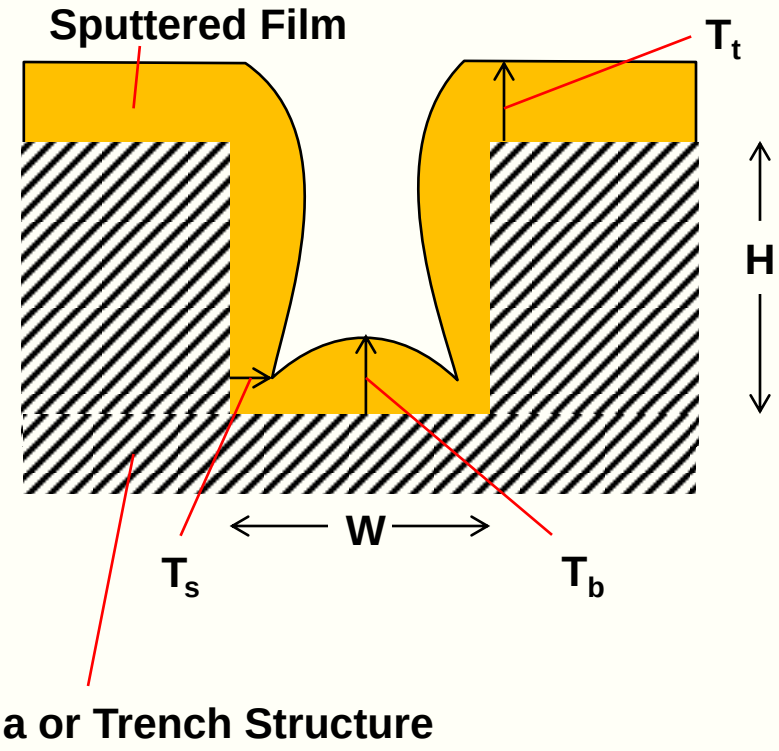




Seed Layer Sputter Process Details

- **Step coverage is a function of many factors including:**
  - Deposition temperature
  - Film thickness
  - Wafer topography
- **In general, DC Sputtered layers:**
  - Won't cover undercuts or vertical gaps.
  - May not deposit in deep trenches.

Step Coverage Diagram:



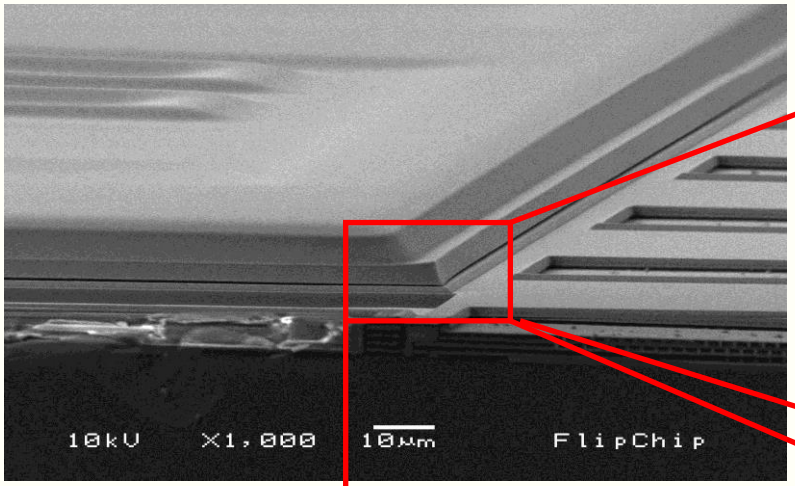
Aspect Ratio = H/W

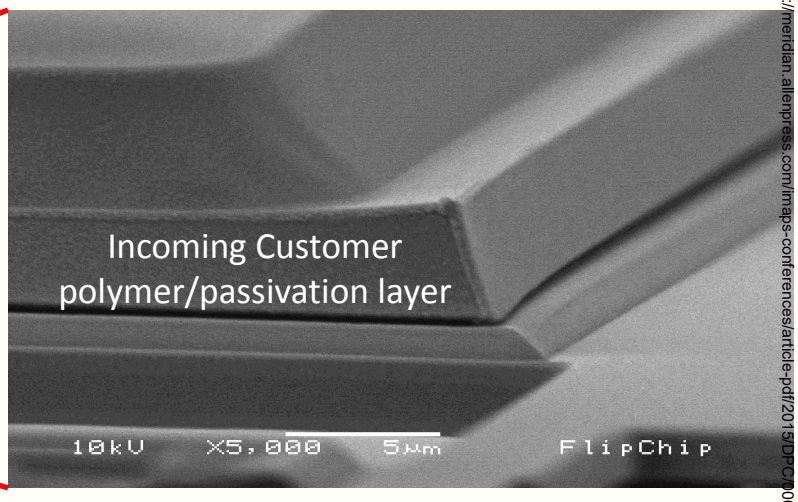
Bottom step coverage= T_b/T_t

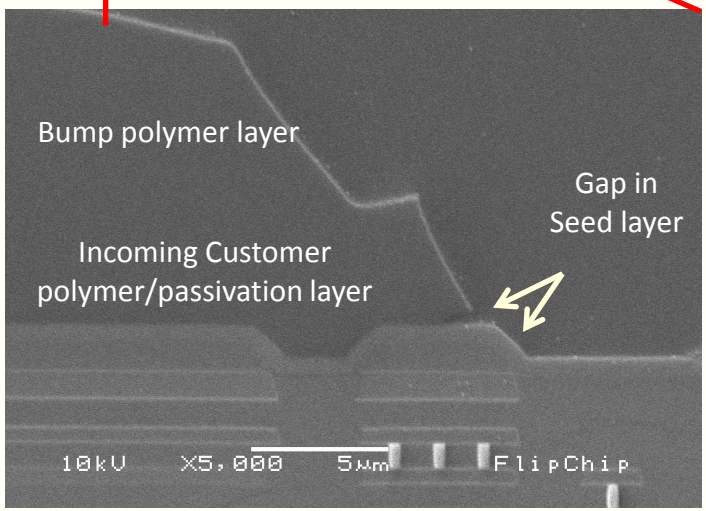
Side step coverage= T_s/T_t

Incoming wafer surface topography

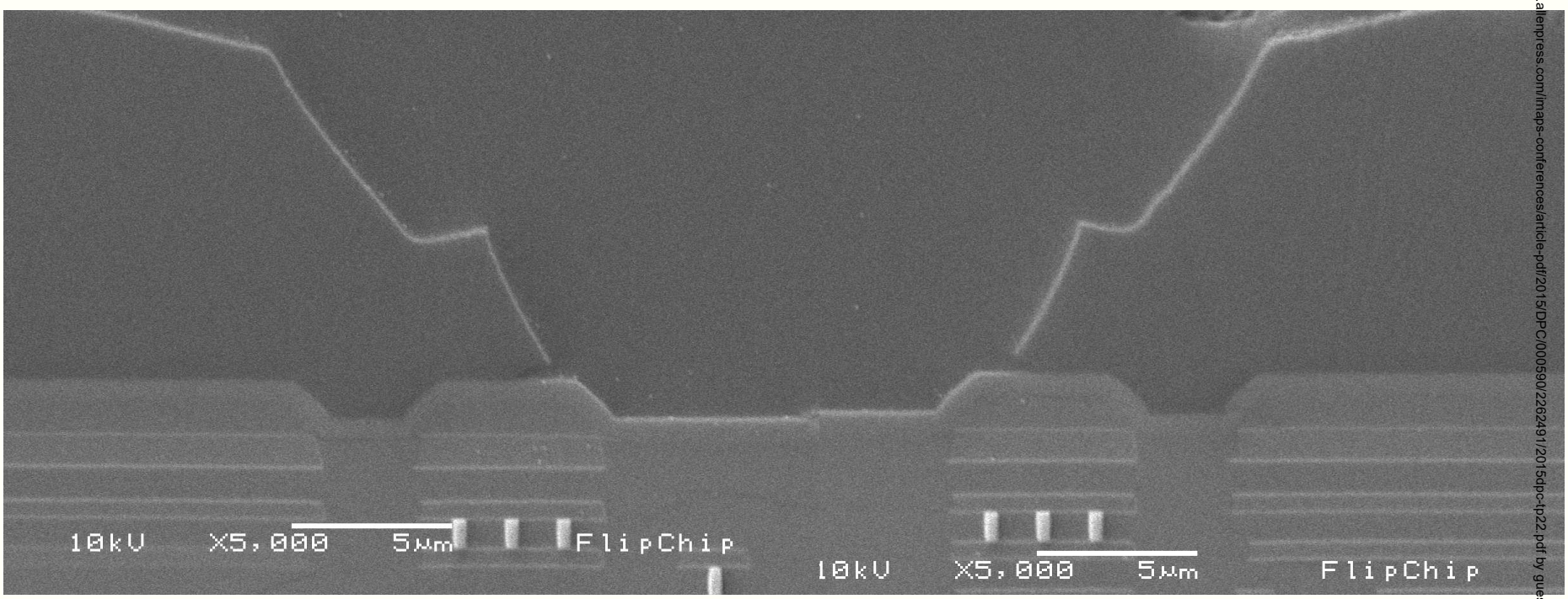
- **Front end fab die edge discontinuity**



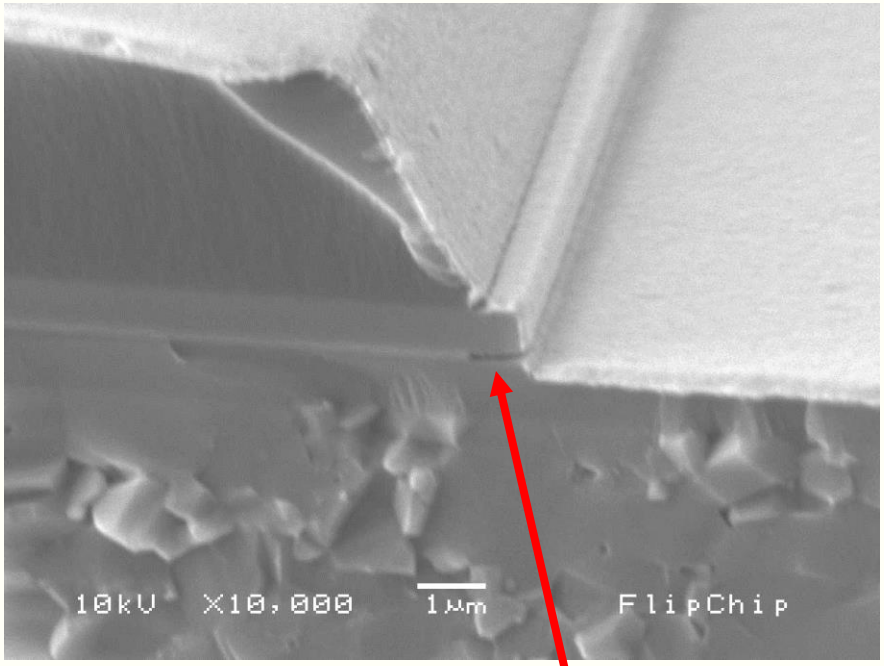


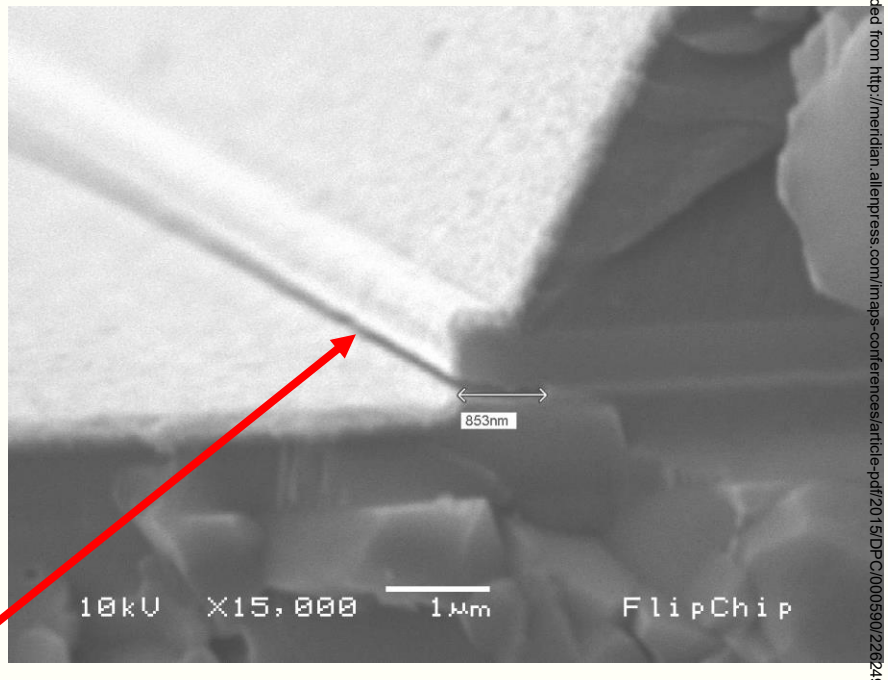


Incoming wafer surface topography



Unexpected Incoming Wafer Surface Topography

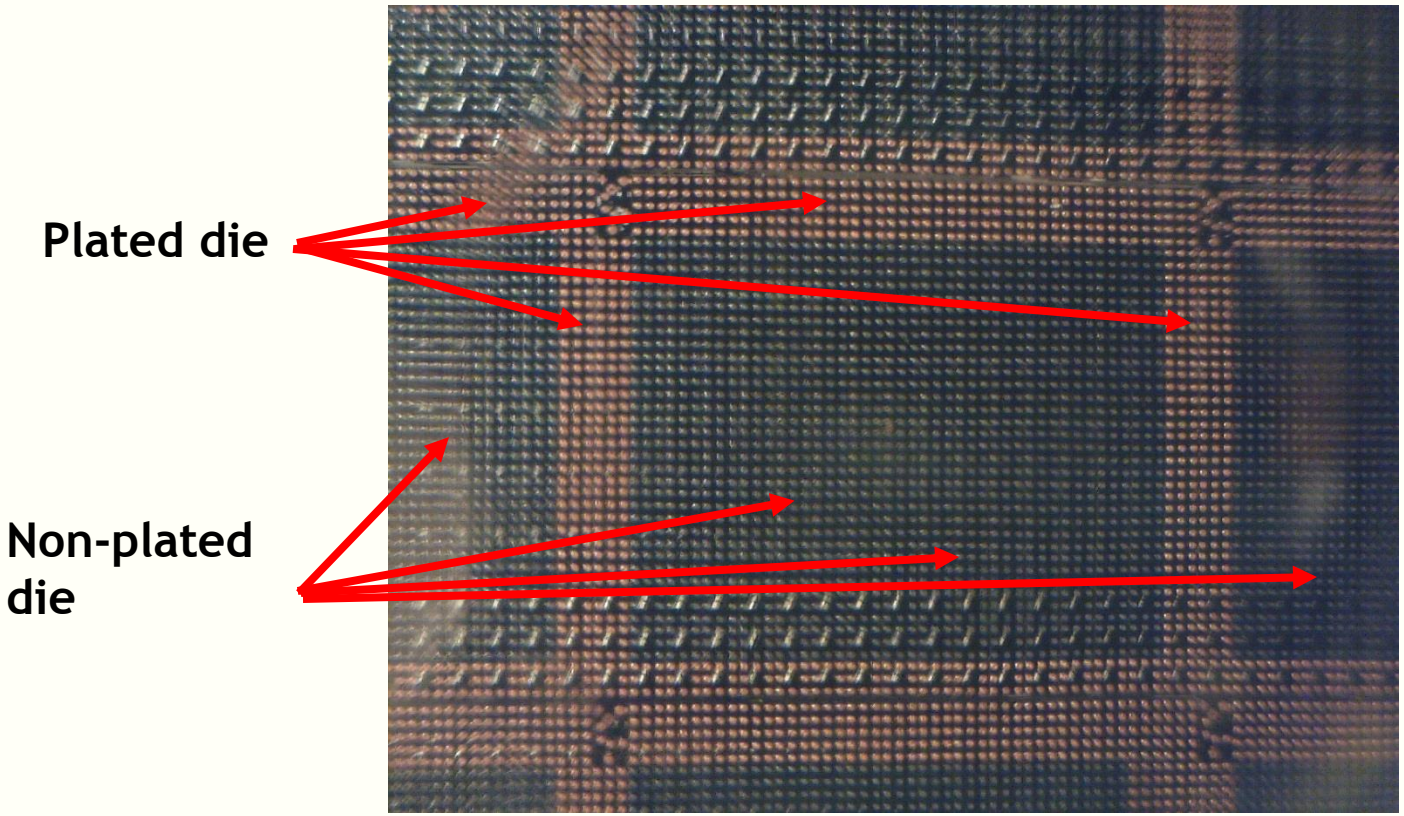




Undercuts present around the perimeter of a die

Uneven Plating Results

Portion of a wafer with non-uniform copper plating:

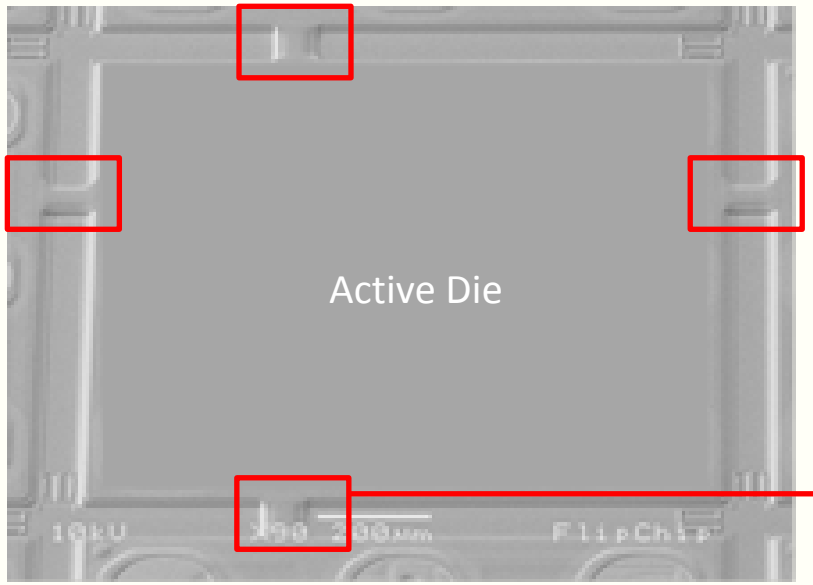


- **Saw Street Topography impacted discontinuous seed layer resulting in substantial plating variation across the wafer.**

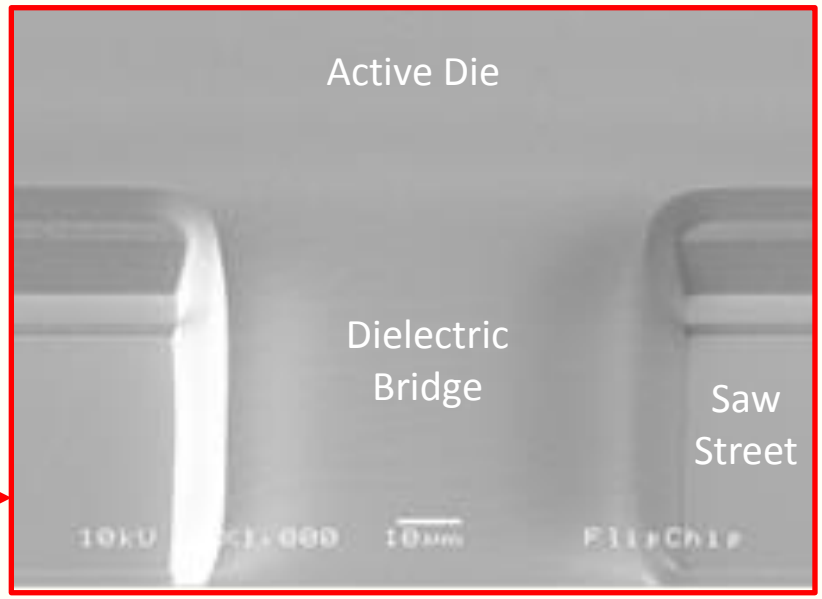
Dielectric Bridge Application

- **Dielectric Bridges interconnect the copper seed layer between die to maintain electrical continuity during electroplating.**

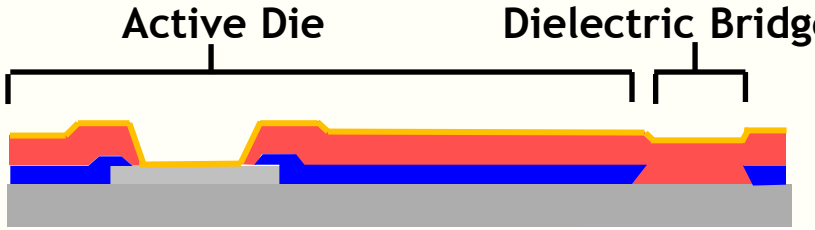
Four Dielectric Bridges (one per die side)



Close-up of a Dielectric Bridge

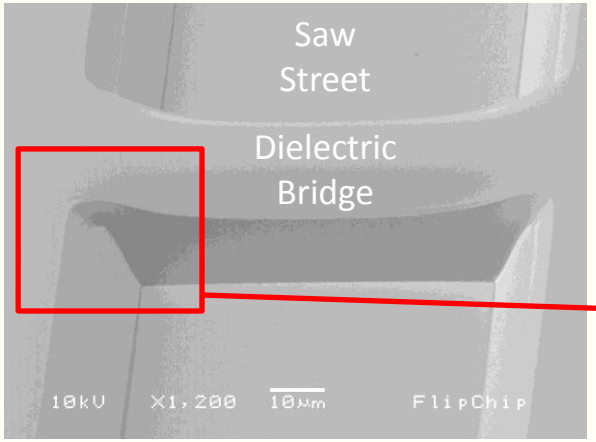


- **Cross-sectional Diagram:**

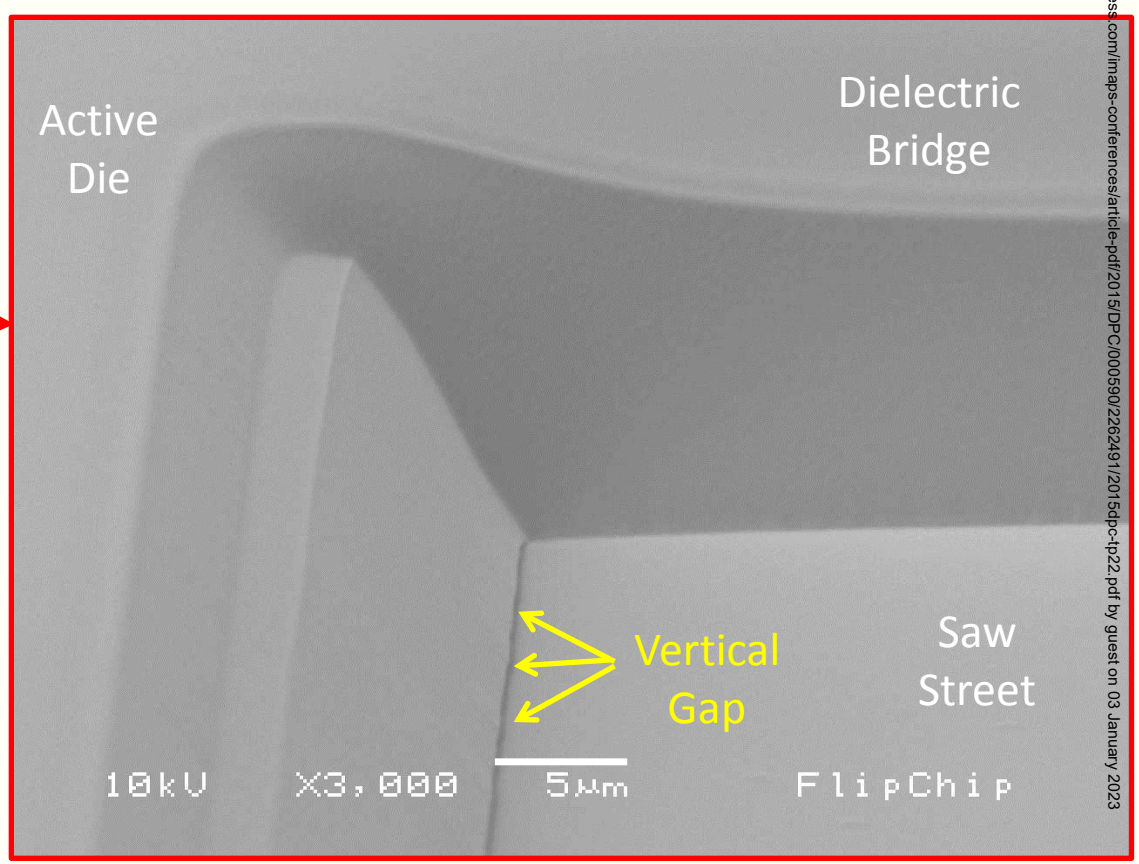


Dielectric Bridges Healing a Vertical Gap

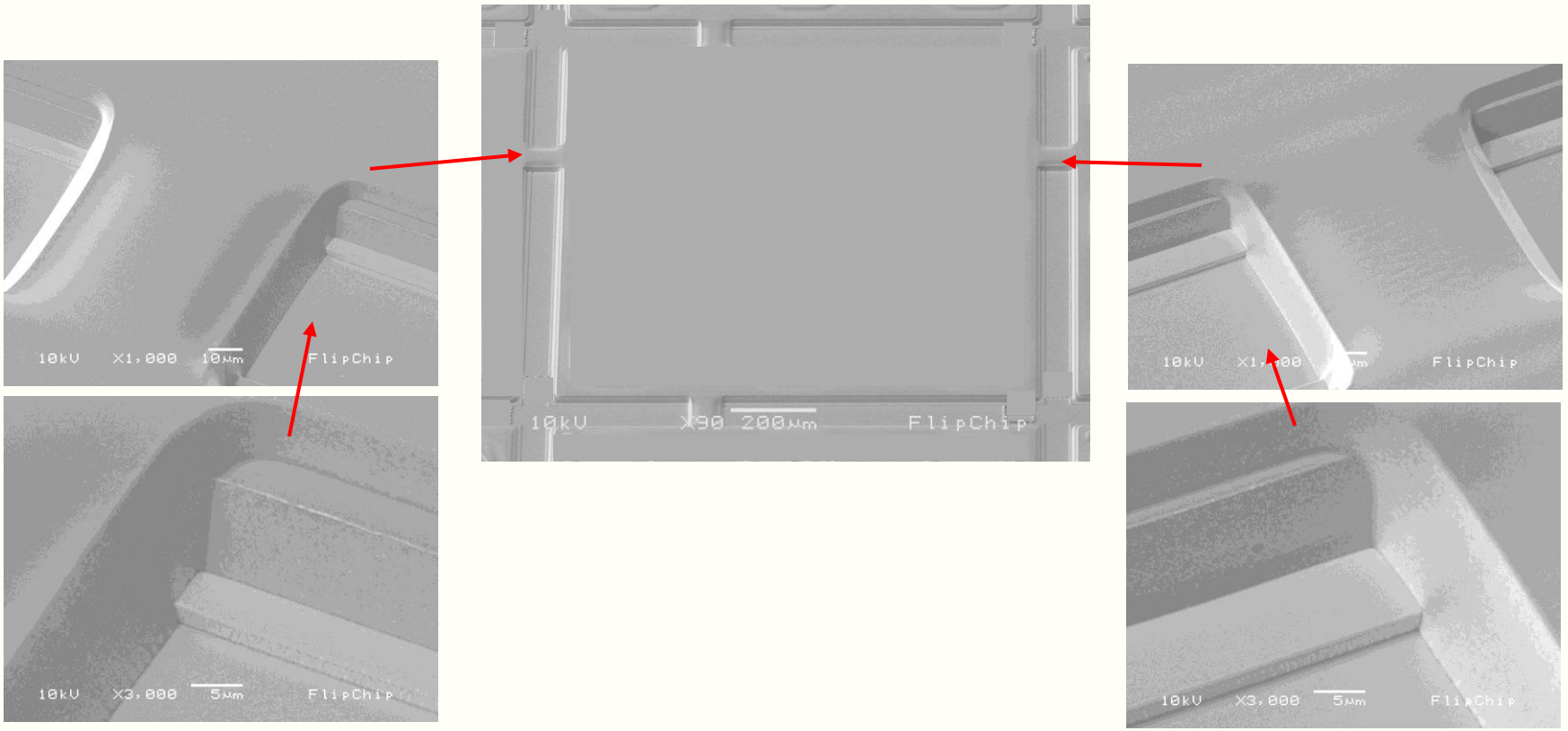
Dielectric Bridge across a saw street



Close-up of die edge area showing coverage of a vertical gap

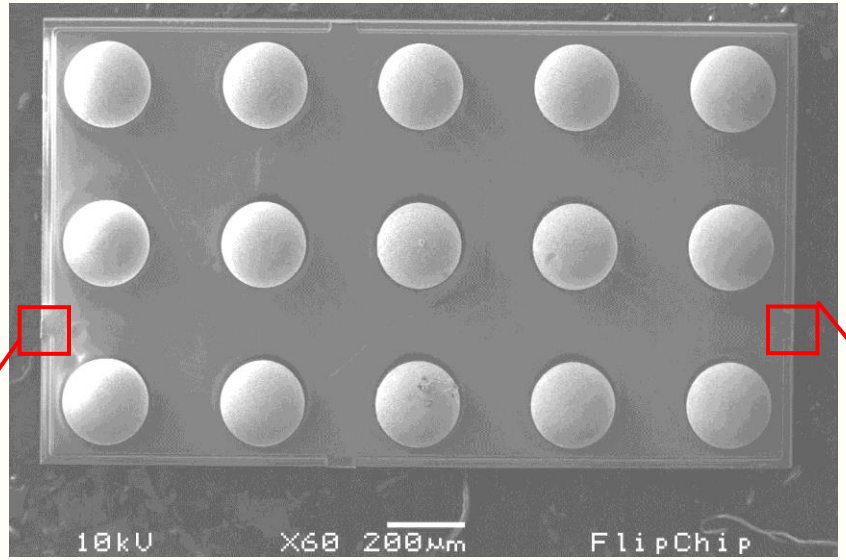


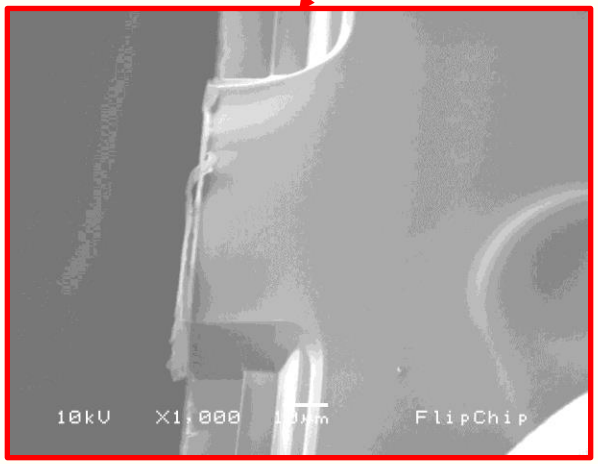
Dielectric Bridges Over Street Features



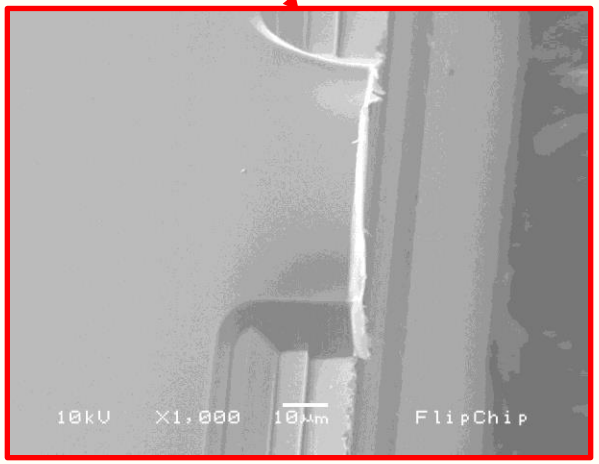
- **Dielectric Bridge surface maintains a continuous surface for a seed layer despite discontinuous street topography.**

Wafer Dicing Results

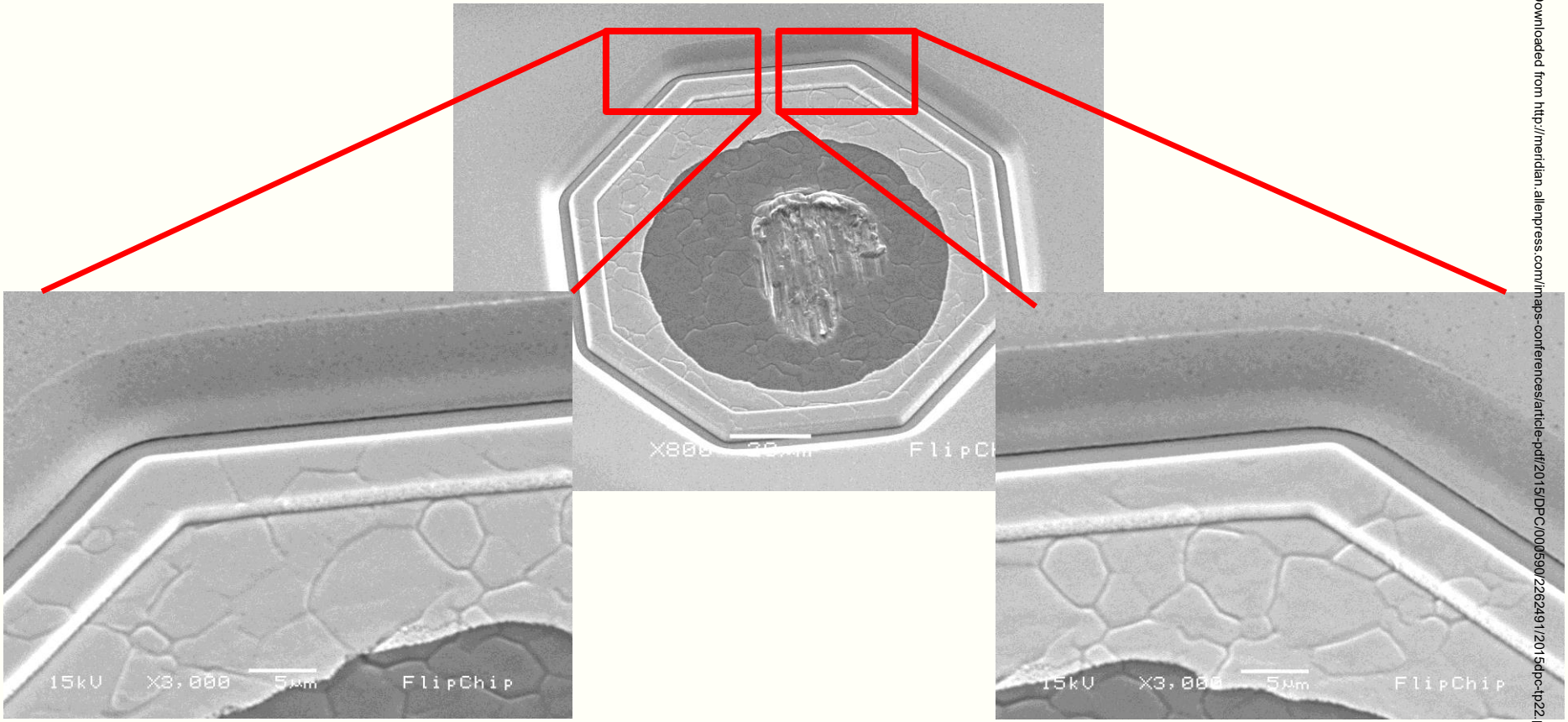




Dielectric Bridges dice cleanly.



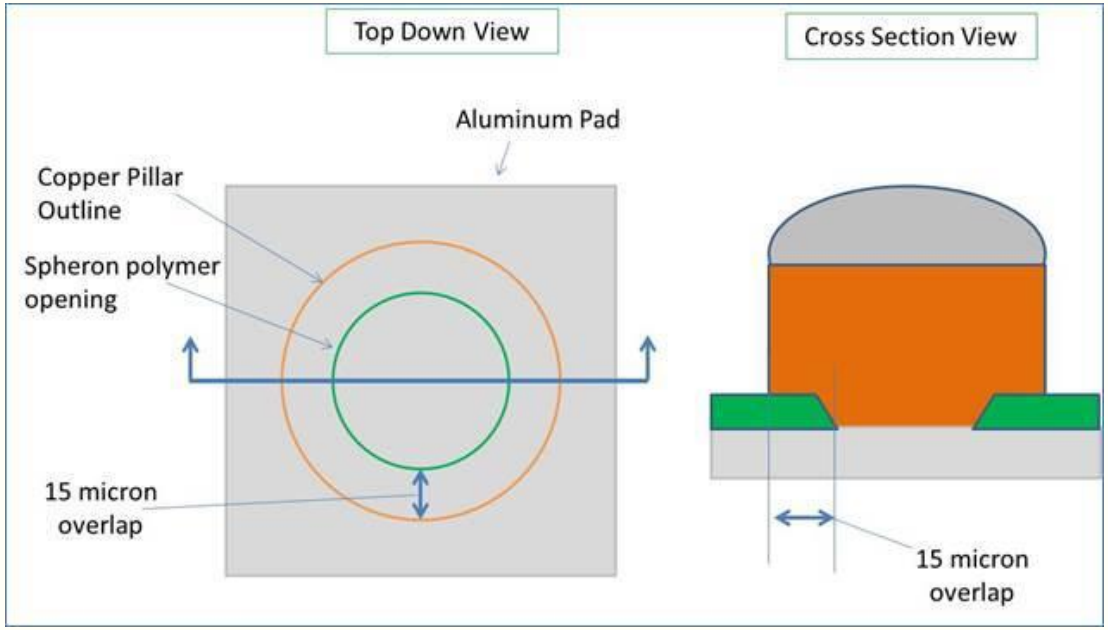
Impact of Localized Topography on Cu Pillar Bump Height Uniformity

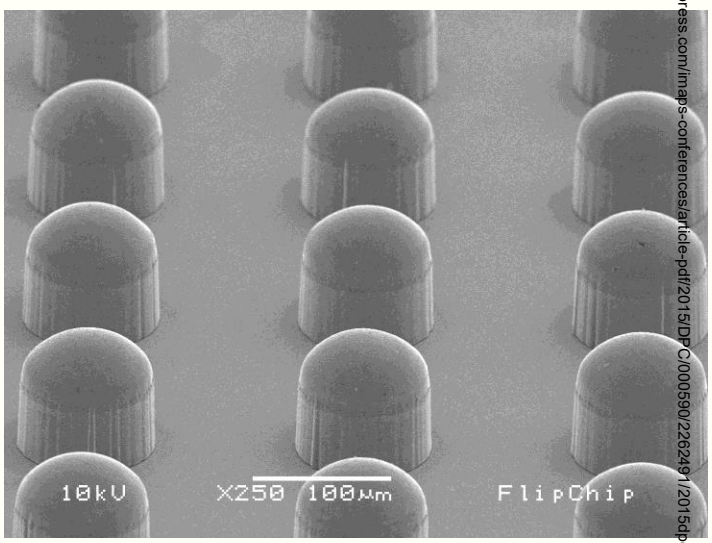


- Incoming polyimide lifted to break seed layer.
- Copper Pillar Plating did not occur for this I/O

Impact of Localized Topography on Cu Pillar Bump Height Uniformity

- **The following revision of this product added repassivation cover the polyimide to enable successful plating.**

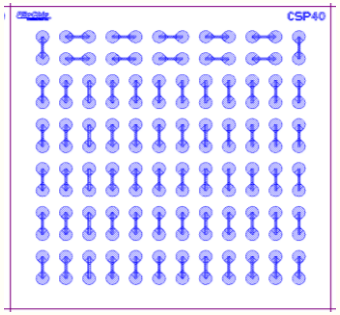




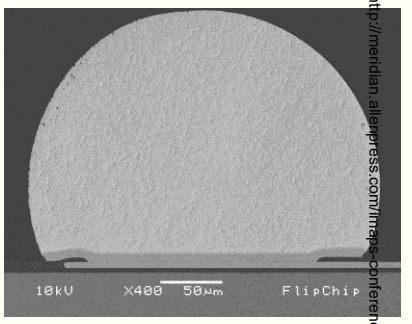
FCI CSP40 Cu Plated RDL Dielectric Bridges – Product Details

- Constructional Details

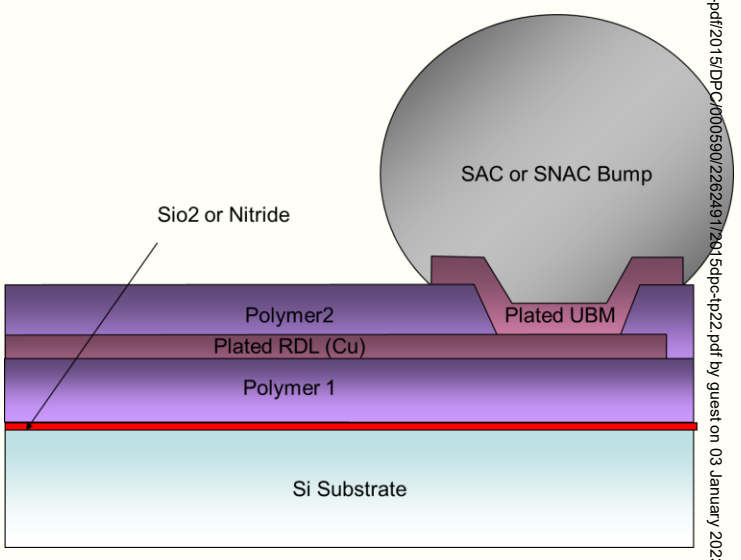
Test Die	CSP 40
Pitch	0.4 mm, 0.25mm Ball diameter
Array Size	Full Array 12 x 12 144 I/O
Die Size	5.3 mm x5.3 mm 345um thick
Solder Alloy	SAC305
Polymer Layer	Layer 1 – 4.5 $^{+/-}$1um thick Spheron Layer 2 – 4.5 $^{+/-}$1um thick Spheron
RDL	Plated – 5um thick
UBM	Plated Cu – 8um thick



CSP Test Die Layout



Cross-section at Time Zero



Cu Plated RDL Layout

Reliability Test Results of CSP40 daisychain. Dielectric Bridges testing in progress.

Qualification test results on control sample FCI's Cu Plated RDL WLCSP with SAC305 solder Alloys. Repeat Testing with Dielectric Bridges in progress.

Wafer Level Tests:

Test	Testing Conditions	Number of Hours/Cycles	Result
High Temperature Storage	150° C	1000 hours	Pass
Multiple Reflow	Standard Reflow Conditions	10x reflows	Pass
Autoclave	121°C /100% RH	168 Hours	Pass

Board Level Tests:

Test	Testing Conditions	Number of cycles/Drops to first failure	Result
Board Level Drop Tests	Jedec Specifications	434 drops	Pass
Board Level Drop Tests (underfilled units)		1004 drops	Pass
Board Level Thermal Cycling		700 cycles	Pass
Board Level Thermal Cycling (underfilled units)		1500 cycles without failures	Pass

Note: Customer Reliability Testing has validated CSP designs with Dielectric Bridges.

High Volume Experience with Dielectric Bridges

- **Electroplated copper designs with Dielectric Bridges have processed in high volume:**
  - Over 5000 wafers processed.
  - No modification in saw set-up or throughput.
  - No complaints or field returns for Dielectric Bridges.
- **Dielectric Bridges are now a standard design feature for repassivated electroplated copper designs at FCI:**
  - Avoid potential program delays in modifying incoming wafer geometry or materials for compatibility with a copper plated bumping process.
  - Eliminates wafer scrap for incoming-related geometry issues.

Conclusions

- **Dielectric Bridges facilitate the application of electroplated copper bumping technologies with different incoming wafer surface topographies.**
- **The use of Dielectric Bridges has proven successful in high volume wafer level packaging applications.**
- **Dielectric Bridges are a standard design feature for FCI repassivated electroplated copper bump designs.**