Enabling Bulk Silicon CMOS Technology for Integration, Reliability, and Extended Lifetime at High Temperature

Rex Lowther, David Gifford, Wesley Morris, Jim Jensen, Scott Peterson, Kevin Atkinson
Silicon Space Technology Corporation

Abstract

Silicon Space Technology has developed a commercial bulk CMOS process technology, HardSIL™, which allows optimization of performance, power, and lifetime at high temperatures. A method for preventing latchup, originally developed for use in the space radiation environment, is presently applied to terrestrial high-temperature environments. With the possibility of latchup eliminated in scaled CMOS technology nodes, further designs specific for high-temperature environments have proceeded well. This novel technology has been applied to our 18Mb synchronous burst SBRAM and our ARM® Cortex® M0 microcontroller, and in two CMOS processes at the 130nm technology node (Texas Instruments and GLOBALFOUNDRIES). Extensive temperature testing on these parts demonstrates that bulk silicon CMOS technology has a practical temperature limit of 250°C or higher.

Both the microcontroller and the SBRAM have been tested with clock rates up to 70MHz and at temperatures up to 260°C. Both parts have performed without error and without latchup under these conditions, and with low operating current and low leakage current. For example, the 130 million-transistor 18Mb SBRAM has average core leakage current of 580mA at 250°C and core voltage of 1.5V with test lots and simulations showing further reduction in leakage in the next, terrestrial version of this part. In addition, the 18Mb SBRAM is undergoing an endurance test at 250°C, presently at the 2500 hour milestone. Operation at temperatures beyond the present limit of the testing equipment (260°C) appears possible from extrapolation of current data.

Integration levels of greater than 8 million gates on a bulk CMOS device would allow multi-core processors with large on-chip secondary caches. Additional DSP engines or other compute engines can be accommodated for processing high resolution three dimensional images in real time. This would provide substantial distributed processing in drilling or jet engine control. These system-on-chip (SOC) integration levels can substantially reduce mechanical failures in a subsystem by reducing the number of wire bonds from greater than 1000 connections to less than 100 connections. Integration of mixed-signal A/Ds and D/As as well as on-chip power management provides a path to further reduction in mechanical connections in a sub-system.

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Introduction: latchup immunity paves way for high temperature bulk CMOS applications

It is a known problem that latchup becomes increasingly likely with increasing temperature, due to decreasing trigger voltage and trigger current margins and to decreasing holding voltages [1, 2]. This is demonstrated on test structures designed with varying width and typical core and I/O spacings in the 130nm process (figure 1) [3]. In these sample measurements, the P^+ current was forced in 1mA increments to the compliance limit of the test equipment. Without any mitigation technique (Control case), the trigger currents typically decreased by more than a factor of four over the range from 25^{O}C to 200^{O}C. This is low enough at high temperature for small voltage glitches to initiate trigger. It is also expected that these lower trigger currents lower the threshold for single-event-latchup -- even to the point where thermal neutrons at sea level, or alpha sources in the packaging can occasionally create enough charge to trigger latchup [4, 5]. Also in figure 1 are corresponding curves showing that these same structures manufactured using the HardSIL™ technology have not snapped back, even when tested to the current compliance limit of 100mA.

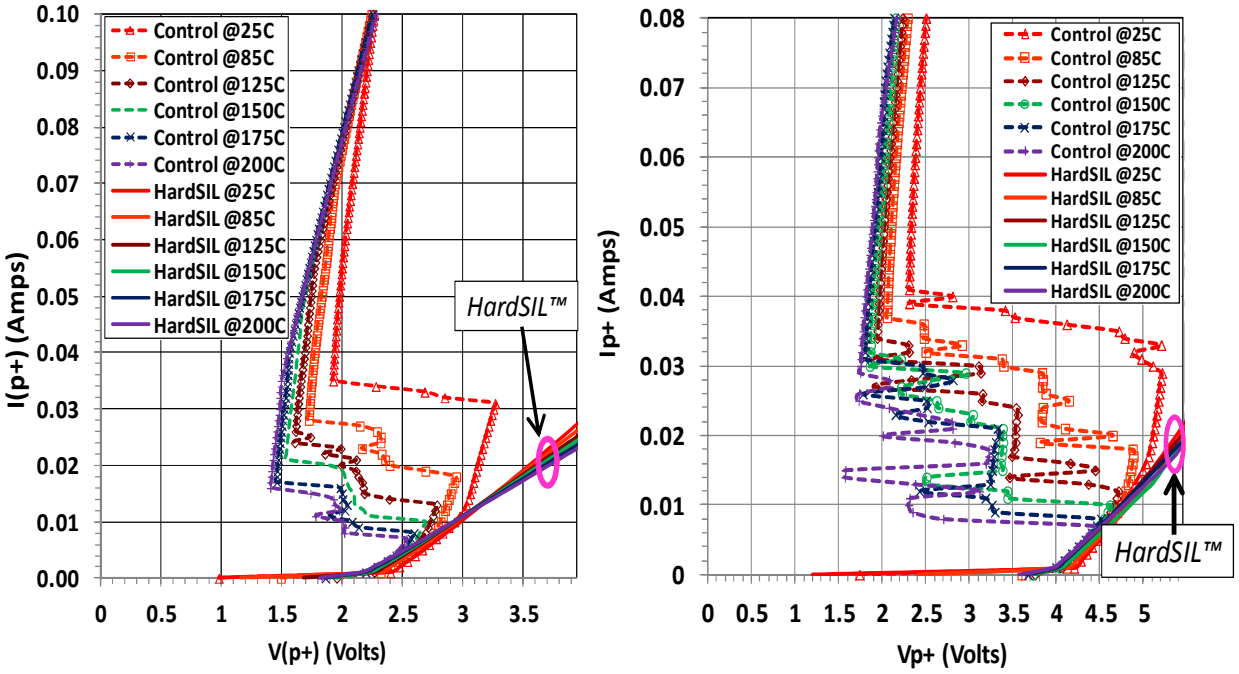

Figure 1: Measured latchup I/V curves for both standard bulk (Control) (dashed and marked lines) and HardSIL™ (solid lines) processes. The P^+ emitter current vs. P^+ emitter voltage is plotted. Both core (left plot) and I/O (right plot) test structures were used.

The approach taken here [6], HardSIL™, originally developed for the tougher space environment and now applied to high temperature environments, eliminates the possibility of triggering latchup by tying the Pwell substrate tightly to ground through a combination of buried layer and deep contacts (Buried Guard Ring, or BGR, trademarked HardSIL™). Memories manufactured on standard CMOS processes have latched at LET (linear energy transfer) as low

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as 3.5MeV-cm^2/mg. In contrast, these same memories manufactured with HardSIL™ have never latched during extensive radiation testing and effective LETs up to 117MeV-cm^2/mg, angles from 0^O to 82^O (all angles tested), temperature up to 150^{O}C, and several combinations of the above extremes. Simulations predict that the BGR will also prevent latchup with further scaling of bulk technology. Removing the threat of latchup has allowed design in bulk CMOS circuits at the 130nm process technology node for high temperature applications.

Two such parts are showcased here: The first is the ARM Cortex M0 microcontroller SOC product which provides 16kb of instruction memory and 16kb of data memory on chip (5.2 million transistors). There are 32 counter/timers with advanced triggering; 2 SPI ports, 2 UART ports, along with 32 configurable GPIO pins (figure 2). The other part is an 18Mb Synchronous Burst SRAM configurable in x9, x18, or x36 data widths with burst transfers up to 4 words. The device operates at over 50MHz at 250^{O}C with on-chip ECC and up to four byte enables for byte, half-word, and word transfers.

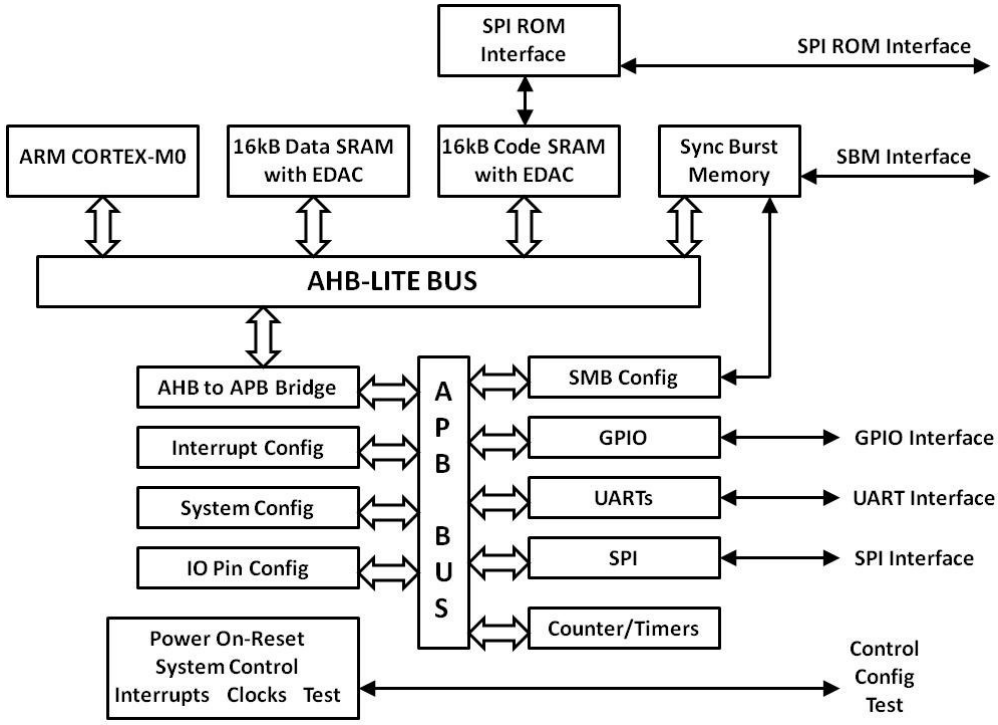

Figure 2: M0 microcontroller SOC block diagram

High Temperature Testing: M0 Microcontroller

Testing was performed on the M0 microcontroller, and functionality verified, stepping both temperature (up to 250^O) and clock rate (up to 70MHz). Core currents are shown in figure 3.

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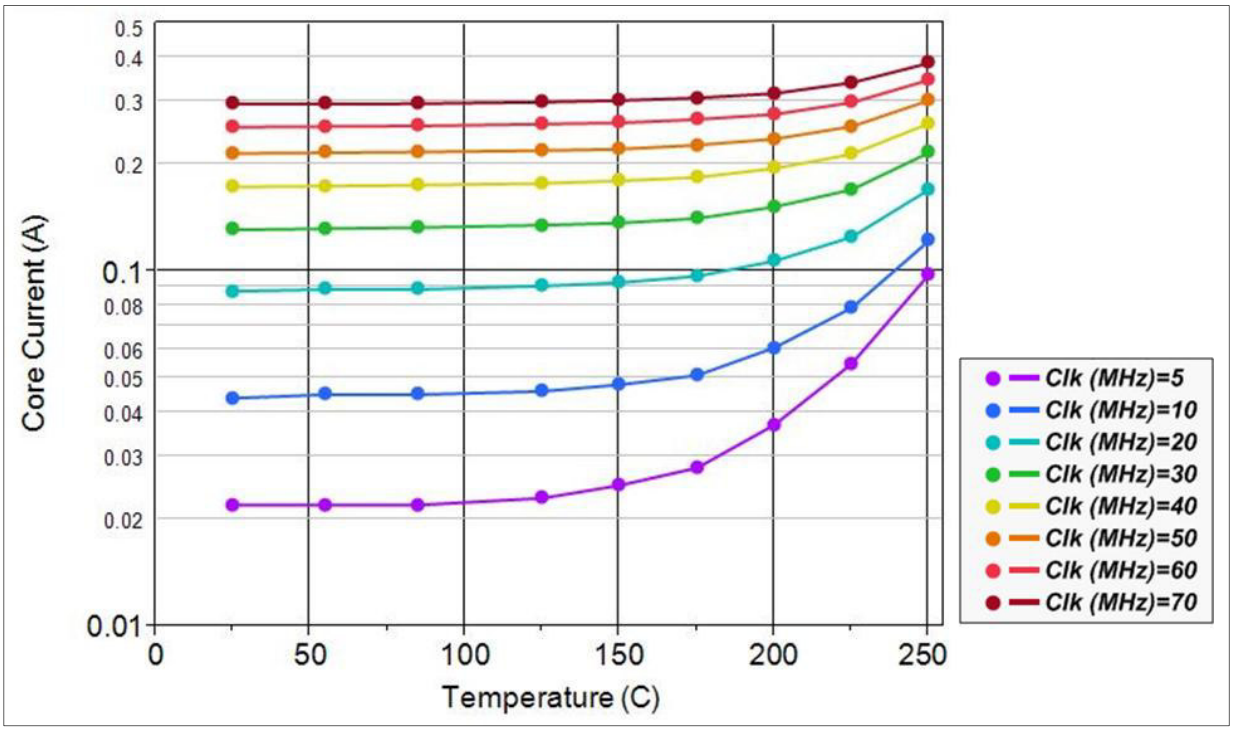

Figure 3: M0 microcontroller log (core current, Amps) vs temperature (^{O}C), stepping clock rate

Leakage current is a small fraction of the total current at the higher clock rates, even at 200^{O}C, though it does become noticeable at 250^{O}C and at the lower clock rates, accounting for most of the temperature dependence. Note that this is a demonstrational part, with ungated clock trees and triple module redundancy for radiation environments (5.2 million transistors), such that currents shown are more than a factor of four greater than expected from the terrestrial version of this same part. Measurements on test lots also predict significant additional leakage current reduction in the terrestrial version from further process optimization.

High Temperature Testing: 250^{O}C Endurance Test

High temperature testing was performed on the SST 18Mb Synchronous Burst SRAM. Testing is ongoing at the SST lab using the setup shown in figure 4. The test fixture used a polyimide heating element connected to the bottom of the packaged device and a thermocouple connected to the top of the device. The device was encased in a fully insulated silicone fixture.

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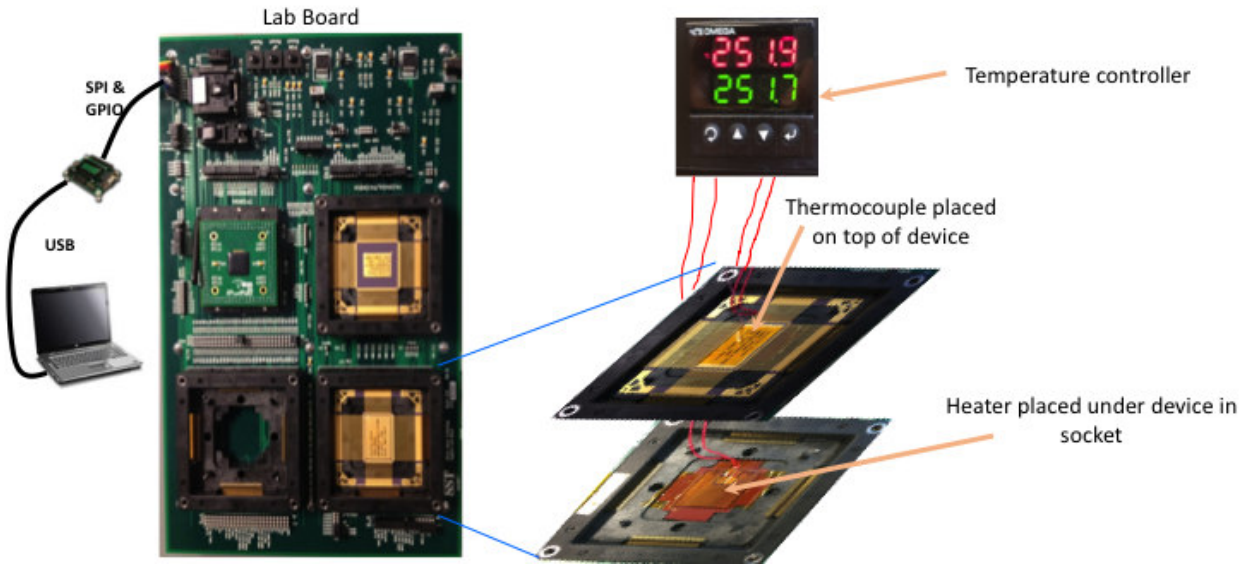

Figure 4: Lab board and test setup

The SST 18Mb SRAM device under test was initialized to 1Mhz at 25ºC with current and temperature logging enabled. Next, the clock rate was programmed to 30MHz and the memory array was written with an incrementing pattern. Continuous reading and validation of the full address space was initiated with I/O Voltage of 3.3V and core Voltage of 1.5V. The temperature was ramped to over 250ºC in approximately 15 minutes while the device array was read at 30MHz and expected data was continuously checked. The current logged is the total VDD current for the entire lab board. Data logging of current and voltage measurements were taken at 5 second intervals while maintaining temperature for approximately 8 hours. The experimental sequence was repeated on a daily basis through the 2500 hour milestone [corresponding to 123 trillion (1.23e14) bit reads without an error]. At 25ºC initialized current readings at 30MHz clock rate (ungated clock tree) remained relatively constant at 250mA. During both the read and write sequences, at 25ºC, board currents increased to approximately 300mA, remaining stable throughout the test. As the temperature was elevated to over 250ºC the current increased to 880mA. Most variation in the logged current can be attributed to variation in the temperature; all remaining variability had a sigma of less than 1%. No significant trends in the total current or its variability were observed. No errors were logged, and no degradation in current or performance occurred over the duration of the test. The time logged does not include test time at 25ºC, the temperature ramp, or the temperature cool-down period.

We are repeating this test on multiple parts for statistical verification and to determine separate chips' contributions to the total current. Until then, since this one device has worked over 2500 hours above 250ºC, we at least have a reference point for the plot in figure 5 where a standard Arrhenius dependence (activation energy = 0.575eV) is used to estimate minimum terrestrial lifetimes at different temperatures.

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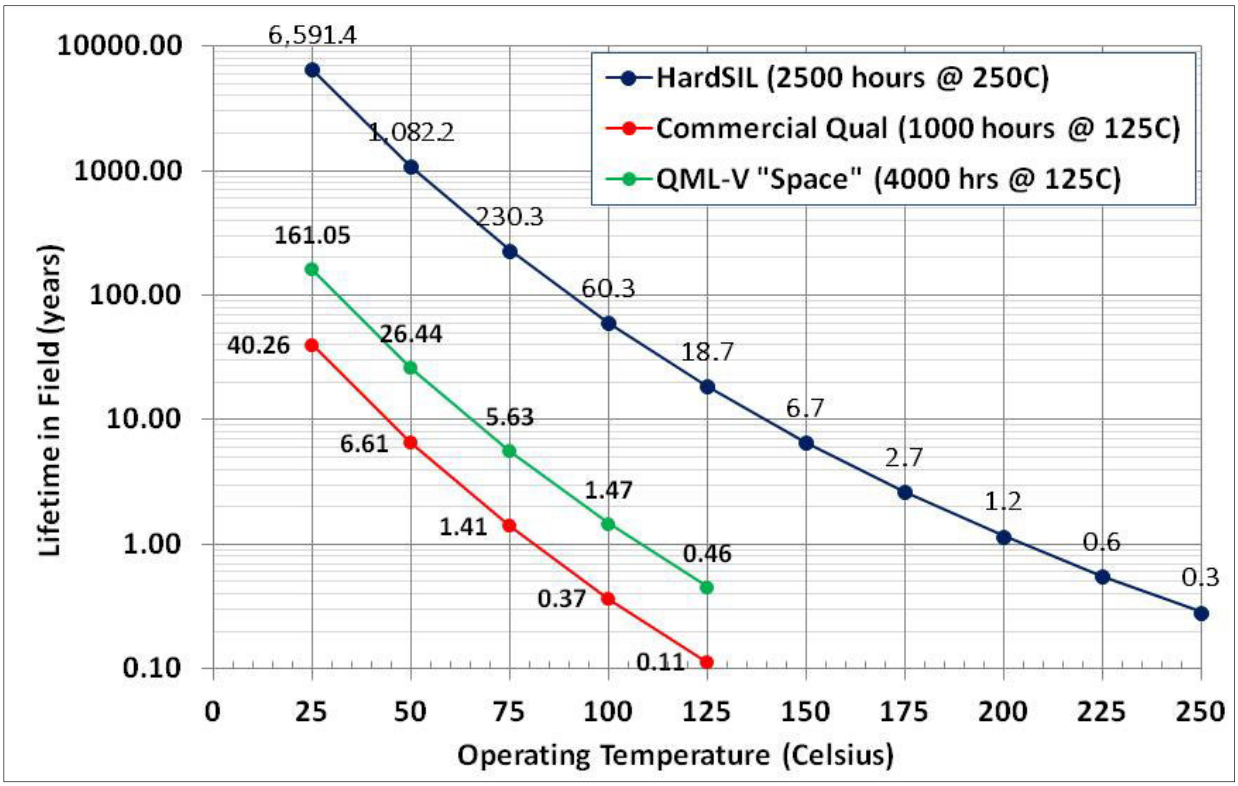

Figure 5: Predicted minimum lifetime vs operating temperature in the field based on various acceleration test criteria (Commercial, QML-V) and on the ongoing endurance test results (18Mb Synchronous Burst SRAM using HardSIL™)

Integration and Summary

The HardSIL™ process inherits the advantages of the baseline commercial 130nm process: high density, low defect count, high yield, and high lifetime with respect to the typical terrestrial wear-out modes. This includes back-end-of-line processing with up to nine levels of all-copper interconnect and its advantages in resistivity and electromigration performance [7]. The 18Mb SBRAM, with over 130 million transistors, equates to a highly integrated system-on-chip (SOC). Bulk CMOS at 130nm design rules at this integration level typically have been specified to run under 1000 hours at 200^{O}C. From the Arrhenius plot (figure 5) based on 2500 hours of testing at 250^{O}C, devices can be expected to function for greater than one year (9600 hours) at 200^{O}C. At 175^{O}C, the plot indicates longevity exceeding 20,000 hours.

Integration levels of 130k used gates/mm^2 with over 8 million usable logic gates on a bulk CMOS device would allow multi-core processors with large on-chip secondary caches. Additional DSP engines or other compute engines can be accommodated for processing high resolution three dimensional images in real time. This would provide substantial distributed processing in drilling or jet engine control. SOC integration levels can substantially reduce

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mechanical failures in a subsystem by reducing the number of wire bonds from greater than 1000 connections to less than 100 connections. Integration of mixed-signal A/Ds and D/As along with on-chip power management provides additional reduction in mechanical connections in a sub-system. The advanced 130nm bulk CMOS technology also allows high speed differential signaling such as LVDS I/O drivers that would further reduce board-to-board mechanical connections improving reliability. For example, consider the reduction from 1000 connections to 100, and a simple assumption of 0.1% error probability for each connection after a particular duration in the field, each random and independent; then the system failure probability at that time is reduced from 63% with 1000 connections to 10% with 100 connections. Of course wear-out of the connections is a more relevant concept than random failure, as failure probability is a strong function of time. But with fewer connections, each can be made more rugged; and the lifetime increases through both reduction of number of failure points, and reduction in the failure rate of each component.

Removing the threat of latchup in a commercial process has allowed us to design bulk CMOS circuits in a more advanced technology process node (130nm) than what is typically used at high temperatures. The higher integration level further allows for much higher system reliability, and systems with greater processing power.

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