SiC Lateral Diodes for ESD Protection of High Temperature Integrated Circuits

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Abstract

Lateral diode based electrostatic discharge (ESD) protection for silicon-on-insulator (SOI) circuits suffer from high leakage currents at elevated temperatures. This may degrade the performance of SOI based integrated circuits and can also limit the life of the system. Wide bandgap materials such as silicon carbide (SiC) can potentially mitigate this problem because of their low intrinsic carrier concentrations. In this study, lateral SiC diodes have been fabricated and evaluated at high temperatures for ESD protection. The leakage level of SiC lateral diodes with an active area of 700 μm^2 is shown to be as low as 1 pA at 200 °C and 25 pA at 300 °C. Furthermore, based on circuit simulations, the number of lateral SiC diodes required to protect against an ESD event (human body model) at 2kV was determined to be 20 devices. Under reverse bias conditions (at 20V), these diodes would have a total leakage current of 20 pA at room temperature and 500 pA at 300 °C. .

Keywords: Silicon carbide, ESD diode, lateral diode, high temperature, extreme environment

Introduction

Protection against ESD events is an important factor for reliability of integrated circuits (ICs). Chip level protection is typically achieved by using ESD diodes at input and output bond pads, along with a supply voltage clamping circuit for maximum reliability. This approach has been implemented in SOI based ICs for high temperature applications. Commercially available SOI ICs typically have ESD ratings of 1kV to 2kV (using the human body model [1]), but can be as low as 250V for certain parts. The buried oxide layer in the substrate with high thermal resistance introduces heat dissipation and thermal runaway concerns [2]. It also limits the ESD protection circuitry to lateral diodes [3]. Furthermore, lateral diode based ESD protection for SOI ICs suffer from high leakage currents at elevated temperatures [4]. This high leakage may degrade performance of IC and can also limit the life of the system. In this work, lateral SiC diodes have been fabricated and evaluated for ESD protection. We also report the diode leakage currents as a function of temperature for certain level of ESD protection.

Device Fabrication

Silicon carbide lateral diodes were formed on a p-type epitaxial layer with doping concentration of $1x10^{17}$ cm^{-3}, grown on Si-face, 4°-off axis, N^+ 4H-SiC substrates. The cathode area of the diode was implanted with nitrogen, and a p+ anode region was formed using an aluminum ion implant. The SiC surface was capped with a graphite layer, and the implants were activated at 1675°C for 30 minutes. Next, 550 Å Ni was deposited over the anode and cathode regions for ohmic contacts. The ohmic contacts were then annealed at 1050°C for 3 minutes to form low resistance contacts. Finally, a metal stack containing gold was deposited as bond pad contacts.

Results and Discussion

Fig. 1 shows the top view of the 700 μm^2 SiC lateral diode and I-V characteristics (forward & reverse) from room temperature up to 500 °C. It can be observed that the cut-in voltage decreases as the temperature increases as seen in SOI diodes. However, unlike SOI, the leakage current at 20V reverse bias, remains less than 25 pA up to 300 °C, and less than 250pA up to 500 °C. This low reverse bias leakage current which is due to low intrinsic carrier concentration in SiC, makes it an ideal candidate for ESD protection when the SOI circuit is intended to operate at high temperatures.

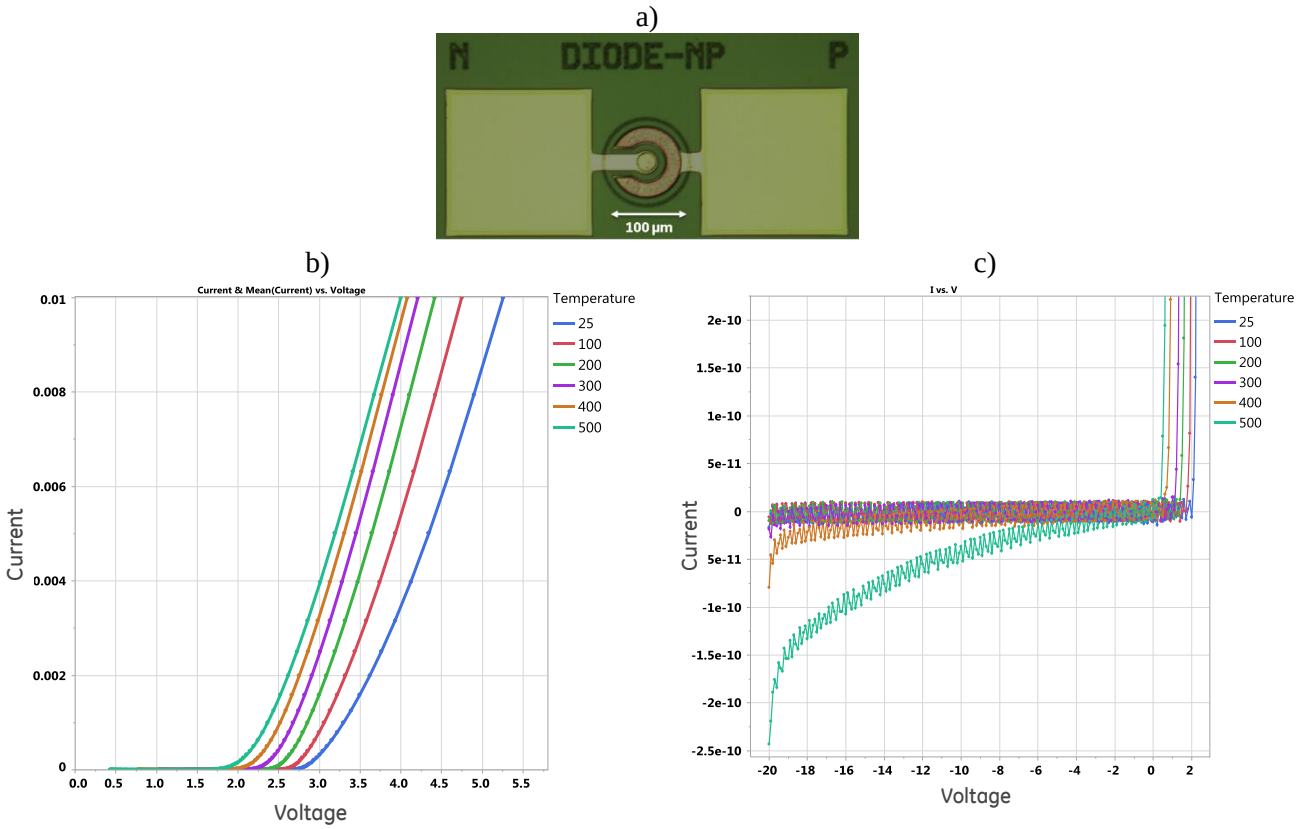

Fig. 1 a) Top view of fabricated SiC lateral diode, (b)I-V sweep of the diode under forward bias at various temperatures , and c) I-V sweep under reverse bias.

The performance of the SiC lateral diode as an ESD protection component has been evaluated with the human body model. In this model, a 150 pF capacitor is charged to a specific voltage, for example, 1kV. A switch is then closed, and the energy is discharged through a 330 Ω resistance to the bond pad of the IC. In Fig. 2, the bond pad is protected via a simple two diode approach (D0 and D1). R1 and C4 represent a MOSFET gate as the load. In a typical IC, the top diode (D0) shunts a positive ESD voltage pulse to the upper supply voltage rail, and a voltage clamping circuit shunts the excess charge back to ground, and limits the voltage build up on the supply voltage rail. For simplicity, we evaluated the effectiveness of the diodes by shunting the ESD charge directly to ground.

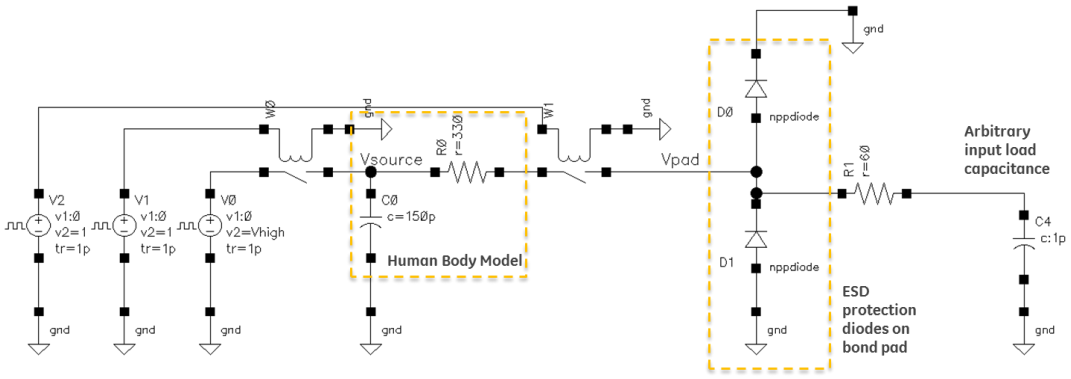

Fig. 2 Schematic of the simulation circuit for an ESD event.

In the simulation presented in this work, C0 is charged to a specific voltage by closing switch W0. W0 is then opened and switch W1 is closed to discharge the energy to the bond pad circuit at 2 ns into the simulation. Fig. 3 shows an example transient response of the voltage on C0 (Vsource) and the voltage on Vpad for a 250V ESD event. Because the ESD diodes shunt current away, the voltage on the bond pad reaches a maximum of only 6.6V.

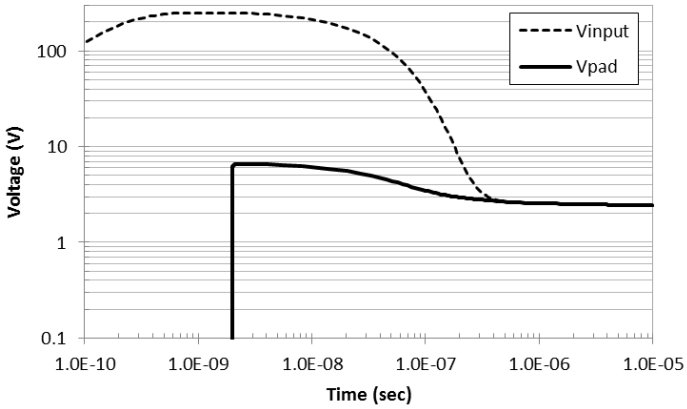

Fig. 3 Transient simulation of a 250V ESD event on a bond pad.

Fig. 4 plots the maximum voltage reached on the bond pad as a function of ESD events. Two cases are simulated: a ”small” ESD protection that corresponds to having 2 of the 700 μm^2 diodes in parallel, and a “big” ESD protection that corresponds to having 20 of the above mentioned diodes in parallel. In this model, the maximum allowable bond pad voltage was selected to be 35V, and the results indicate that the two diode protection circuit (small ESD) affords an ESD protection level of roughly 250V. The 20 diode circuit provides a protection level of about 2kV.

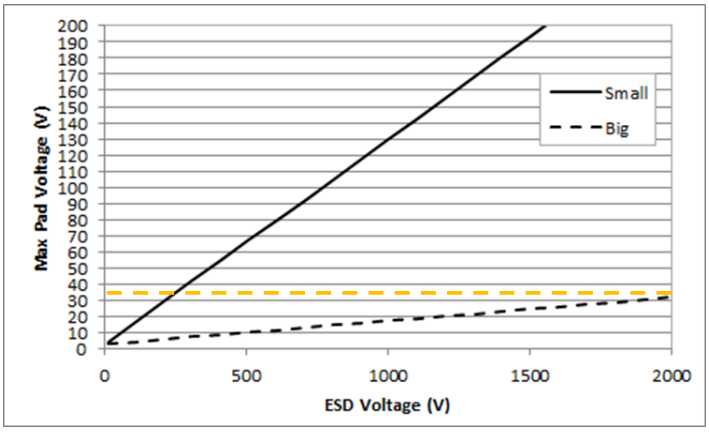

Fig. 4. Maximum bond pad voltage reached vs. ESD event voltage.

Based on the leakage measurement (Fig.1) at 300°C, the leakage current of the 2 diode protection circuit is estimated to be 50 pA with a 20V reverse bias, whilethe leakage current of the 20 diode protection circuit under the same condition would be 500 pA. The results are summarized in Table.1

Table.1 Summary of SiC ESD protection level and corresponding leakage current at 300 °C and 500 °C

	Maximum ESD protection (V)	Leakage (@ 20V reverse) 300 °C	Leakage (@ 20V reverse) 500 °C
Small ESD (2 diodes)	250	50 pA	500 pA
Big ESD (20 diodes)	2000	500 pA	5nA

For validation of the simulation results, we used a handheld ESD simulator and applied various levels of ESD events (at room temperature) to the bond pad of a test circuit consisting of two shunting diodes and a MOSFET gate. The MOSFET was observed to be functional after a 250V ESD event, but failed after a 300Vevent, which agrees with the simulation results.

Conclusion:

In this work, lateral SiC diodes have been fabricated and evaluated at high temperatures for ESD protection. The leakage levels of SiC lateral diodes with active areas of 700 μm^2 have been observed to be as low as 1 pA at 200 °C and 25 pA at 300 °C. Furthermore, based on circuit simulations, it was determined that 20 lateral SiC diodes are required to protect against an ESD event (human body model) at a 2 kV level. These diodes would have total leakage current of 20 pA at room temperature and 500 pA at 300 °C with a 20V reverse bias.

Acknowledgment

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