

Ceramic-Based Planar Heat Pipe (Plate) for Passive Electronics Cooling

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Abstract

Heat dissipation has become a major hurdle for the electronics industry, especially as higher performance integrated circuits are being developed for the power industry. Two of the primary hurdles in dissipating this heat are:

- 1) The thermal contact resistance between the IC and the cooling device.
- 2) The ability to effectively spread the heat, such that traditional cooling technologies can be effective.

By selecting ceramic materials that are thermo-mechanically matched (CTE) to IC materials, the proposed heat plate can be directly bonded by typical solder or braze techniques to the back-side of the IC. This eliminates thermal resistances due to contact and thermal interface materials. Within these heat plates, a three dimensional network of gas channels and fluid wicks spread the high-flux heat loads from localized hot spots to the surrounding regions via phase change fluids and mass transport. Like traditional heat pipes, these heat plates operate at nearly uniform temperature due to the phase change. The internal networks provide for multi-dimensional heat and mass flow, increasing their dissipating capability.

By using matched ceramic materials, and the inclusion of a heat plate, these primary hurdles for heat dissipation can be mitigated. The performance of prototypical planar heat plates will be presented.

Keywords: Ceramic, Heat Plate, Passive Cooling, Thermal Management

Introduction

Demands for heat management have increased with increasing power densities in micro-electronic components. In order for these devices to operate reliably the heat produced must be dissipated. Advanced chips have localized power densities approaching 500 W/cm²; advanced electronics compound these issues because of the increased number of chips requiring cooling. Heat dissipation in notebook computers is restricted by the available space. Current, state-of-the-art thermal management devices use active liquid cooling, phase change materials, and evaporative cooling. Microchannel devices can enable these cooling methods, or be used to fabricate micro heat pipes. Ceramic microchannel devices have attractive dielectric and thermophysical properties, and can be fabricated relatively inexpensively.

There are two primary thermal resistances in dissipating these heat loads.

The first resistance is found at the chip to cooling system interface – getting the heat out of the chip and into the cooling system. Most often, the chips are made from silicon, gallium, or silicon carbide based materials. These have moderately low coefficients of thermal expansion (CTE), in the range of 4-6x10⁻⁶ mm/mm°C. Heat sinks and other cooling systems are most often fabricated from metals with high thermal conductivities to augment heat dissipation; their CTEs are about 15-18x10⁻⁶ mm/mm°C. This thermo-mechanical mismatch requires a compliant thermal contact medium that prevents mechanical stresses from building while high temperature ICs shed heat to cooler heat dissipation devices. The compliance of these thermal contact mediums fills the irregular surfaces and prevents mechanical shear. Under high power conditions, these interface materials restrict the heat rejected to the cooling system and drive up the chip temperature or driving potential for heat dissipation.

Even a few degrees are substantial in electronic packages that are at their limits with the existing technologies. Without improved cooling technologies, increased chip performance can not be realized.

The second resistance for dissipation of these high heat loads is that of distributing or spreading the heat so that it can be rejected to the surrounding environment. The introduction of heat pipes has facilitated the distribution of heat to remote and large surface areas with minimal temperature gradient, because of the isothermal phase change of the working fluid. For most terrestrial applications, ultimately this heat is rejected to the ambient air through convection. Large surface areas are necessary because of the low density of air, its poor convection characteristics, and the relatively small temperature differential between air and the IC. This has been illustrated by the development of larger, more complex heat sinks. Minimizing the temperature drop within the heat spreader permits more effective dissipation, may increase its thermal capacity, or reduce the size and flows required for the heat sink.

Although it is an over-simplified analogy, when budgeting for cooling of high performance electronics, the taxes of temperature drops due to thermal interfaces and heat spreading must be understood and minimized so that one can predictably and reliably use the remaining buying power to attain the goal – low temperature ICs.

Minimization of Interface Losses

In optimizing the interface between the high power electronics chip and the cooling system, the objective is to minimize the temperature drop while ensuring that the thermo-mechanical stresses for the coupled IC and cooling system do not compromise the reliability and life of the chip. Obvious other constraints would include size, weight, and cost.

A common metric for evaluating the temperature losses at the interface is the thermal contact conductance of interface materials. Several of these reported values are given below. For descriptive purposes, these conductance values are evaluated to yield a comparative temperature drop per 100 W/cm² heat flux.

Table 1: Contact Conductance for Interface Systems

Interface	Thermal Conductance (10 ⁴ W/m ² K)	ΔT (°C)	Comments
Arctic Silver 3 ⁱ	6.15 + 0.65	1.63	Rough faces, low pressure
Arctic Silver 5 ⁱ	9.79 + 1.01	1.02	Rough faces, low pressure
Ceramique ⁱ	7.21 + 0.10	1.39	Rough faces, low pressure
Carbon/Silver bilayer ⁱ	21.18 + 1.64	0.47	Rough faces, low pressure
63%Sn-37%Pb Solder ⁱⁱ	600 + 80	0.17	15 micron molten application

These temperature drops across the interface scale linearly with power and become much more significant with high power applications. Hence, if the chip to cooling system interface could be made from a molten solder the thermal conductance is greatly improved, minimizing the temperature losses; this is presumably due to the filling of voids and gaps while minimizing the overall thickness.

More optimal solders may include silver yielding higher thermal conductivities. Based solely on thermal conductivity of the materials, a 96.5Sn/3.5Ag solder could have a temperature loss as low as 0.1°C per 100W/cm² flux.

The thermo-mechanical stress that results in the bonding of dissimilar materials as they go through thermal transients is a complex analysis. A simple, yet conservative approach is to estimate the residual stress after bonding assuming that the bond layer (solder) is thin and bonds perfectly to the substrates without yielding between these substrates. These calculated stresses reflect the severity of the material mismatches and must be compensated for in the chip, cooling device or bond material (See Figure 1). Typically, high stresses catastrophically fail the chip, or the bond fails with cycling fatigue.

With the understanding that these calculations are comparative, it can be seen that the residual stresses between a silicon chip and a ceramic-based cooling system is feasible due to low stresses. The CTE matching of silicon and the preferred non-oxide ceramic systems make them relatively insensitive to the bonding temperature. However, metal-based cooling systems are not feasible, even with low temperature solders. Hence, compliant thermal conductive pastes are used.

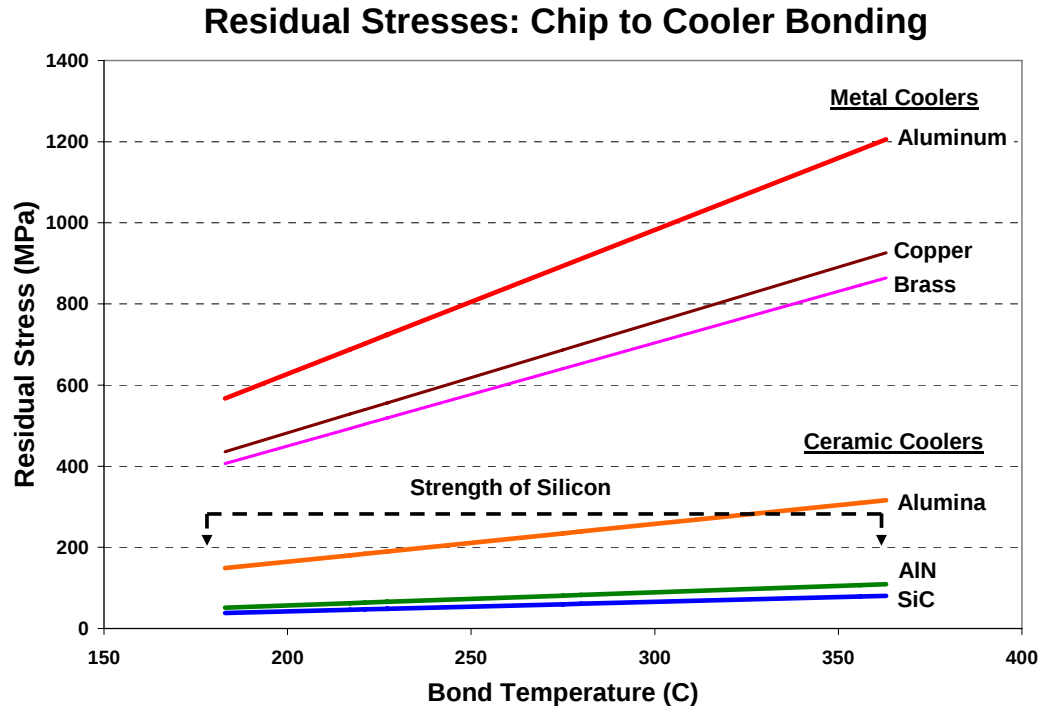


Figure 1. Residual Stresses Resultant from the Bonding of Silicon to Thermal Cooling Materials of Construction.

It can be seen that directly bonding/soldering a chip to a cooling system significantly reduces the thermal resistances, enabling increased heat transfer. It is also seen that the direct bonding of a silicon chip to a ceramic-based cooling system is thermo-mechanically feasible, especially with the non-oxide ceramics (AlN and SiC).

Heat Spreading

Heat pipes are passive thermal dissipation devices capable of very high heat loads and have high apparent heat conductanceⁱⁱⁱ. This is accomplished by using the latent heat of vaporization to extract heat from a vaporizing section, transporting this “heated vapor” to a cooler region where the heat is released through condensing. The coupled effect of phase change and mass transport enable heat pipes to “conduct” heat much more effectively than thermal conductivity of solids. Heat pipes essentially pump heat from evaporator to condenser for heat rejection and back from condenser to evaporator for heat absorption.

Heat pipes are already implemented into high power electronics cooling systems^{iv}. The demand for heat removal in small packages makes this technology a preferred and viable solution. Many of these have relatively small cross sections resembling

a pipe, which can be bent and formed to fit within an electronics package. These pipes essentially allow for flow only along the axis of the heat pipe, limiting the capillary flow and the vapor flow. Hence the output is also limited. In order to increase the cooling capacity of these systems, multiple heat pipes are used in parallel configurations^v. More heat pipes leads to greater cross sections and hence greater cooling capacities. More recent heat pipes have migrated to the flat plate configuration^{vi} allowing for greater, multi-dimensional flows in the plane of the heat plates.

Ceramic Heat Design

The ceramic heat plate seeks to take advantage of 1) direct bonding to the electronics chip to minimize interface losses, and 2) planar heat plate configurations to maximize the heat spreading capabilities of multi-dimensional flows. Hence within this planar structure capillary wicks and counter-flowing gas channels are required. Without “a priori” defining where the chip is mounted or how many chips are mounted on the heat plate, these wicks should allow for either evaporation or condensation in any location. This can be accomplished by creating a wick structure with porous walls permitting flow communication

between the liquid capillary and gas flow channels. Likewise, the porous walls are ideal for fluid evaporation or vapor condensation whereby the high surface area provides for numerous sites for phase change initiation.

A simplified schematic of the heat plate is shown in Figure 2. The cross-sectional cut helps provide

understanding to the orientation of these layers and flow channels within the heat plate. This figure also includes photographs of the heat plate sections for further clarification.

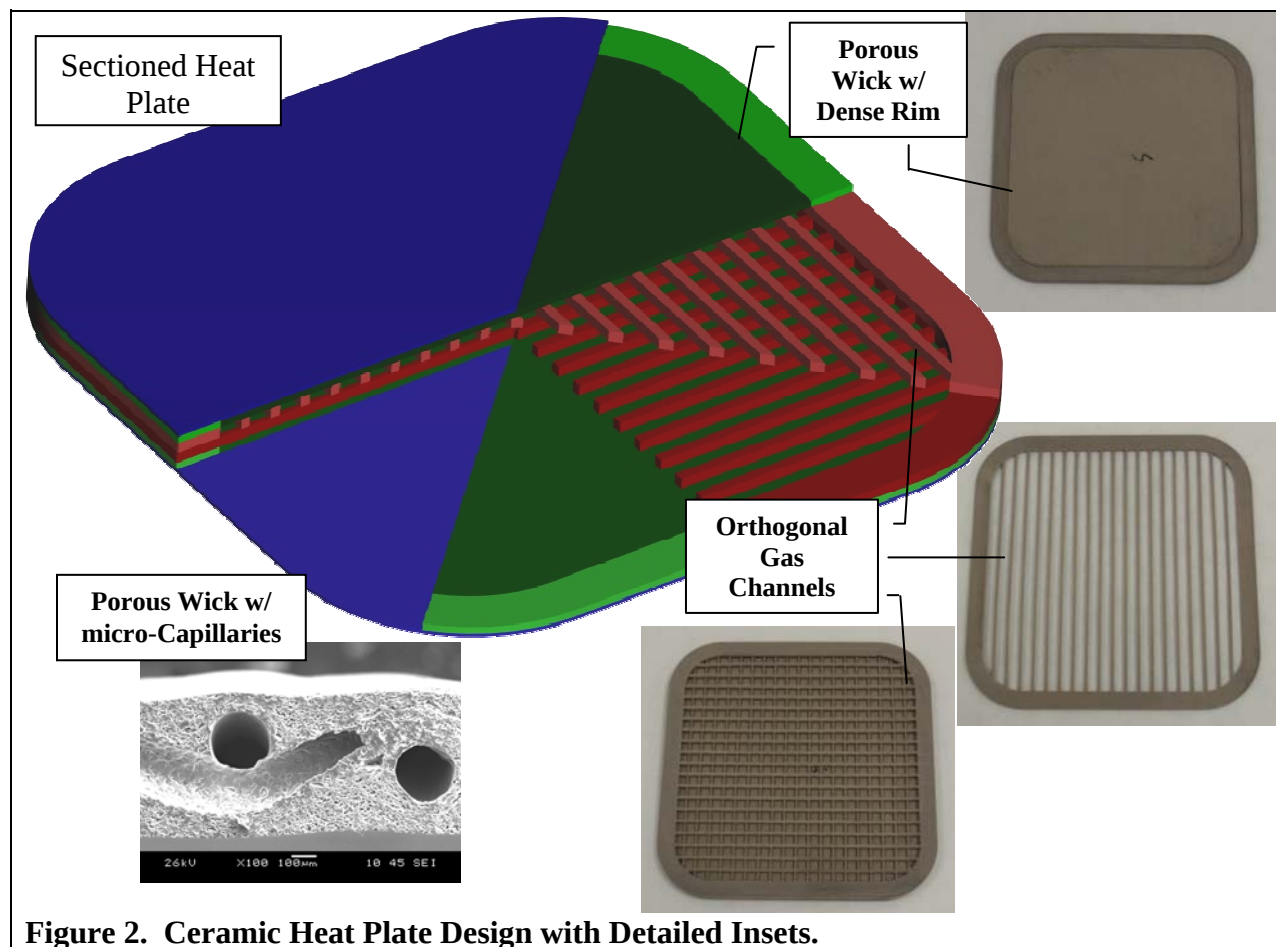


Figure 2. Ceramic Heat Plate Design with Detailed Insets.

Heat Plate Testing

As a closed loop passive system, the heat plate will have a uniform mass flow rate through the system; the vapor flow rate from evaporator to condenser will be equal and opposite to the liquid flow rate in the wick. Predicting the flow rate in this porous wick with the micro-capillaries is difficult due to the various length-scales. The pores are about 30 micron in diameter, the capillaries are about 240 micron in diameter, and the device is 50 mm x 50 mm. Hence, the permeability of the porous wick was determined by empirical testing. Correlations were derived so models could be used to estimate the flow rate within the 2-dimensional wicks of the heat plate.

Wick specimens were fabricated using similar processes as would be used in the fabrication of the

heat plate; however, the dense skin and the vapor channels which sandwich the wick were not included.

The wick specimens were tested using a vertical orientation such that the height of the fluid could be measured throughout the test. Given the porosity and void fraction due to the micro-capillaries, the volumetric flow was determined as a function of the capillary height. The time measurement for these tests was determined by the time stamp of the frames as it was captured on video. Selected frames of these tests are shown in Figure 3a and the correlation for the permeability is in Figure 3b. Dashed lines have been added to indicate the elevation of the fluid during the capillary tests.

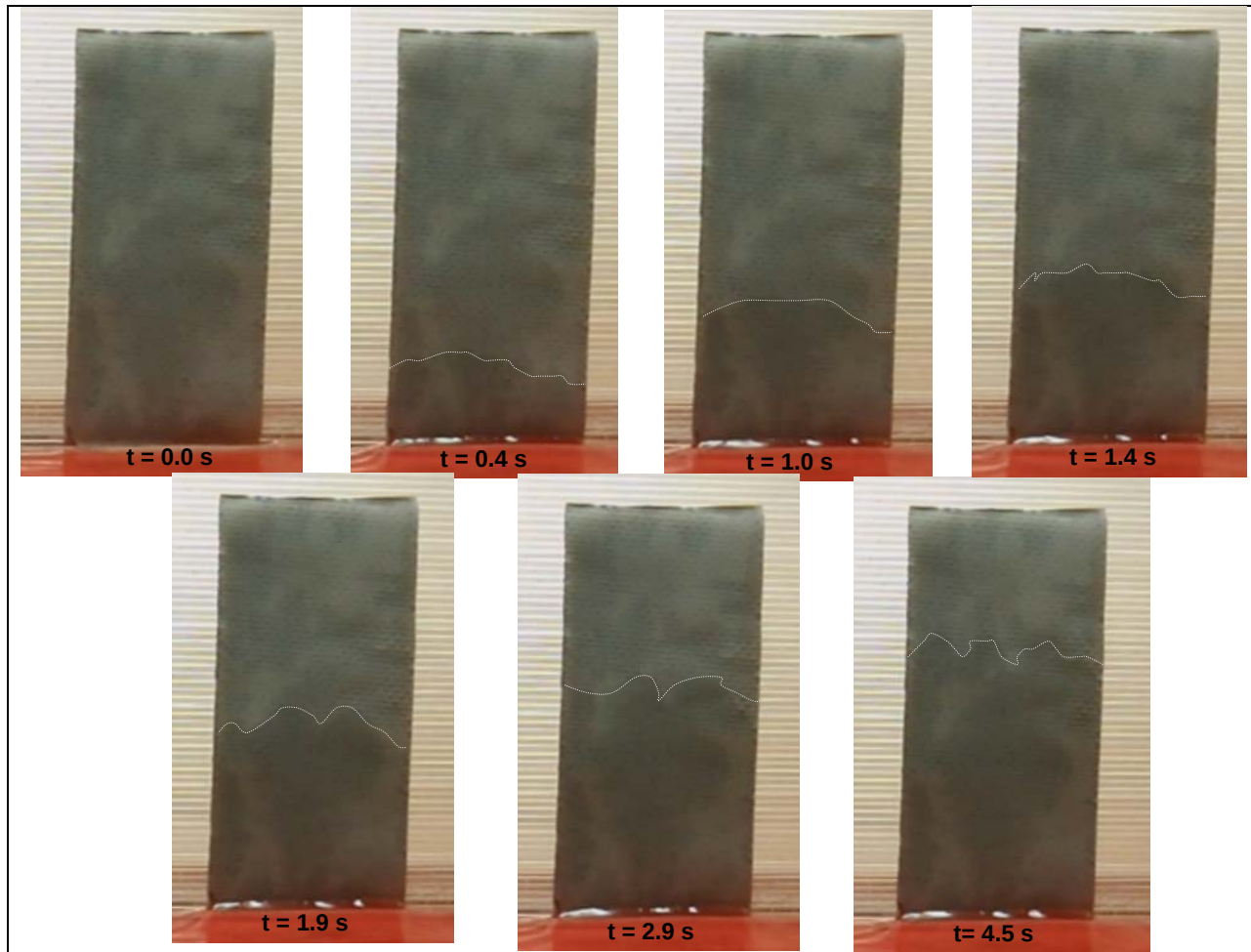


Figure 3a. Permeability Testing of the Porous Wick Structures.

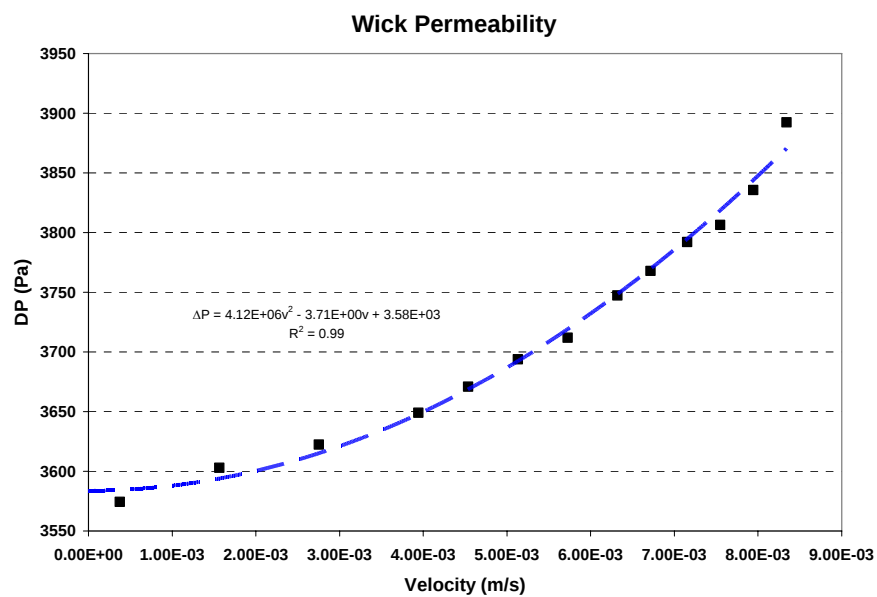


Figure 3b. Permeability Correlation of the Porous Wick Structures.

Heat Plate Modeling

Computational Fluid Dynamics (CFD) models were used to estimate the flow rate versus pressure drop for both the liquid wicking channels and the vapor channels. Under presumed operating conditions, the flow rate and pressure drop characteristics of these two flow paths should be balanced.

For the fluid wick model, the wick was treated as a porous material using the permeability correlation shown in Figure 3b; that is:

$$\Delta P = 4.12 \times 10^6 v^2 - 3.71v + 3.58 \times 10^3$$

where :

$P \equiv \text{pressure (Pa), and}$

$v \equiv \text{velocity (m/s)}$

The nominal pressure was assumed to be about $\frac{1}{2}$ an atmosphere, making the boiling point within the system about 80C. The pressure had little or no effect on these calculations in that the condensation and vaporization processes were ignored; only the fluid transport was considered. The boundary conditions included a specified flow rate from the perimeter, which was varied parametrically. The central region, presumably where the high power IC

would be located, utilized a continuity boundary condition using the nominal pressure as the reference pressure. Utilizing the symmetry of the heat plate, a one eighth section was modeled; a quadrant with only a single wicking layer.

For the vapor channel model, the orthogonal channels were modeled, again assuming $\frac{1}{4}$ symmetry. The vapor phase was water at $\frac{1}{2}$ an atmosphere. The inflow boundary condition also assumed a parametrically adjusted flow rate; however, it originated from the center region, flowing outward. The perimeter utilized the continuity boundary condition with the pressure set at the nominal $\frac{1}{2}$ an atmosphere. Because the velocities and flow channel dimensions are small, the vapor was modeled as a laminar, non-compressible fluid. Again, the condensation and evaporation processes were ignored in order to understand the flow characteristics of the channels.

The results of these analyses are found in Figure 4a-c. The first plot shows the pressure distribution in the porous wick. The following plot indicates the pressure distribution of the vapor channels. The last plot is a summary of the parametrics comparing the pressure drop vs. mass flow rate of both systems.

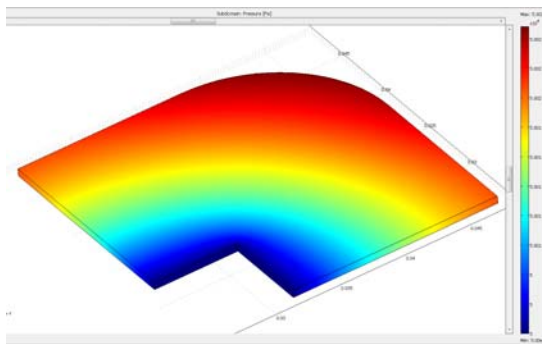


Figure 4a. Pressure Drop in Wick

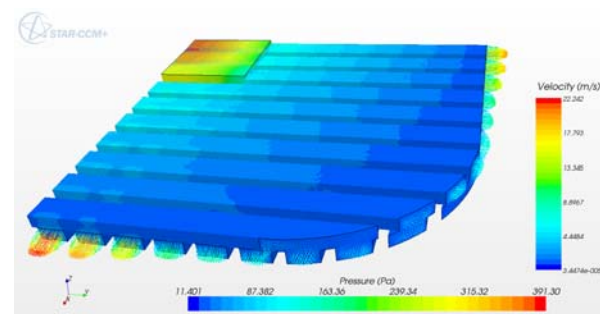


Figure 4b. Pressure Drop in Vapor Channels

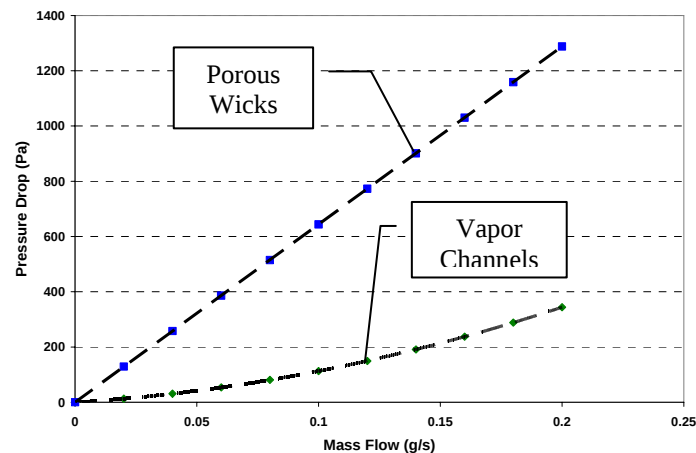


Figure 4c. Pressure Drop Characteristics for Heat Plate.

From the analyses, it can be seen that the pressure drops for either the wicking channels or the vapor channels is quite low. Even at a flow rate of 0.2 g/s, the high pressure drop wicking channels results in only about 1200 Pa, or about 1% of atmospheric pressure. Assuming a mass flow rate of 0.2 g/s throughout the system and given the latent heat of water, this system should be able to provide about 400-500 Watts of cooling.

It can also be seen that at any given flow rate these pressure drops are not in balance; typically, the pressure drop in the porous wick is about 3 times that of the vapor channels. This would indicate that in this preliminary design and throughout the operating regime, the wicking channels would likely limit the performance of the heat plate.

Conclusions and Future Work

By selecting thermo-mechanically matching materials with electronic chip materials, it seems feasible that these ICs can be direct bonded to the cooling system to minimize the thermal interface resistances due to poor contact and thermal contact

greases. The direct bonding of an IC to ceramic-based cooling systems will also result in minimal residual stresses which may allow for long life durability even with thermal cycling.

The preliminary design of this heat plate has resulted in low pressure drops within the porous wick and in the vapor channels. And although these to flow networks are yet to be optimized and balanced, the systems should be able to cool systems with significant heat loads (400-500W).

Future developments of these ceramic-based heat plates will include:

- 1) Iterating and optimizing of engineering designs with the manufacturing processes such that the flow networks are more closely balanced, and
- 2) Fabrication and testing of prototypical systems to evaluate their cooling performance under operating conditions such that the effects of vaporization and condensing can be included.

ⁱ Chia-Ken Leon, D.D. Chung, "Carbon Black Dispersions and Carbon-Silver Combinations as Thermal Pastes that Surpass Commercial Silver and Ceramic Pastes in Providing High Thermal Contact Conductance", Carbon, Vol 42, pp 2323-2327, June 2004.

ⁱⁱ Xiangcheng Luo, D.D.L. Chung, "Effect of the Thickness of a Thermal Interface Material (Solder) on Heat Transfer Between Copper Surfaces", International Journal of Microfluidics and Electronic Packaging, Vol 24, number 2, Second Quarter 2001.

ⁱⁱⁱ <http://www.amecthermasol.co.uk/AmecThermasolFlatCoolPipes.html>

^{iv} <http://www.electronics-cooling.com/1996/09/heat-pipes-for-electronics-cooling-applications/>

^v J. Weyant, S. Garner, M. Johnson, and M. Occhionero; "Heat Pipe Embedded AlSiC Plates for High Conductivity – Low CTE Heat Spreaders", http://www.1-act.com/pdf/Hi-K_AlSiC_June_2010.pdf

^{vi} Matt Connors, "Vapor Chambers Improve Cooling of Power Semiconductors", Power Electronics Technology, April 2010.