Ultrathin WLP Die Embedded Polyimide Multilayer Wiring Board

S. Okude,

M. Okamoto, Y. Sano, N. Ueta and O. Nakao

Electron Device Laboratory, Fujikura Ltd.

okude@lab.fujikura.co.jp

IMAPS DPC(8th March 2011)

Contents

- Background
- Technical overview of the proposed embedded board
  - Wafer Level Packaging for embedding
  - Multilayer polyimide wiring board fabrication process
  - Fabricated results
- Reliability Issues
  - Applicable die size
  - Bending stress
  - Environmental tests
- Applications
- Conclusion

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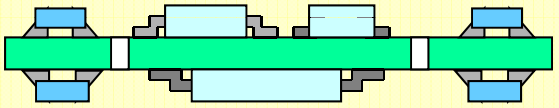
Background

- Evolution of Wiring Boards

Double-sided Board



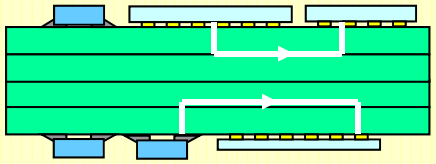
Footprint size =

=Wiring+Σ(Components)

Multi-Layer Board

Footprint size

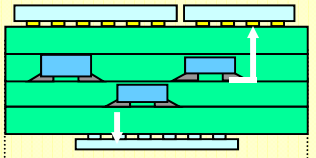
~Σ(Components)



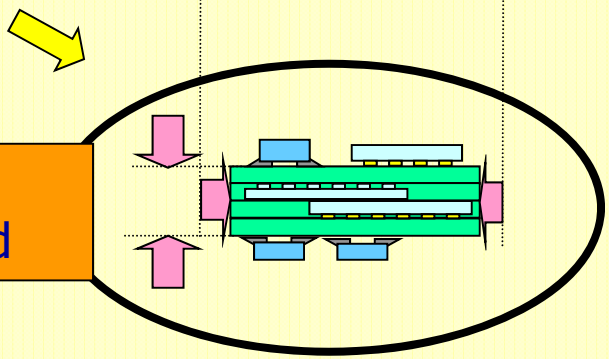
Embedded Board

Footprint size

<Σ(Components)



Passive Embedded



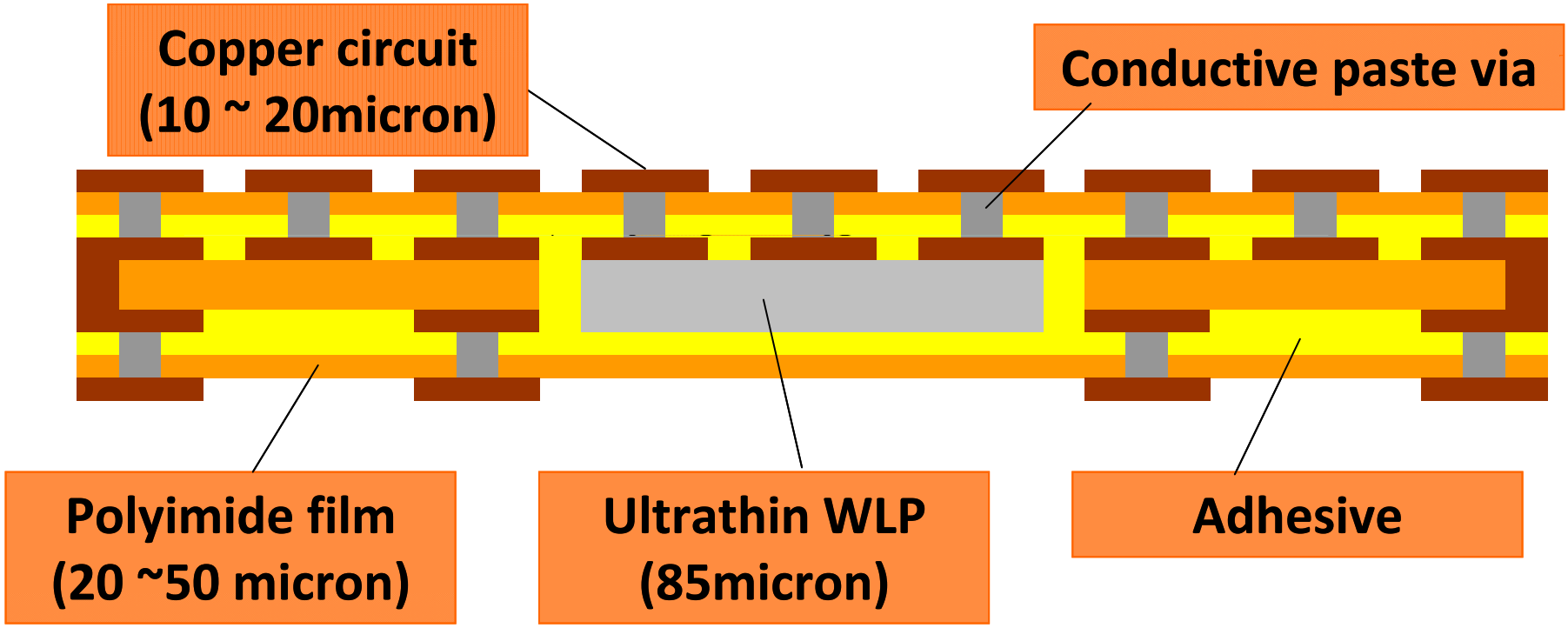
IC Embedded

*Effective to shrink board footprint

*Effective to shrink board thickness

Basic structure of the embedded board

Wafer And Board level device Embedded Package

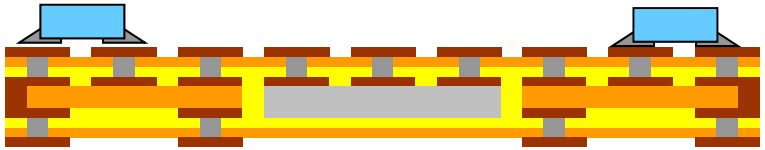
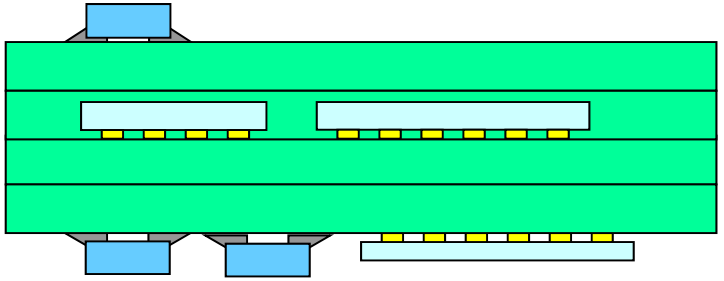


(1) Ultrathin WLP

(2) Flex based multilayer wiring board

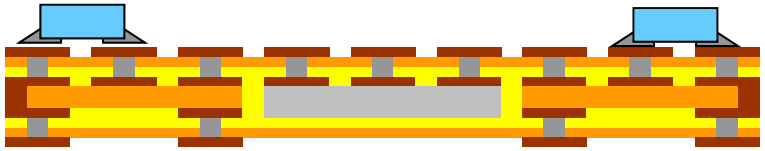
(3) Interstitial Via Hole filled by Conductive paste

Comparison of embedded board technology

Proposed structure		General Embedded board
		
Polyimide+Adhesive	**Material**	Glass Epoxy
WLP-IC	**Device**	WLP-IC, Bare die, Passive components
Conductive paste	**Joint**	Solder, Au bump,..
220 microns	**Thickness**	500 – 1000 microns
Soft and Flexible	**Thickness**	Solid, hard to bend

The Aim of this work

Proposed structure



Polyimide+Adhesive

WLP-IC

Conductive paste

220 microns

Soft and Flexible

Do these features affect on its reliability?

To investigate the effect of
Die size vs. Thermal Stress,
Bending Stress,
Environmental tests

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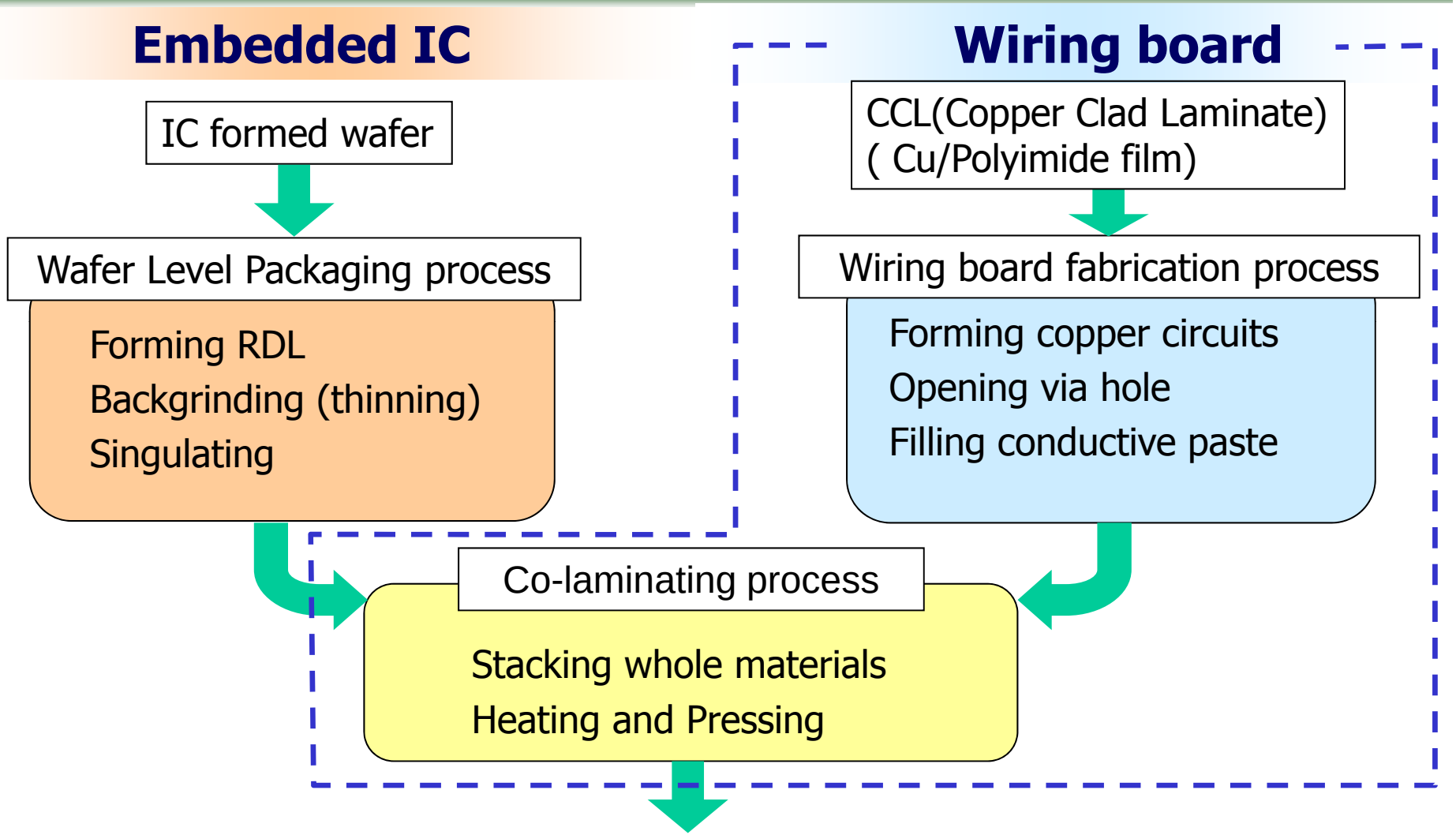
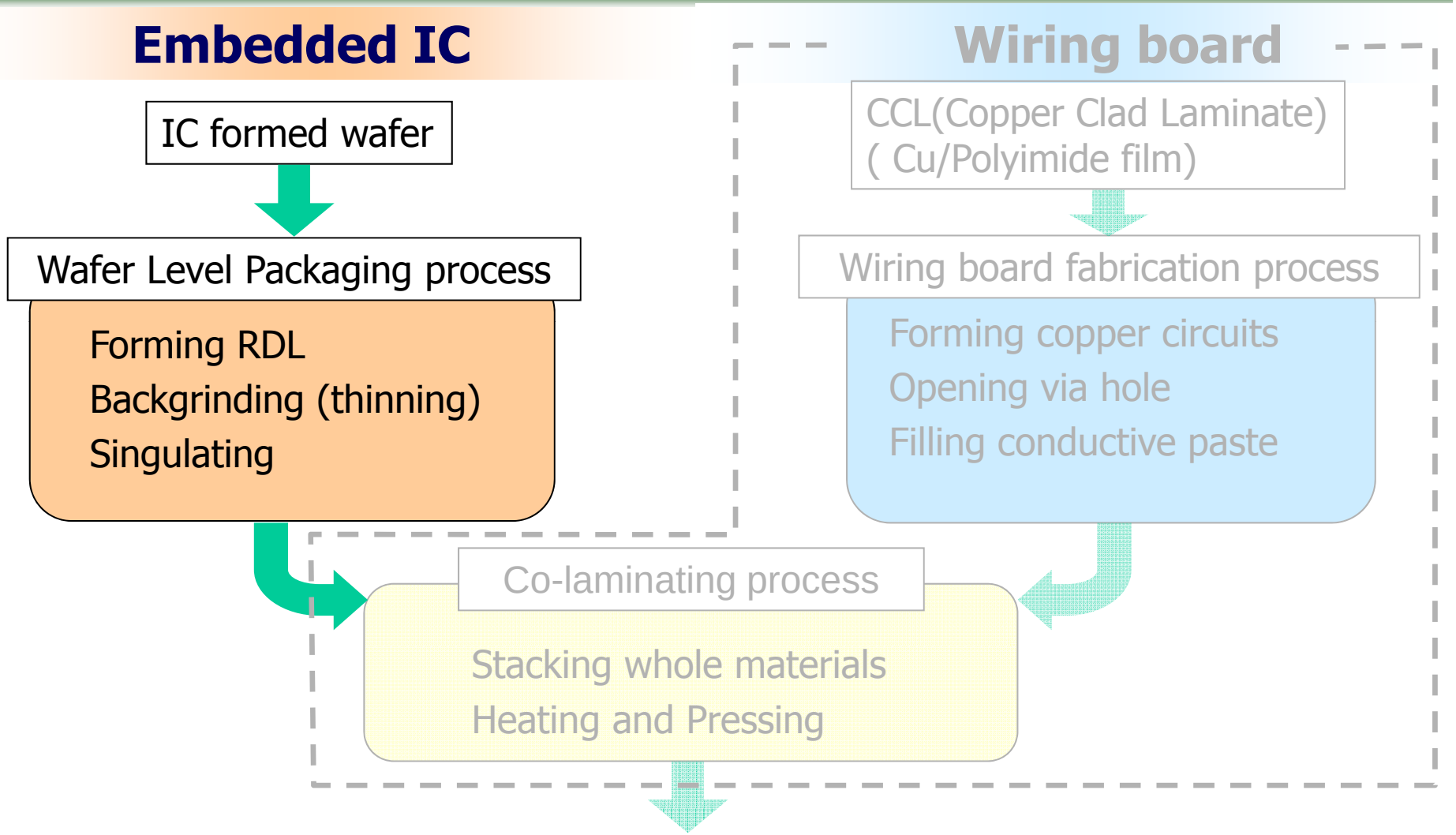
Fabrication Flow



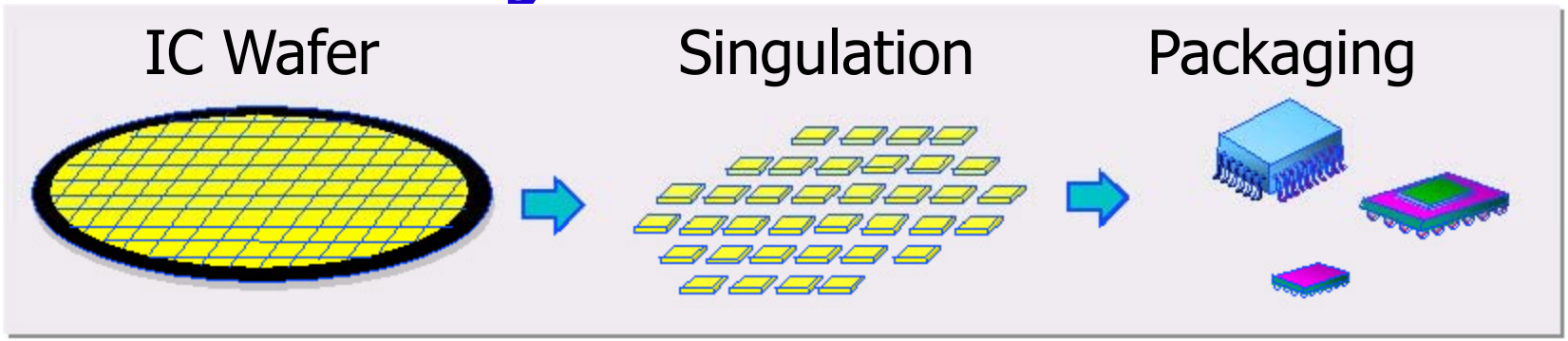
Fabrication Flow



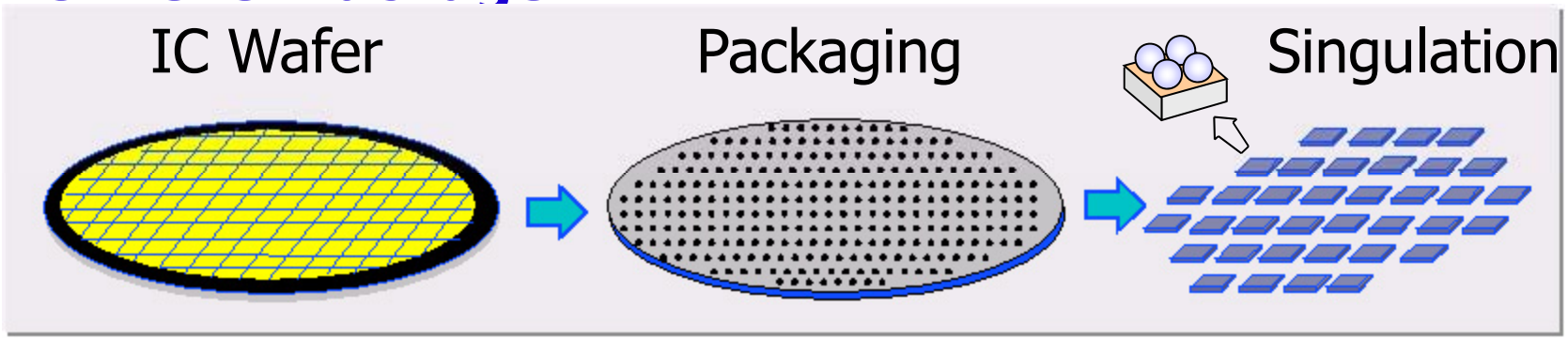
What is WLP?

- Wafer Level Packaging (WLP, WLCSP)

Conventional Package

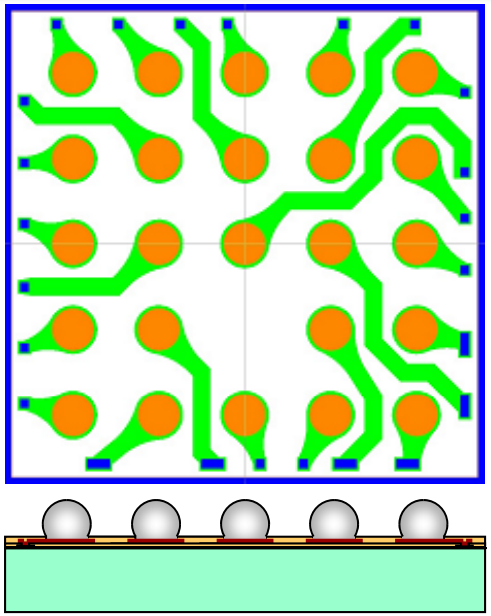


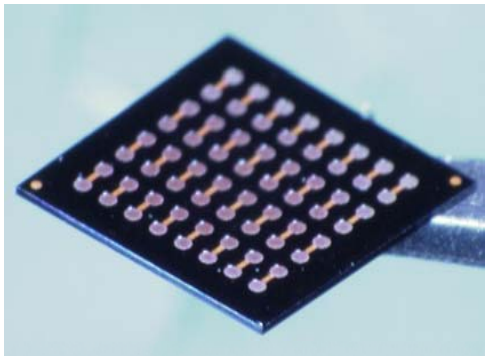
Wafer Level Package



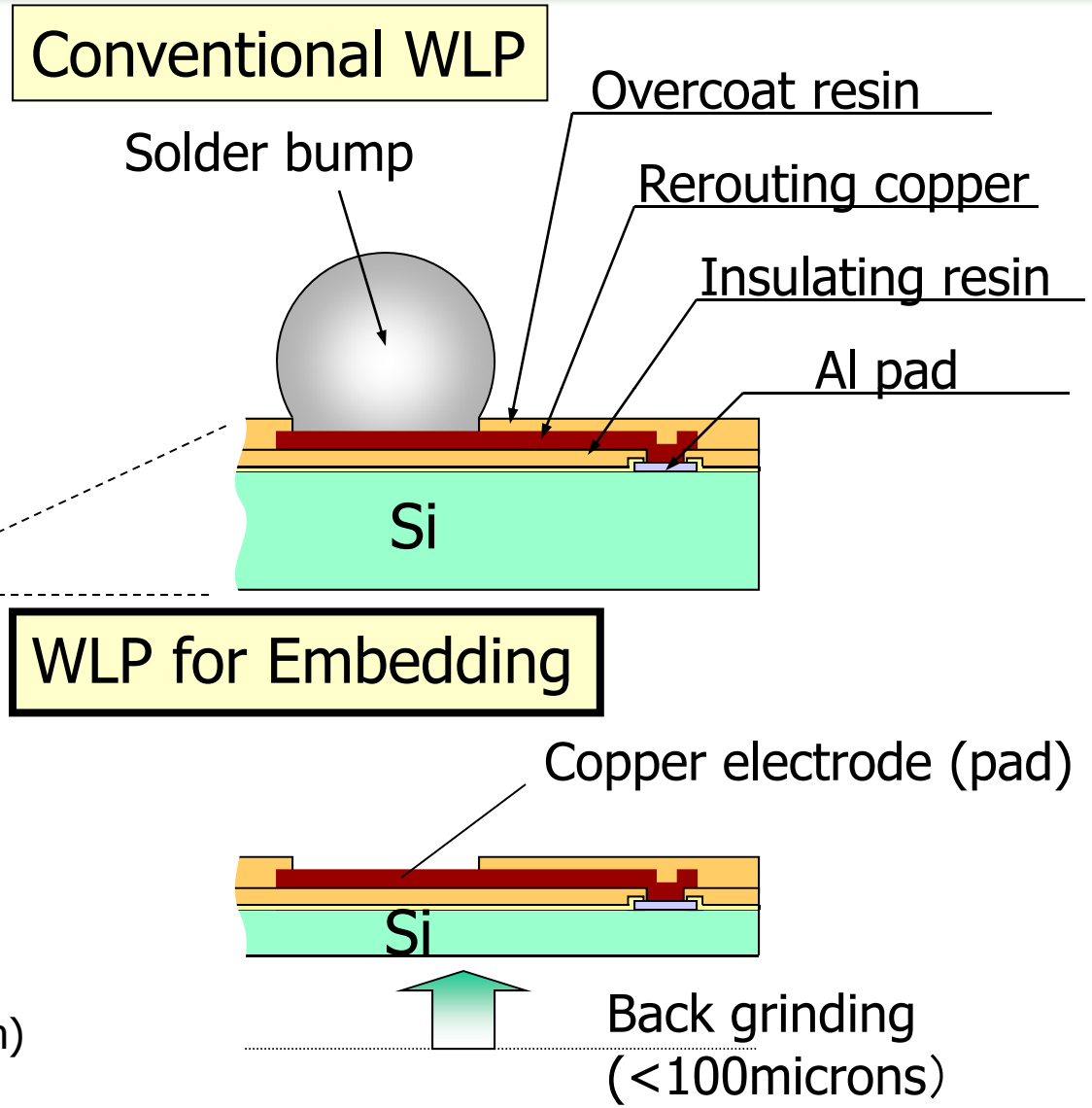
Die Size = Package Size ➡ ***Ultimate small IC Package***

Structure of WLP for embedding

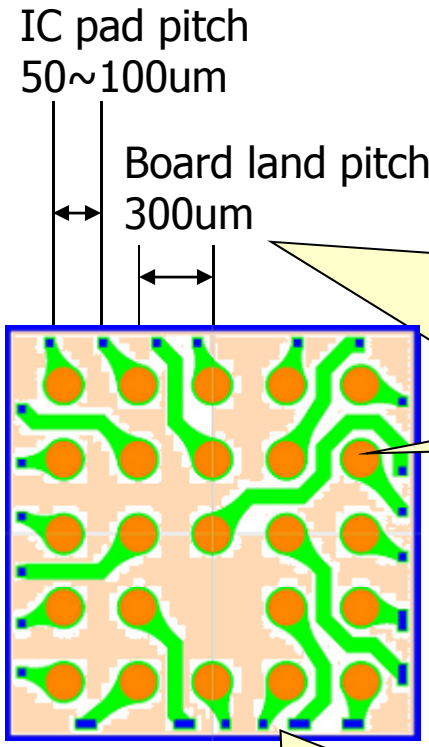




(TEG WLP: 3 x 3 x 0.085mm)



Why WLP ?



I/O pitch conversion

・Expand electrode pad pitch to fit board level design rules

Copper electrode

・Easy to connect to board level circuit
（Plating, Solder, Conductive paste）

Rerouting pattern

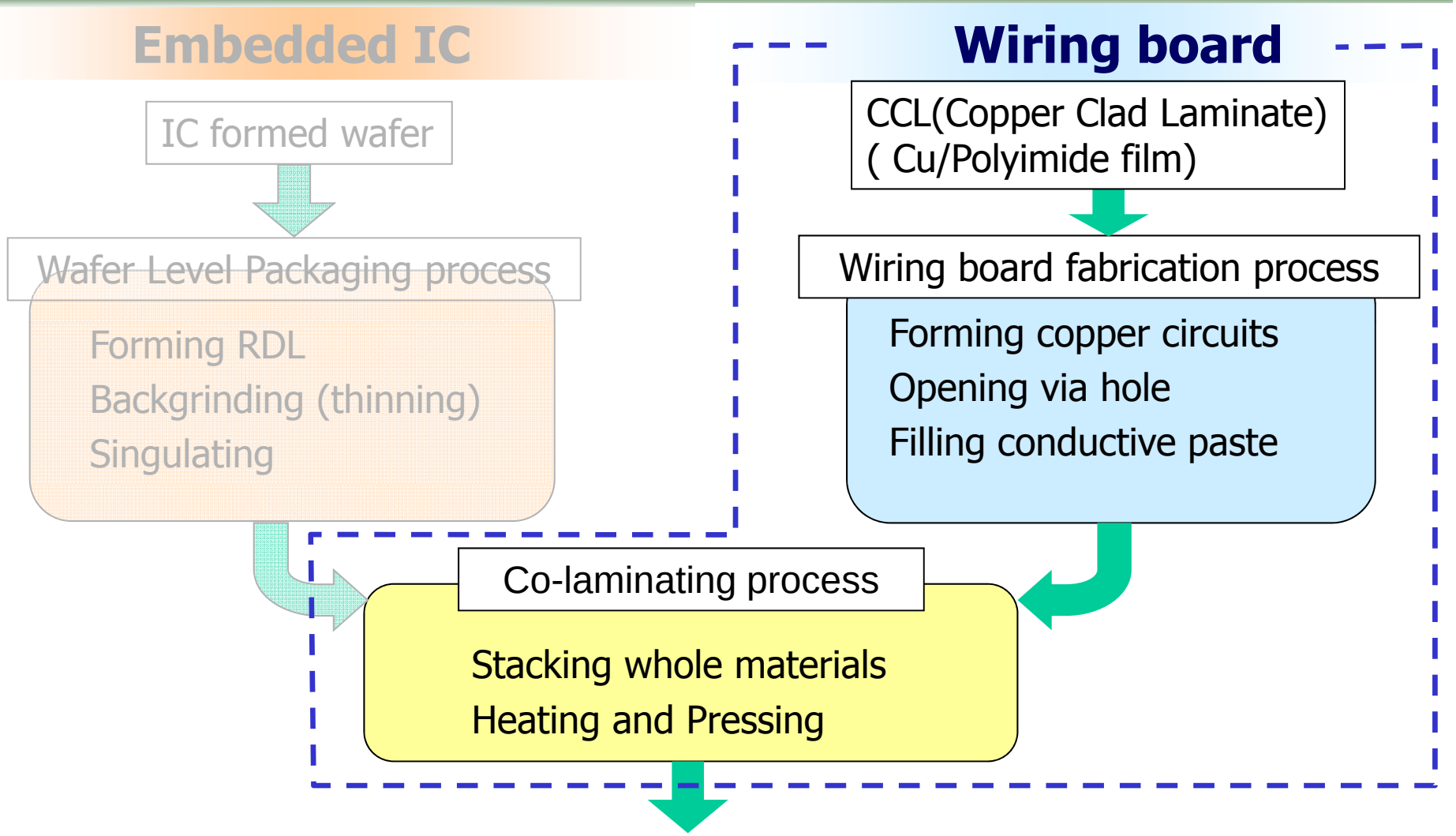
KGD（Known Good Die）

・To assure all embedded die is good
・High yield

Standard wiring board process can be employed for embedding process

(Cost effective)

Fabrication Flow



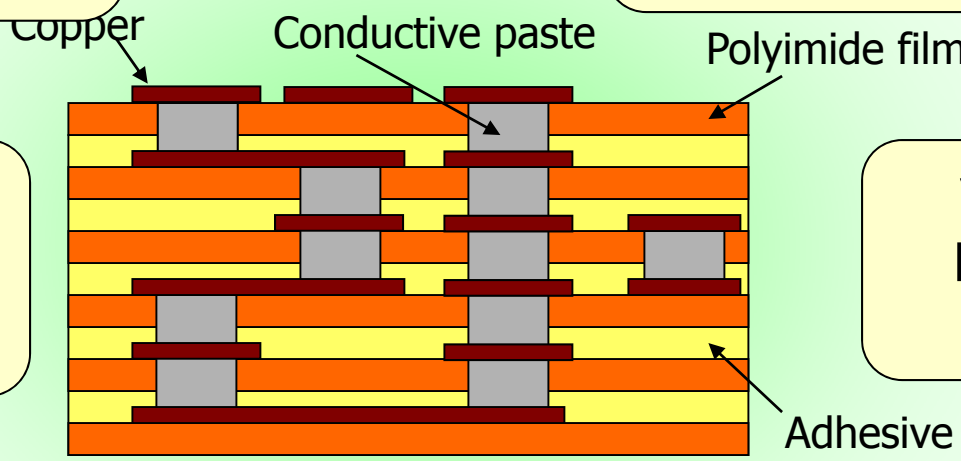
Polyimide Multi-layer Wiring Board

All Polyimide Interstitial Via Hole Colaminated ; APIC

Low cost process
by Co-lamination process
(not build-up process)

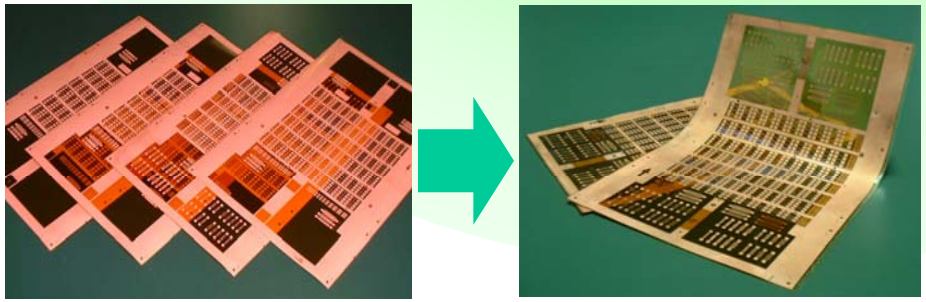
Thin Multi-layer board
based on polyimide film
(<300um / 6layer)

Cross sectional schematic



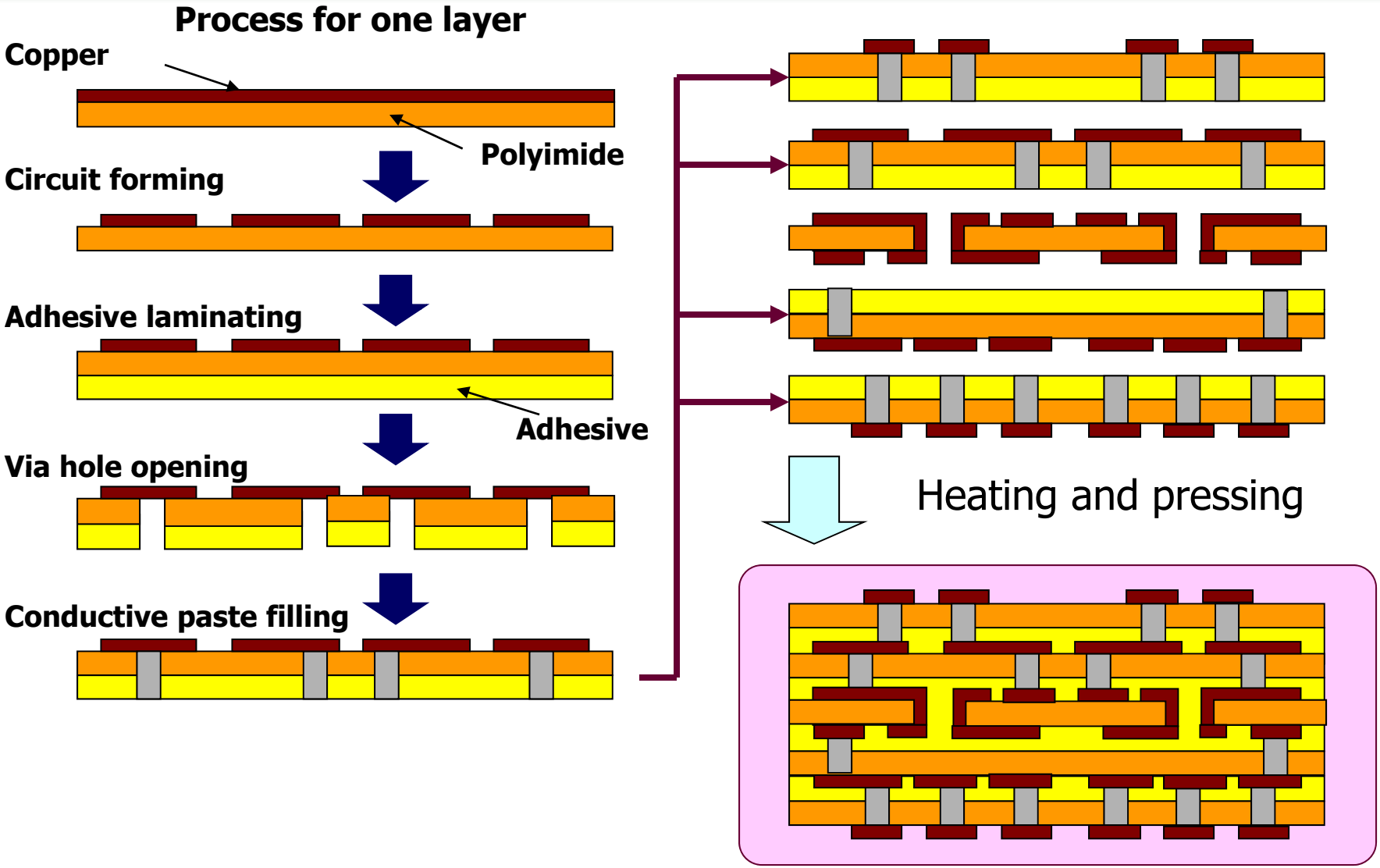
High wiring density
by Interstitial Via
Hole Structure

Via on Via
Pad on Via
Structure



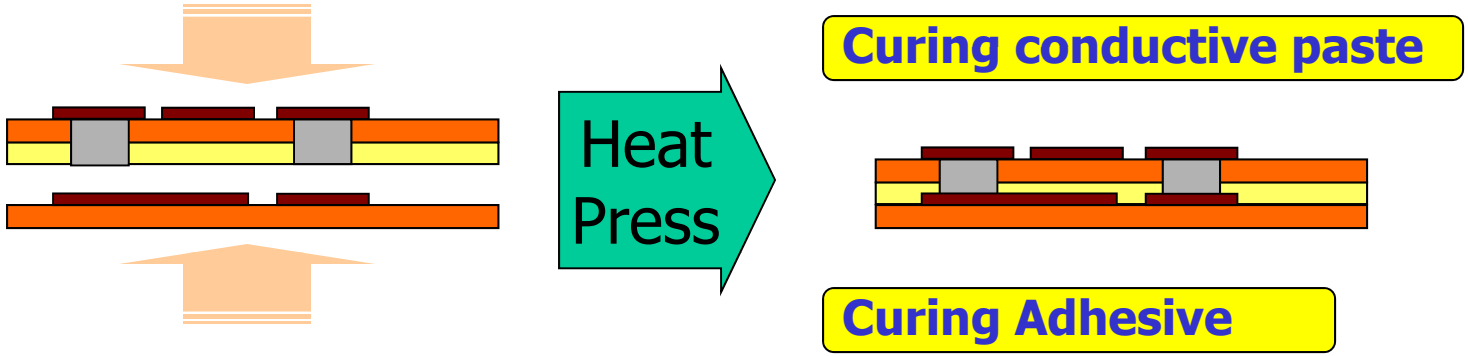
Filled via structure
by conductive paste

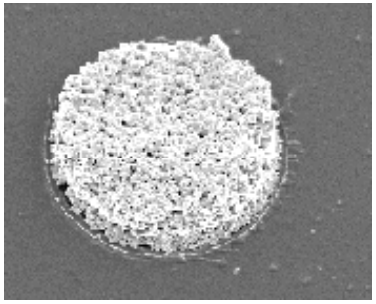
Fabrication process of the embedded board



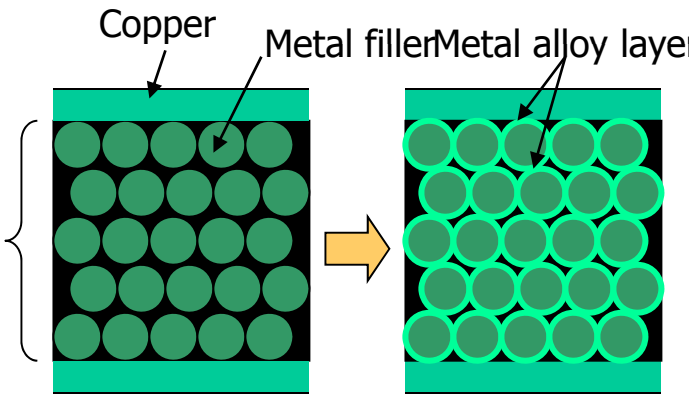
Via Structure

Via is filled by metal sintering type conductive paste

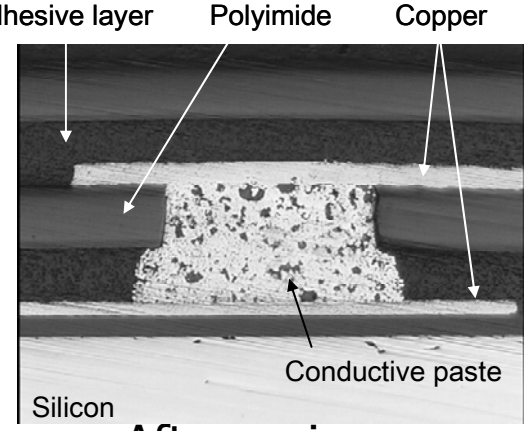




Before curing
(paste surface)

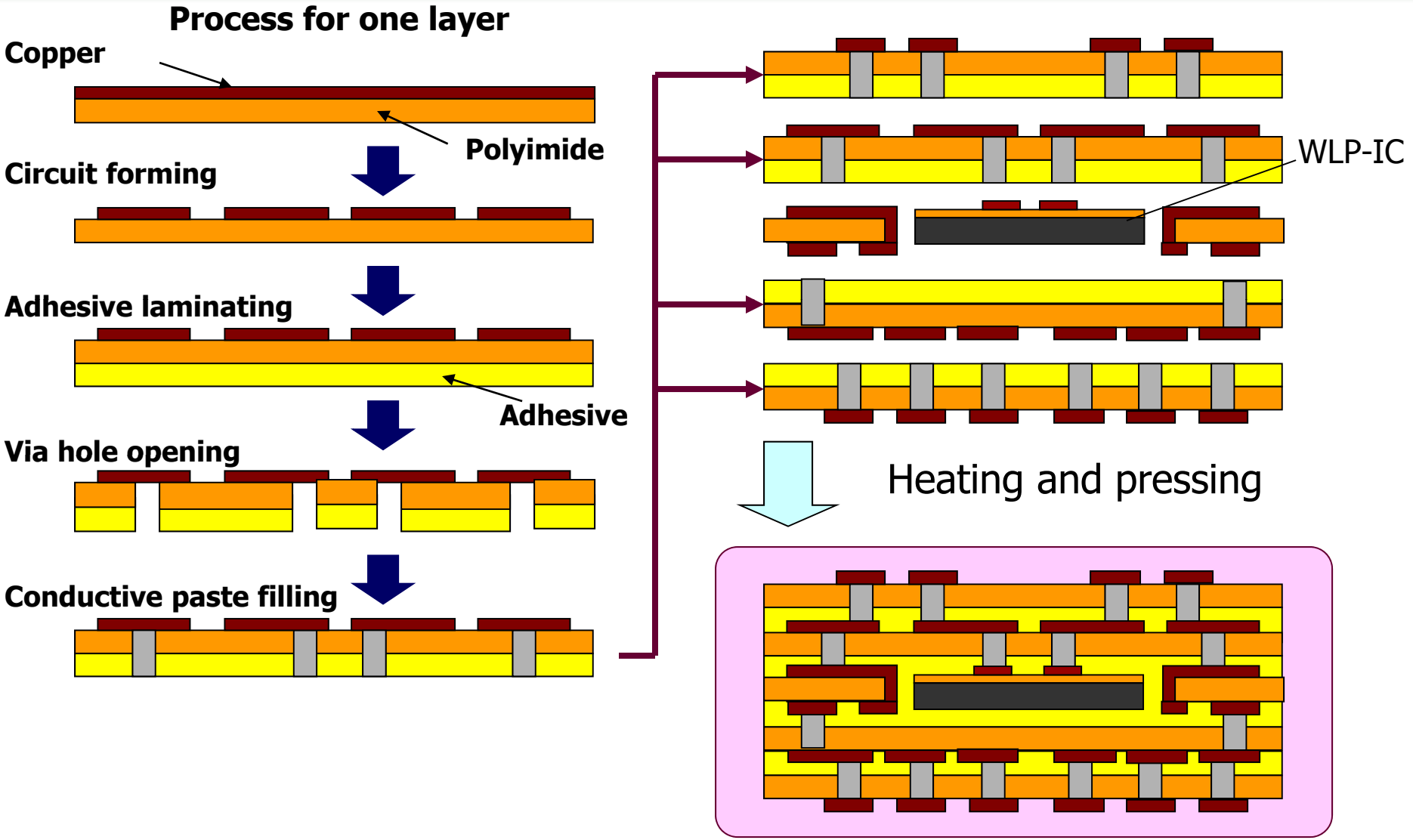


Schematic of paste curing



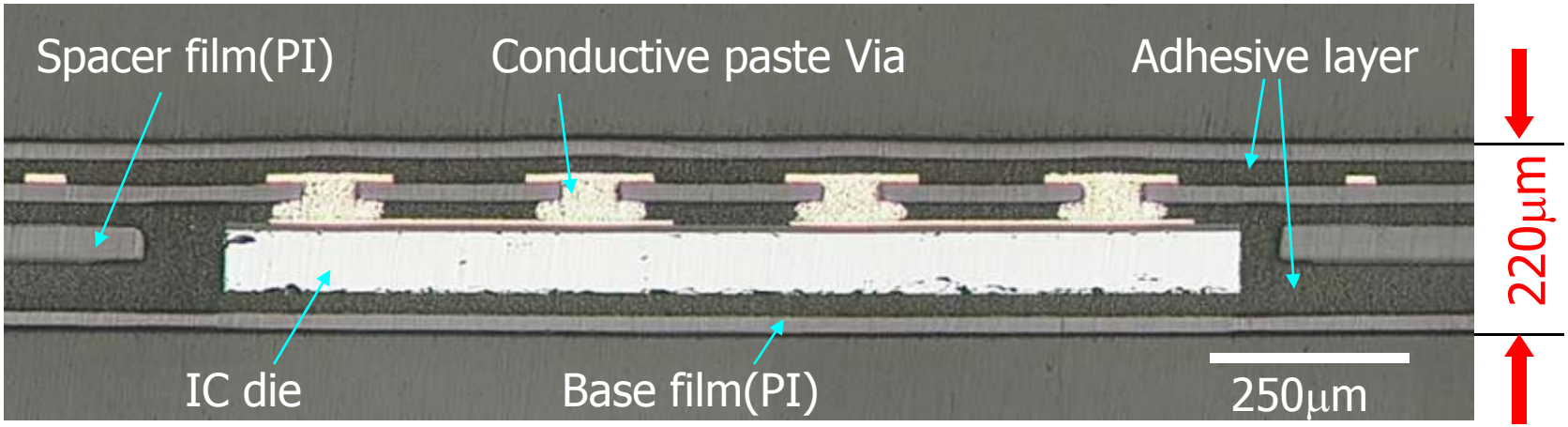
After curing
(Cross section)

Fabrication process of the embedded board



Fabricated Results

Cross-section photograph of a TEG board



Total board thickness	220μm
Embedded WLP die dimensions	1.2mm x 1.2mm x 85μmt
Interstitial via diameter	80μm
Interstitial via pitch	300μm

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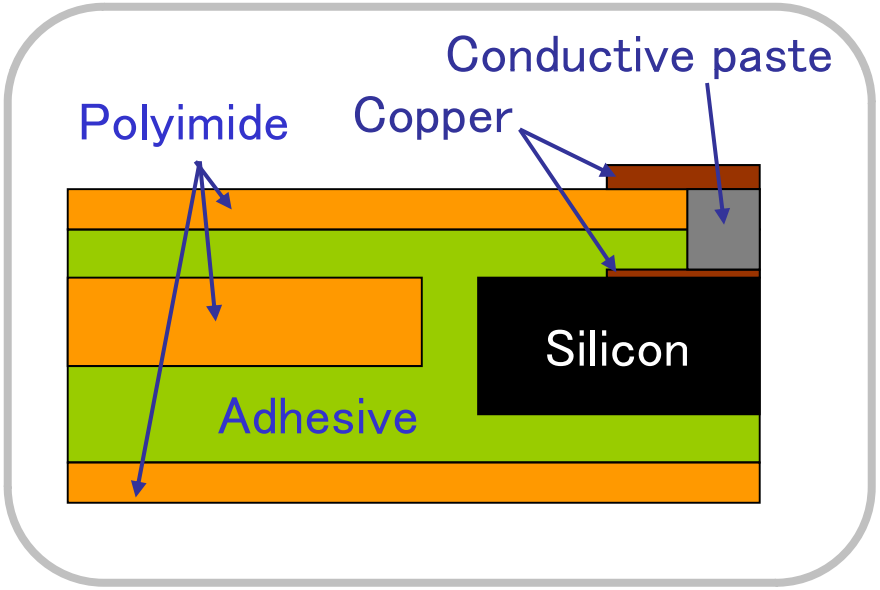
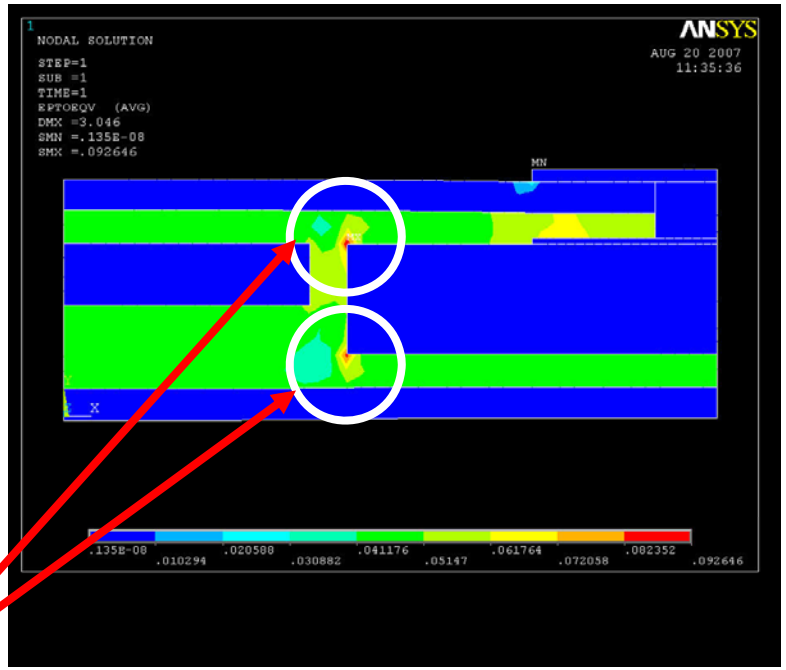
Reliability (I) : Applicable die dimensions

FEM simulation of internal strain distribution under certain temperature change

Simulation model



Results (Temp:25℃->150℃)

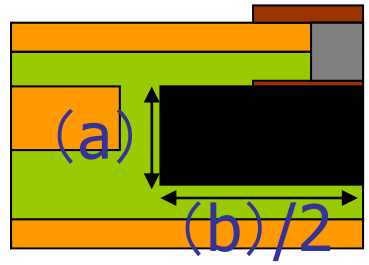


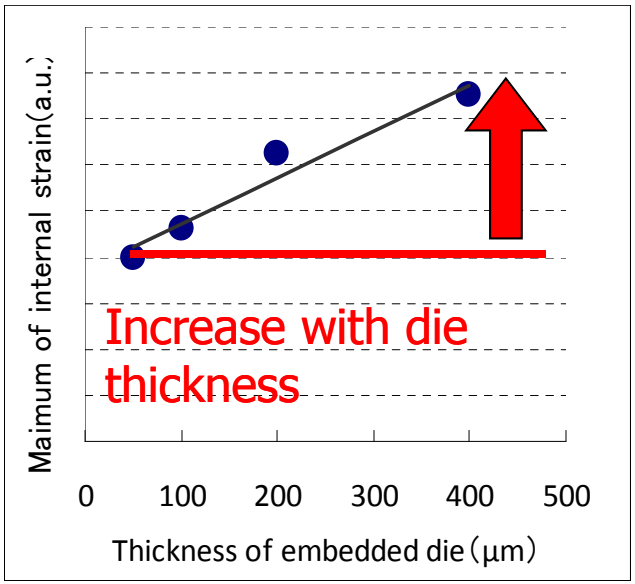
Largest internal strain appeared in adhesive around the edge of the embedded die

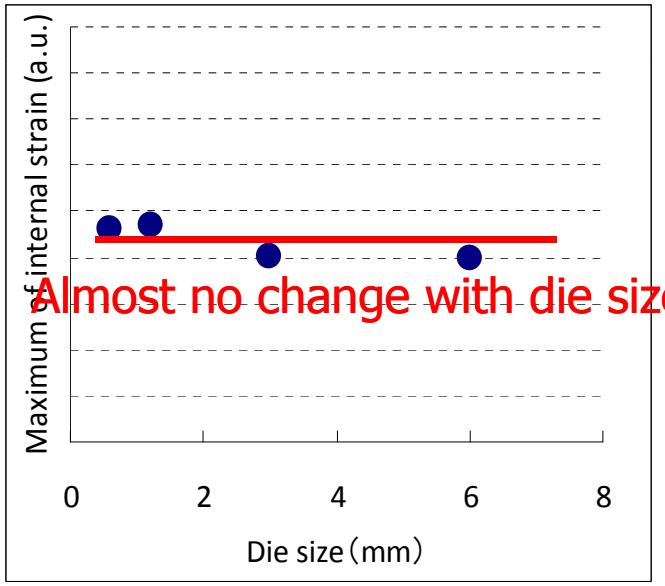
Reliability (I) : Applicable die dimensions

Influence of die dimensions on internal strain

Parameters: (a) Die thickness
(b) Die size (length of one side)





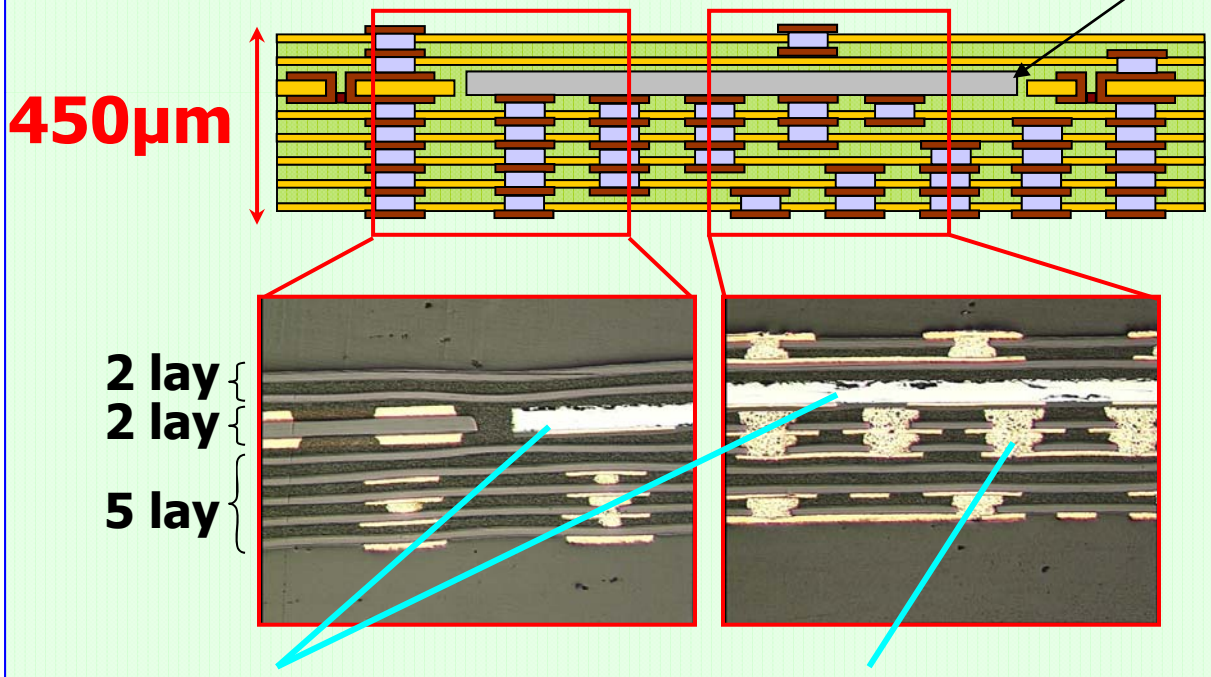


Internal stress can be reduced by thinning the die
The footprint size of the die doesn't degrade the reliability

Large die embedded WABE Package

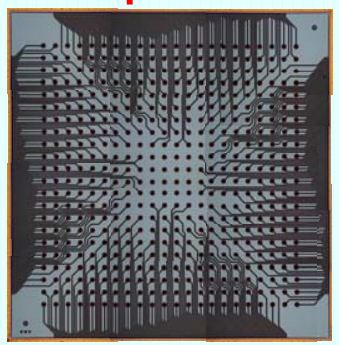
Cross sectional photo

TEG board structure (9 wiring layers)



Enlarged view of cross section

[WLP Size]
8mm × 8mm
85µmt
[Pad pitch]
0.30mm
[Pin counts]
464pin

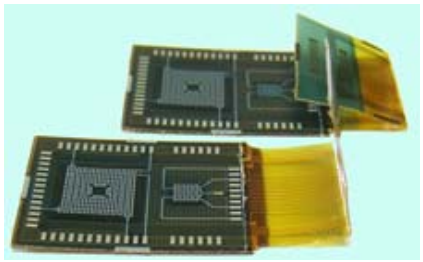


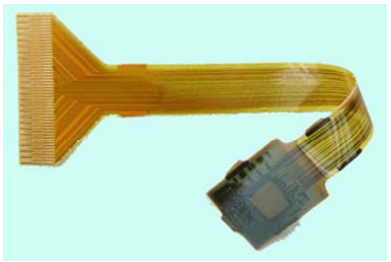
WLP RDL pattern

Reliability (II) : Bending durability

Features

Thin & Flexible

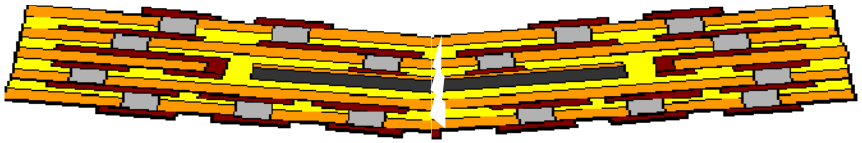




Concerns

Break of the embedded die

Resistance change of conductive paste via



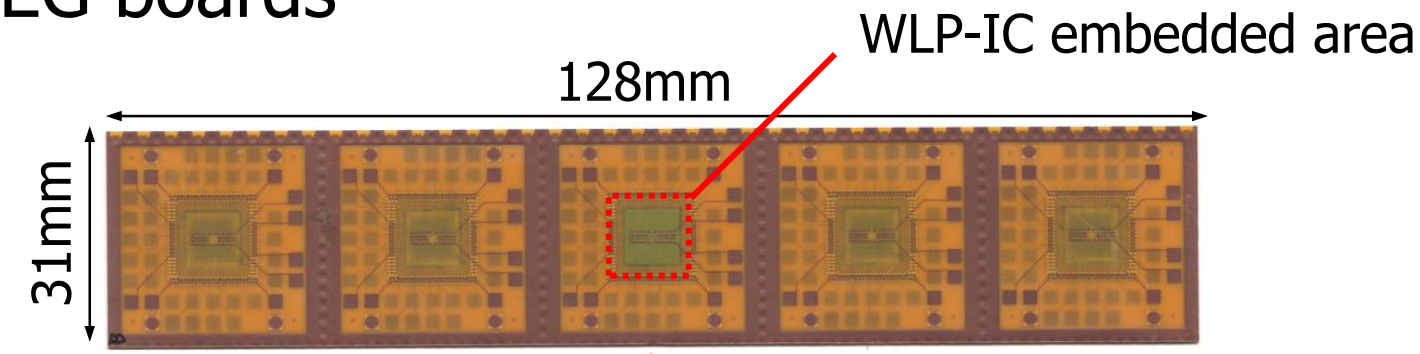
Aim of this test

Quantitative evaluation of the bending durability of the embedded board

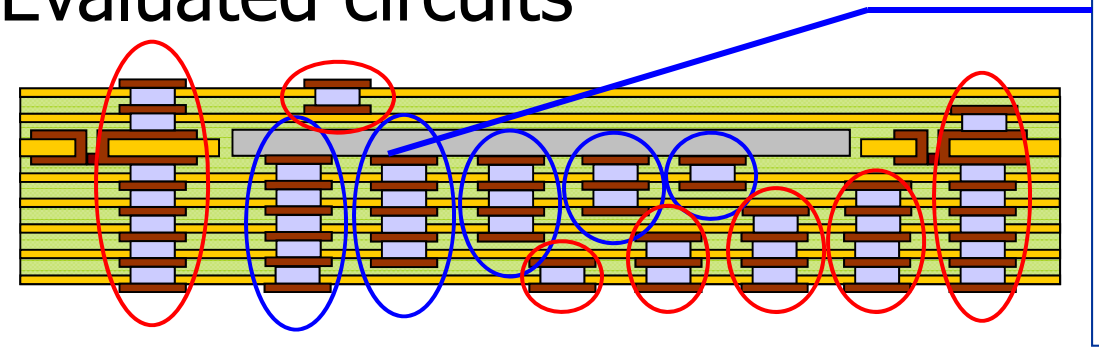
Bending limit test, Bending cycle test

Reliability (II) : Bending limit test

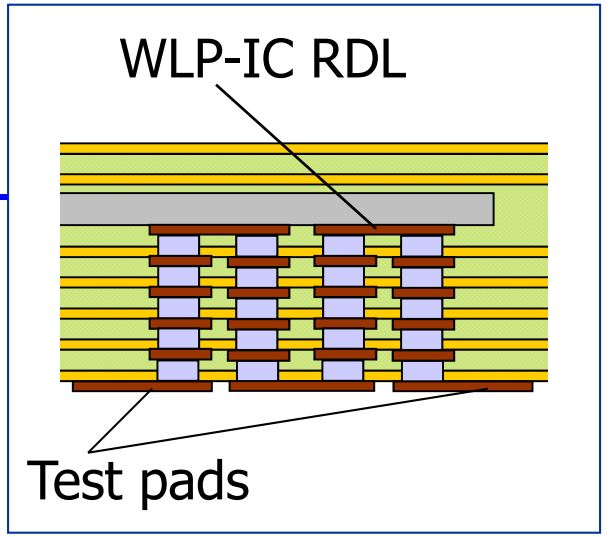
- TEG boards



- Evaluated circuits



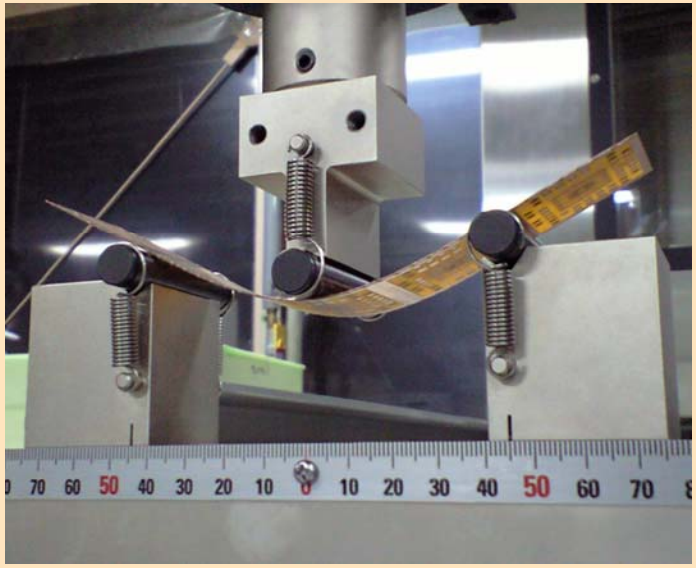
Cross section schematic



Reliability (II) : Bending limit test

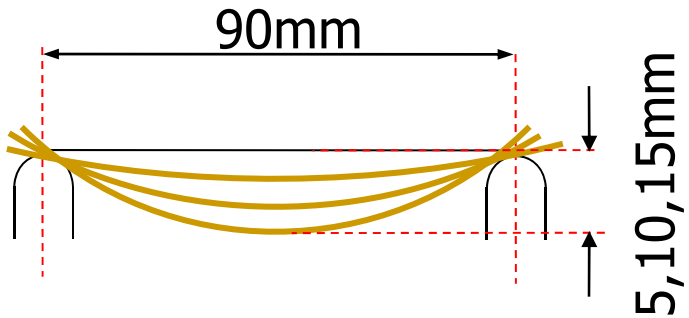
- Test conditions

Supporting span	Bending speed	Radius of supporter
90mm	10mm/min	5.0mm



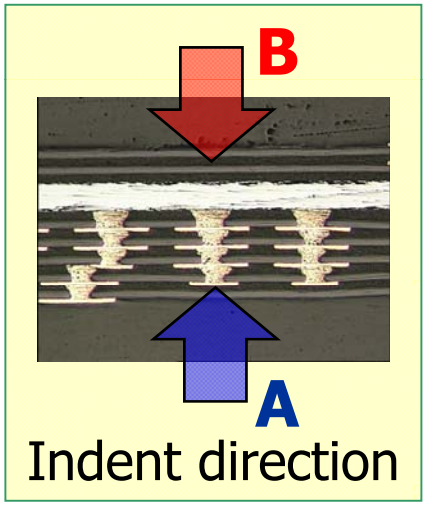
Test apparatus

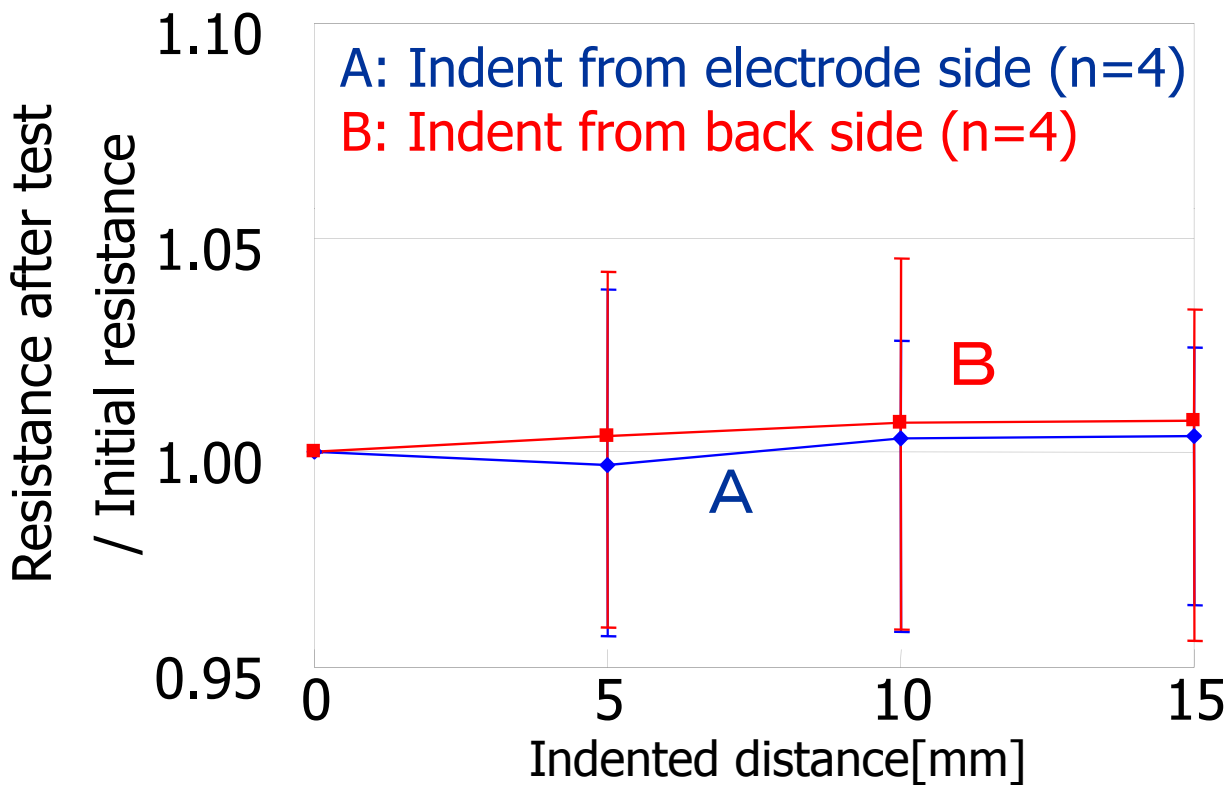
（Autograph/ SHIMADZU）



Tested under 15mm indentation

Reliability (II) : Bending limit test

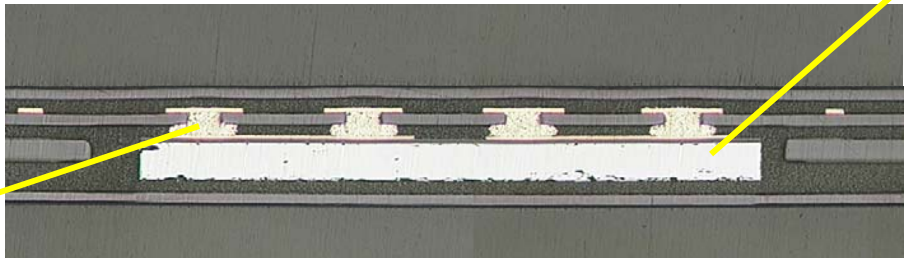




Max. resistance change : less than 5%

Reliability (III) : Environmental test

Cross section of TEG board



Test Item	Conditions	Result
Moisture Reflow Test	85degC, 60%RH, 168hrs 260degC peak reflow 3 times （compliant to M.S.L. JEDEC Level.2）	Passed （n=24）
Heat Cycle	Precondition : M.R. JEDEC Level2 -25degC, 9min / 125degC,9min 1000times	Passed （n=24）
HAST	Precondition : M.R. JEDEC Level2 130degC, 85%RH, 192hrs, No bias	Passed （n=24）

Criteria: Relative resistance change :<20% / Appearance: No void and de-lamination

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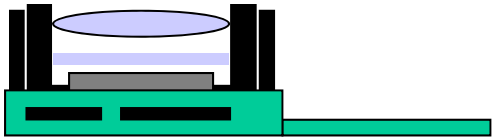
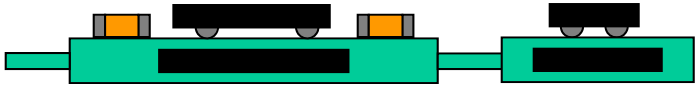
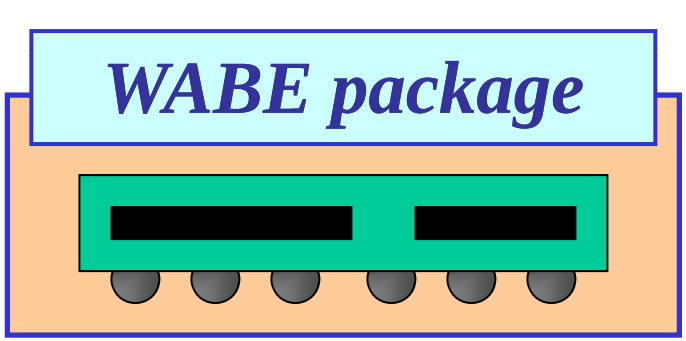
Application

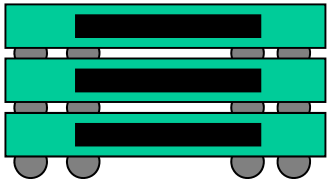
Module board



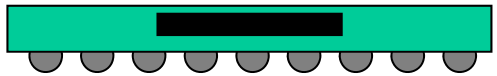
Main/Sub board for mobile phone





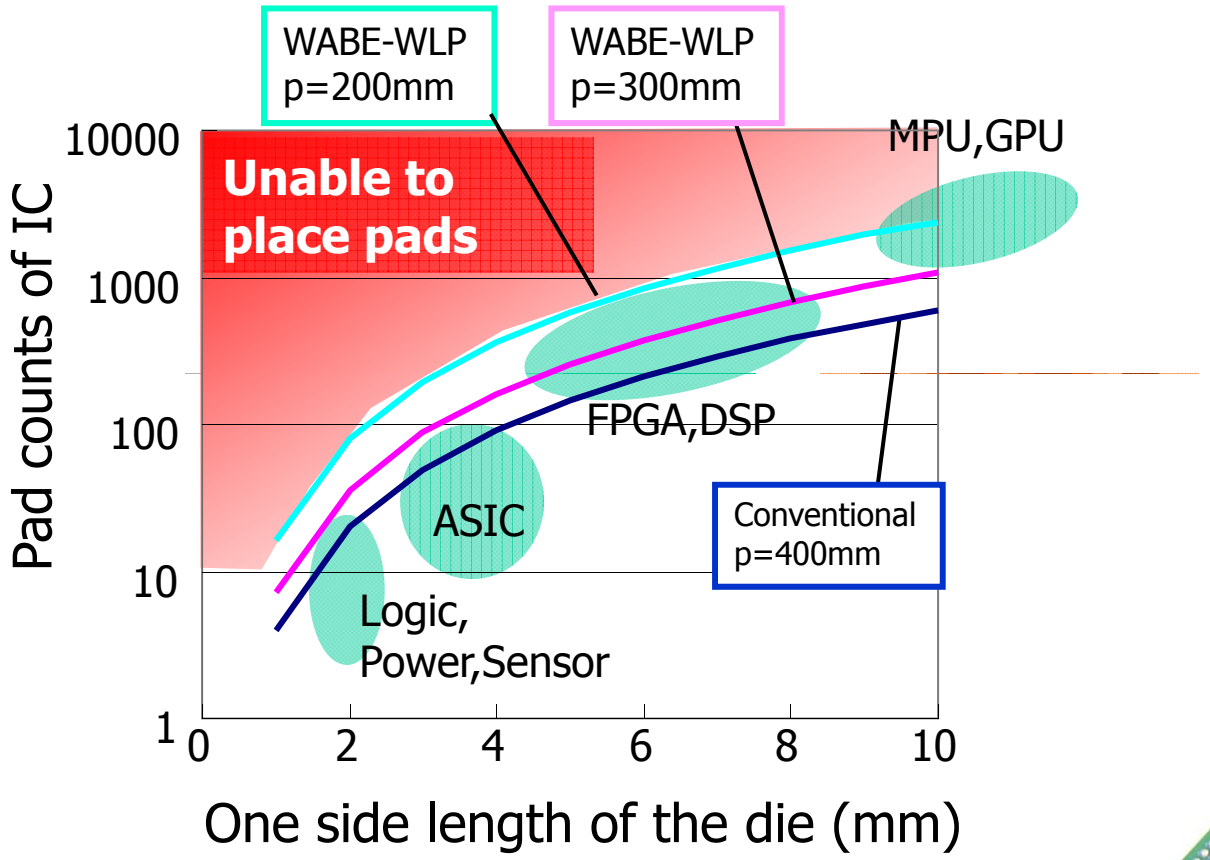


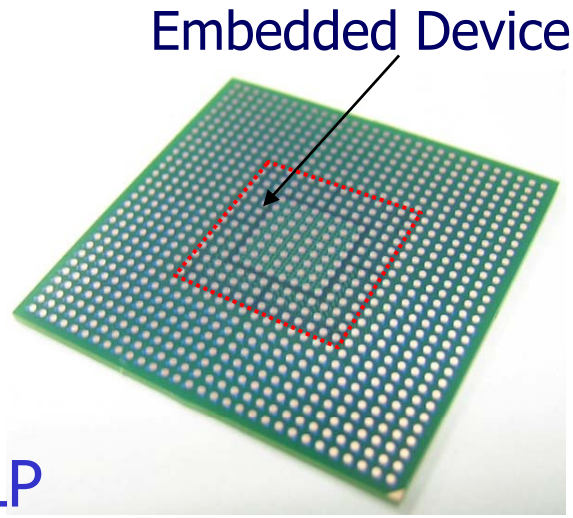
Package on Package



Fan-out WLP

Fan-out WLP

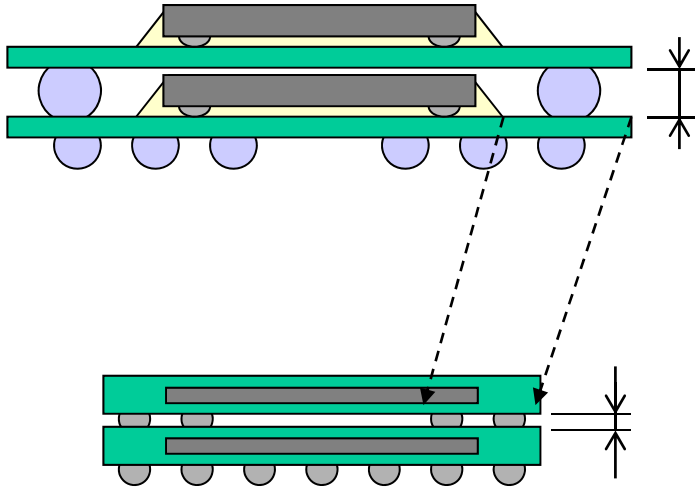


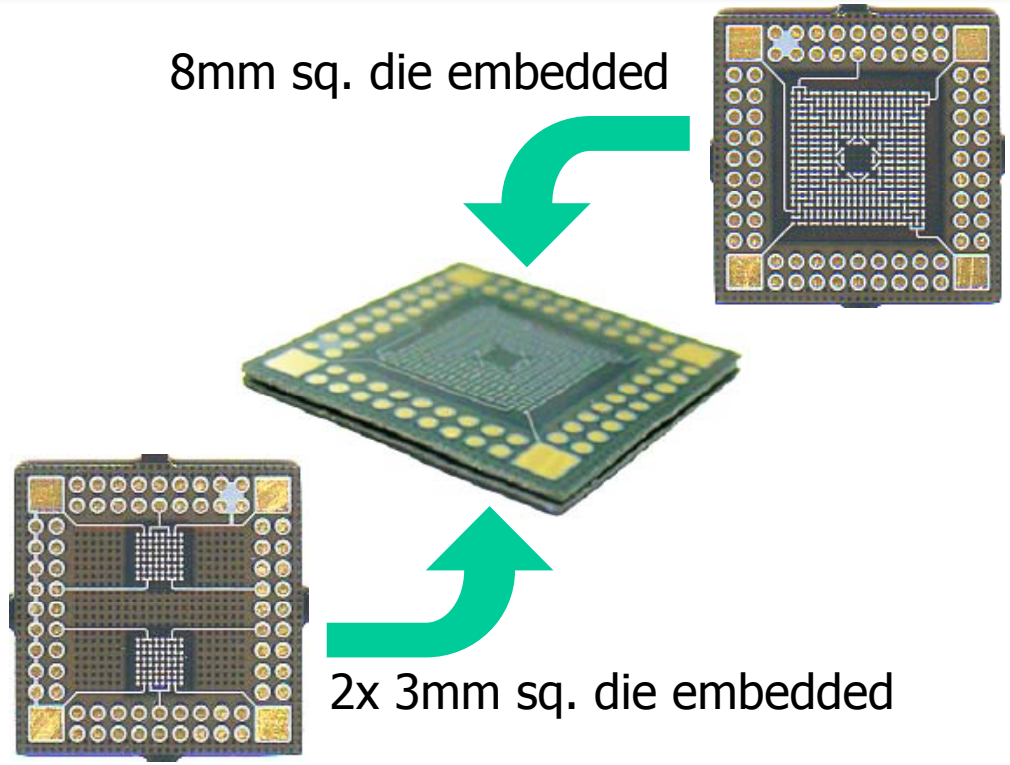


Enabling to expand the applicable area of WLP

IMAPS DPC(8th March 2011)

Package on Package





Reducing the footprint size and the thickness

- By placing the connecting bumps inside the outline of the die
- By reducing the diameter of connecting bumps

Contents

- Background
- Technical overview of the proposed embedded board
  - Wafer Level Packaging for embedding
  - Multilayer polyimide wiring board fabrication process
  - Fabricated results
- Reliability Issues
  - Applicable die size
  - Bending stress
  - Environmental tests
- Applications
- Conclusion

Conclusions

- Ultrathin WLP-IC embedded multilayer polyimide wiring boards have been developed utilizing
  - Ultrahin Wafer Level Packaging technology
  - Multilayer flex board
- The reliability of the embedded board have been confirmed
  - Applicable die dimensions
  - Bending limit test
  - Environmental test